Freescale Semiconductor
Application Note

AN3964
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MC13892 Layout Guidelines

1 Purpose

This document is intended to show good practices on how to layout the MC13892 PCB for a correct functionality of the whole system.

2 Scope

This document contains the packaging and recommended footprint for the IC, pinout, and layer stacking recommendations, and layout tips for routing transmission lines and switching power supply traces.

The MC13892 device in addition to other Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

Contents

3 Packaging

The MC13892 is offered in two BGA packages: a 139 pin 7x7 mm, 0.5 mm pitch package, and a 186 pin 12x12 mm, 0.8 mm pitch package. The package style is a low profile BGA semi populated matrix, MC13892VK includes 139 balls including 4 sets of triple corner balls, so in total 131 assigned signal pins, where the MC13892VL includes 186 balls, all of which are assigned signal pins.

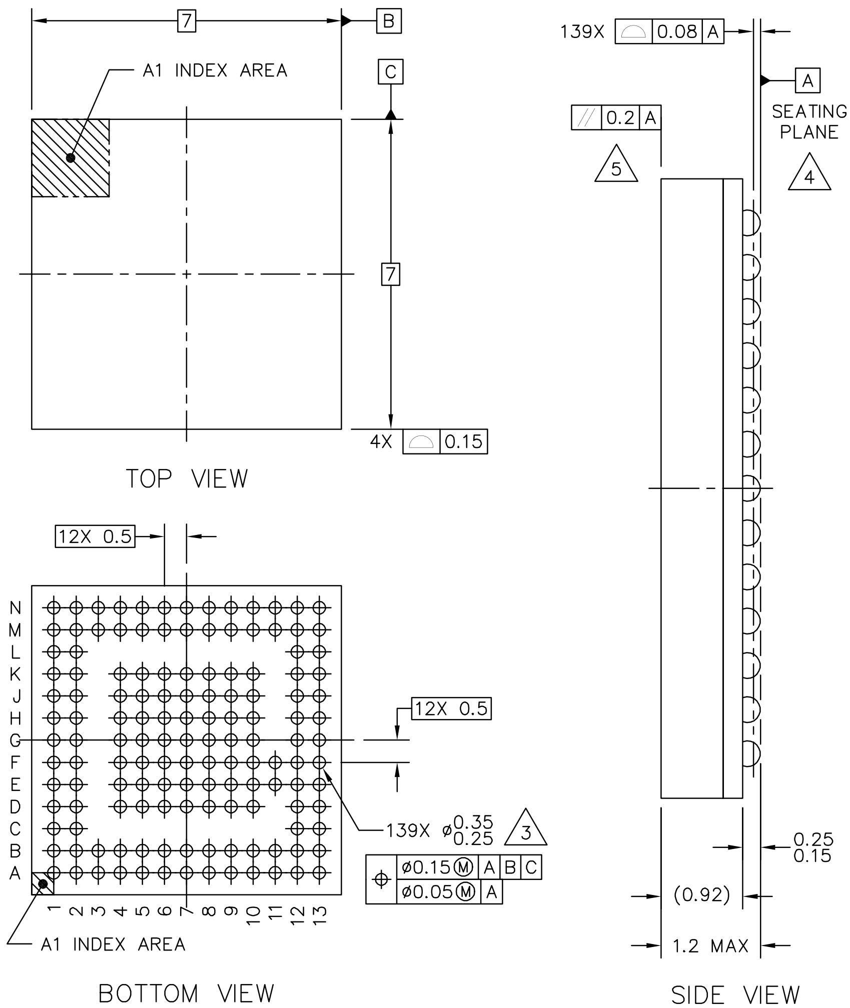

Figure 1. MC13892JVK Package

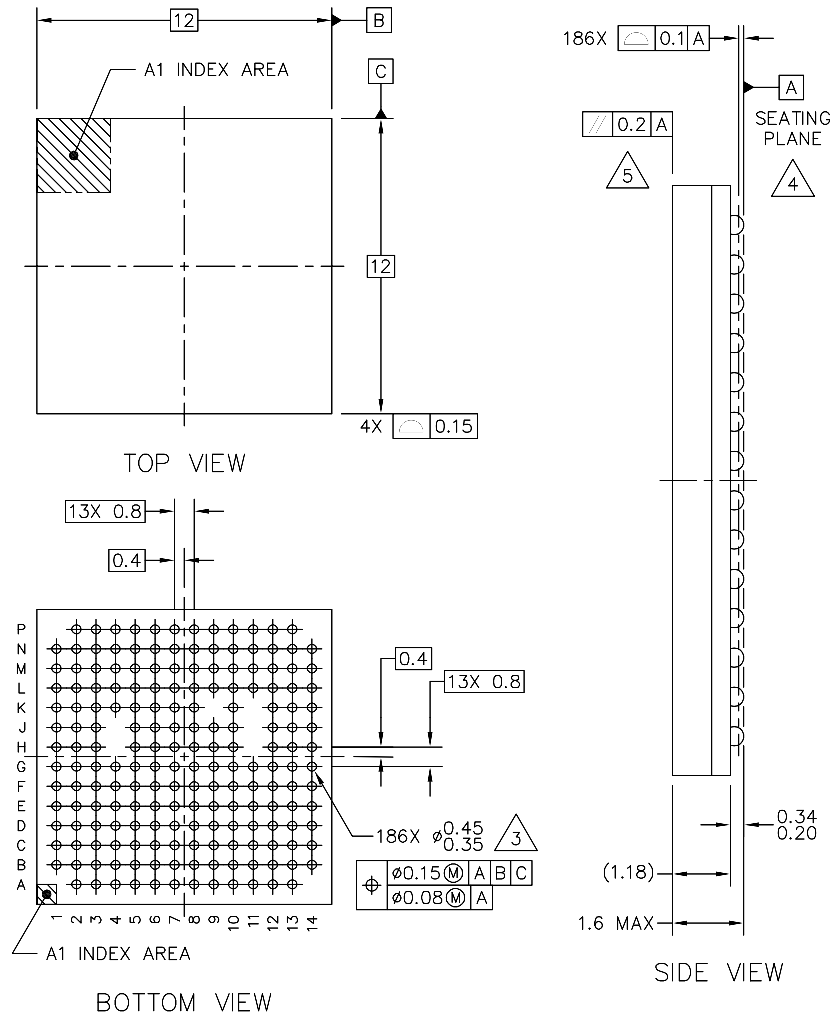

Figure 2. MC13892JVL Package

3.1 Recommended Footprints

The MC13892JVK footprint consists of 10 mil pads with a 19.68 mil pitch, and the MC13892JVL footprint has 16 mil pads with a 31.496mil pitch. These are recommended as shown in Figures 3 through 4.

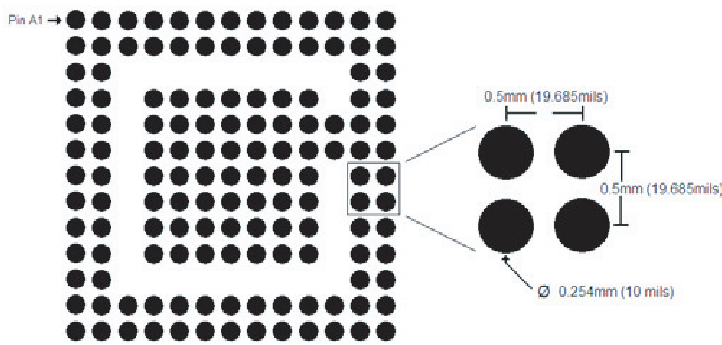

Figure 3. Recommended Footprint for the MC13892JVK (Top View)

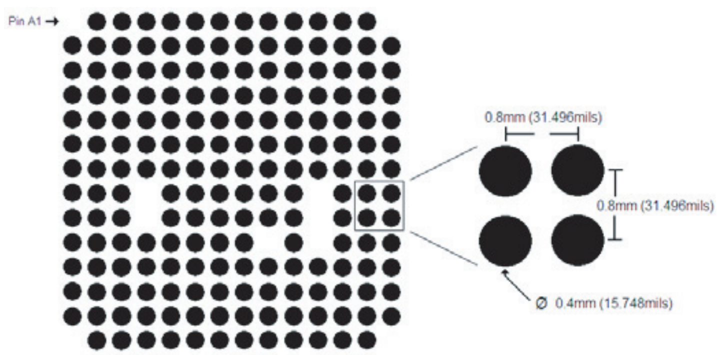

Figure 4. Recommended Footprint for the MC13892JVL (Top View)

A	VUSB2	VUSB2	VINUSB2	SWBSTIN	GNDSWBST	GNDBL	NC	MODE	VCORE	BATT	CHRGRAW	CHRGCTRL2	CHRGCTRL2
B	VUSB2	GPO1	DVS2	SWBSTOUT	LEDB	LEDKP	LEDR	GNDCORE	VCOREDIG	BP	CHRGCTRL1	BATTISNSCC	CHRGCTRL2
C	VINPLL	VSDDRV										CHRGISNS	BATTISNS
D	VUSB	VSD		SWBSTFB	LEDMD	DVS1	REFCORE	CHRGSE1B	LICELL	BATTFET		BPSNS	PWRON1
E	UVBUS	VPLL		LEDG	GNDLED	UID	PUMS2	GNDCHRG	CHRGLED	PWRON2	ADTRIG	INT	GNDSW1
F	GNDSW3	VBUSEN		SW3FB	LEDAD	GNDSUB	GNDSUB	GNDSUB	GPO3	GPO2	RESETBMCU	RESETB	SW1OUT
G	SW3OUT	VINUSB		SW4FB	GNDREG2	GNDSUB	GNDSUB	GNDSUB	PUMS1	WDI		GPO4	SW1IN
H	SW3IN	MISO		GNDSPI	GNDREG3	GNDSUB	GNDSUB	GNDSUB	GNDCTRL	SW1FB		STANDBYSEC	SW2IN
J	SW4IN	MOSI		CLK32KMCU	STANDBY	GNDADC	GNDREG1	PWRON3	TSX1	SW2FB		TSX2	SW2OUT
K	SW4OUT	SPIVCC		PWGTDRV1	CLK32K	VCAM	CFP	CFM	ADIN5	ADIN6		VVIDEODRV	GNDSW2
L	GNDSW4	CS										TSY2	VVIDEO
M	VGEN3	CLK	VGEN2	VSRTC	GNDRTC	VINCAMDRV	PWGTDRV2	VDIG	VINDIG	VGEN1DRV	ADIN7	TSY1	TSREF
N	VGEN3	VGEN3	VINGEN3DRV	VGEN2DRV	XTAL2	XTAL1	VINAUDIO	VAUDIO	VIOHI	VINIOHI	VGEN1	TSREF	TSREF

	Regulators
	Switchers
	Backlights
	Control Logic
	Charger
	RTC
	Grounds
	USB
	ADC
	SPI/I2C
	No Connect

Figure 5. MC13892JVK Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		VUSB2	VINUSB2	SWBSTOUT	SWBSTIN	GNDSUB	NC	MODE	VCORE	BATT	CHRGRAW	CHRGCTRL2	CHRGISNS	
B	VSDDRV	GPO1	GNDSUB	GNDSUB	LEDR	UID	DVS1	REFCORE	GNDCORE	CHRGSE1B	BP	GNDCHRG	BATTISNSCC	BATTISNS
C	VSD	DVS2	SWBSTFB	LEDB	LEDG	LEDKP	LEDAD	PUMS2	VCOREDIG	LICELL	BATTFET	BPSNS	GPO3	PUMS1
D	VUSB	VPLL	GNDSUB	GNDSUB	GNDSWBST	GNDLED	LEDMD	GNDBL	CHRGCTRL1	CHRGLED	PWRON1	PWRON3	ADTRIG	GPO4
E	UVBUS	GNDREG2	VINPLL	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	PWRON2	GPO2	INT	RESETBMCU
F	SW3OUT	VBUSEN	VINUSB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDCTRL	WDI	RESETB	SW1OUT
G	GNDSW3	GNDSW3	SW3FB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	SW1FB	GNDSW1	GNDSW1
H	SW3IN	SW3IN	GNDSUB		GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		GNDSUB	SW1IN	SW1IN
J	SW4IN	SW4IN	SW4FB		GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		SW2FB	SW2IN	SW2IN
K	GNDSW4	GNDSW4	SPIVCC	GNDSUB	GNDSUB	GNDSUB	GNDSUB	GNDSUB		GNDSUB		VVIDEODRV	GNDSW2	GNDSW2
L	SW4OUT	CS	GNDSPI	GNDSUB	GNDSUB	GNDSUB	VCAM	VINAUDIO	VDIG	GNDSUB	TSY2	STANDBYSEC	VVIDEO	SW2OUT
M	CLK	VINGEN3DRV	CLK32KMCU	CLK32K	VSRTC	STANDBY	VINCAMDRV	CFP	CFM	VGEN1DRV	VGEN1	TSX1	TSX2	TSY1
N	VGEN3	MOSI	VGEN2	GNDREG3	XTAL2	XTAL1	VAUDIO	PWGTDRV2	VIOHI	VINIOHI	GNDADC	ADIN5	ADIN7	TSREF
P		MISO	PWGTDRV1	VGEN2DRV	GNDSUB	GNDRTC	GNDSUB	GNDSUB	GNDSUB	GNDSUB	VINDIG	GNDREG1	ADIN6	

	Regulators
	Switchers
	Backlights
	Control Logic
	Charger
	RTC
	Grounds
	USB
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	SPI/I2C
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Figure 6. MC13892JVL Pinout

Signals are placed on the most convenient sides and grouped according to which block they belong. The most critical signals are located on the outer sides of the integrated circuit to easily route them, which improves the performance of the whole circuit.

Table 1 shows the recommended layer stack-up for the signals to receive good shielding.

Table 1. Layer stacking recommendations

Layer	Stack-up
Layer 1 (Top)	Signal
Layer 2 (Inner 1)	Fan-out/Ground
Layer 3 (Inner 2)	Power
Layer 4 (Bottom)	Signal/Ground

NOTE

Note: A more detailed layer design may be required to route the i.MX. If the MC13892 is being interfaced with an i.MX, just four of the layers will be needed to route it. Please note, for the MC13892VK, the fan-out needs to be made on the layer right next to the top, since micro vias will be needed to take the signals out of the IC as explained in the Pin Escape section.

3.2 Component Placement Hints

- Place these components first so they are as close as possible to the IC:
  - Place input caps of the switchers first (SW1, SW2, SW3, and SW4)
  - Place the output diode of the boost (SWBST)
  - Place output caps and diodes of the boost (SWBST) and SWLED
  - Place the REFCORE cap
- Shield feedback paths of the switchers (trace them on the bottom so the ground and power planes shield these traces).
- Sense pins must be directly connected to the pads of the sense resistors via separate traces (BATT, BATTISNS, BATTISNSCC, BPSNS, and CHRGISNS).
- BATTISNSCC must be connected directly to the pads of the sense resistor via a separate trace from BATTISNS.
- External pass devices of regulators must be closer to the load, but be careful with the sense and drive traces.
- Output caps of LDOs with the external pass device option should be close to the transistor (VVIDEO, VCAM, VSD, VGEN1, VGEN2 and VGEN3).
- Avoid a coupling trace between important signal/low noise supplies (like REFCORE) from any switching node.
- Ensure each of the components is referenced, or at least it does not have a long return path to the ground of the block to which it belongs.
- Trace REFCORE away from, or shielded from SWLEDOUT
- Traces that go from BP to a pin of the MC13892 must reach a capacitor before the pin.
- Routes for GNDSW should be suitably large. They will carry heavy switching currents.
- Switcher inductors should also be placed close to the IC, and switching node traces should be short and wide, to reduce conduction losses.

4 Pin Escape

Pin Escape is defined as the manner by which the signals leaving the IC from their associated pin, can be delivered on a circuit board trace of a specified size, to a point at which the traces can acquire the size necessary to perform their process function.

4.1 The MC13892VK Package

The most convenient way to approach pin escape is to take the signals coming from the bottom of the IC, with 3.0 mil traces on the top layer. Micro vias can be put on the pads of the footprint for the signals on the center of the IC. These will take the signals from the outer layer to the following one, once there, since this layer will not be as crowded as the top one, 5.0 mil traces can take the signal between the vias. These traces can become bigger once they are out from the bottom of the IC. More micro vias can be put among the pins to take the signal to another layer.

The recommendation is for the micro vias to have a 10 mil diameter (same as the pads of the footprint) with a 5.0 mil drill, which along with the 3.0 mil traces, will result in a 3.0 mil separation between the pad and the trace. This can be done with a 0.5 oz copper thickness on the top layer. The rest of the layers can have 1.0 oz copper thickness for better current handling. Care must be taken on these layers that the separation is more than 5.0 mils between traces, vias, pads, and planes. Reference Figure 7.

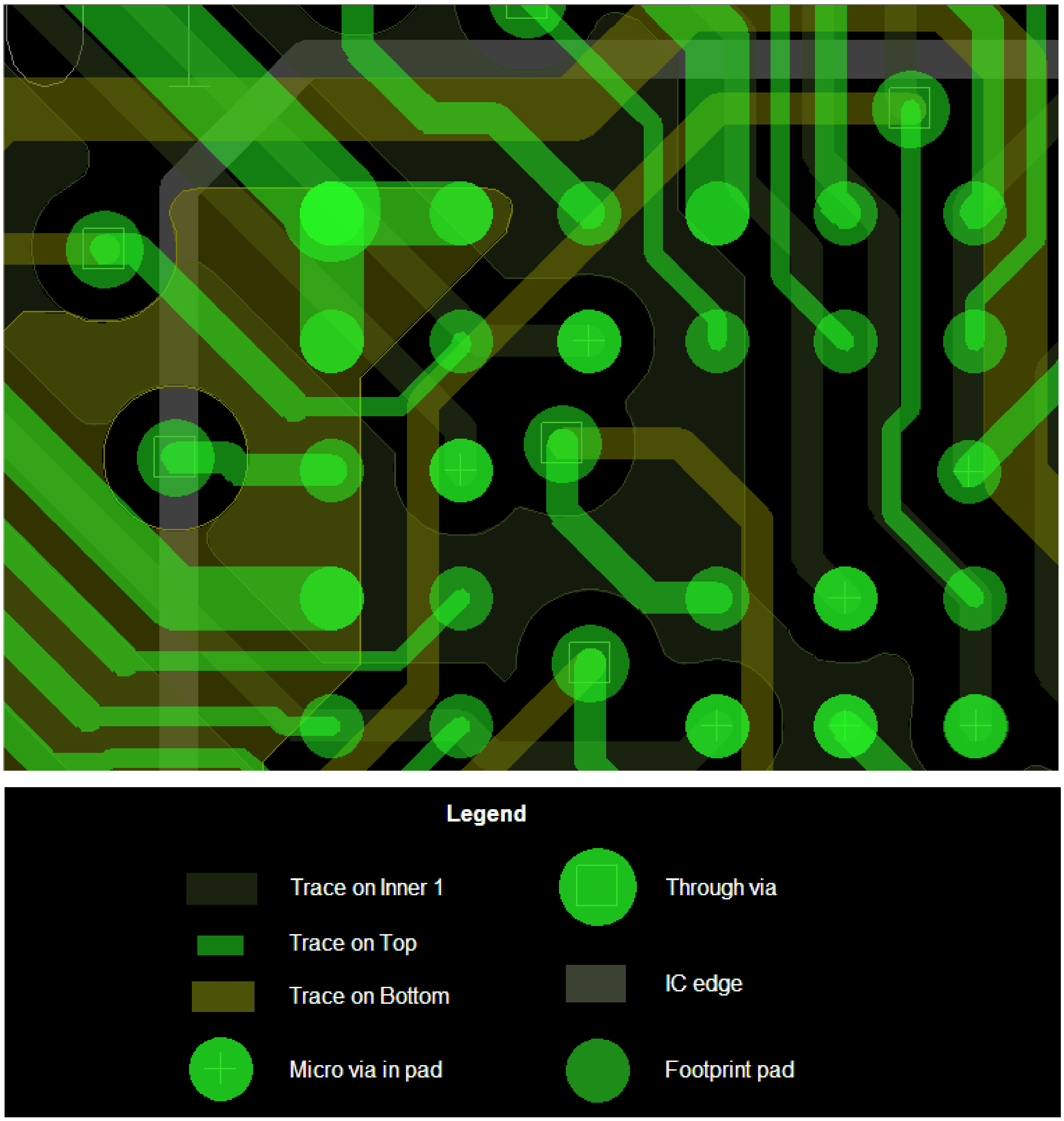

Figure 7. Pin Escape for the MC13892VK

Figure 7 shows the top left side of the MC13892VK. Note how the outer pins can have wider traces, and inner pins have narrow traces that become wider once out (escaping) from the bottom of the IC.

Bigger vias can be put on the clear area of rows C and L, and columns 3 and 11 (see Figure 5) to route critical signals.

The most convenient way to trace a signal depends on the length and width it must have. Tips for each kind of signal are found in SPI/I2C Communication and Real Time Clock Signals and Switching Power Supplies Traces.

4.2 The MC13892VL Package

Since the pins of this version of the device are wider, the use of micro vias can be avoided, and through vias can be used for the whole design for cost savings. The problem with through vias is that, since they go through the entire board from top to bottom, the drill can not be too narrow. The MC13892VK's small pins do not allow their use, but MC13892VL does.

Vias placed on the pads of the footprint can have a 12 mil diameter hole, with an 8.0 mil drill for the manufacturer to be able to use a conductive fill in them. 12 mil diameter vias will allow 9.0 mil traces to pass through them on the inner and bottom layers of the board, while 16 mil pads of the footprint will only allow 5.0 mil traces on the top layer below the IC. It is recommended to place high current traces on the bottom layer.

5.0 mil traces passing through 16 mil pads will result in a 5.0 mil separation between the pad and the trace, which can be made with a 1.0 oz copper thickness.

Taking advantage of the trough vias, the fan-out can be primarily made on the top and bottom layers, for the inner ones to be completely ground and power.

5 SPI/I2C Communication and Real Time Clock Signals

CLK is the fastest signal of the system, so it must be given special care. Here are some tips for routing the communication signals:

To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

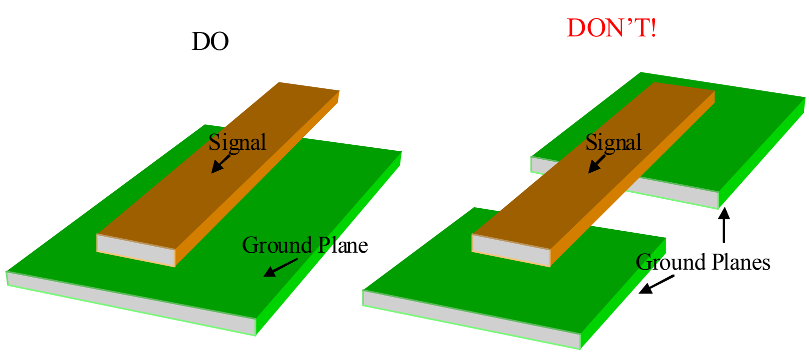

Figure 8. Recommended Shielding for Critical Signals.

These signals can be placed on an outer layer of the board to reduce their capacitance in respect to the ground plane.

The crystal connected to pins XTAL1 and XTAL2 must not have a ground plane directly below.

The following are clock signals: CLK, CLK32K, CLK32KMCU, XTAL1, and XTAL2. These signals must not run parallel to each other, or in the same routing layer. If it is necessary to run clock signals parallel to each other, or parallel to any other signal, then follow a MAX PARALLEL rule as follows:

- Up to 1 inch parallel length – 25 mil minimum separation.
- Up to 2 inch parallel length – 50 mil minimum separation.
- Up to 3 inch parallel length – 100 mil minimum separation.
- Up to 4 inch parallel length – 250 mil minimum separation.

Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers so there is a minimum area of proximity between signals.

Recommended Crystal Layout

Keep the crystal as close to the XTAL1 XTAL2 pins as possible.

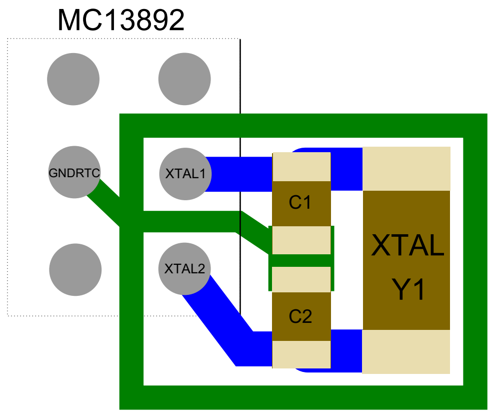

Figure 9. Crystal Layout

6 Switching Power Supplies Traces

6.1 Buck Converter

To place and route adequately external switcher components, follow the current paths of a Buck converter, as shown in Figure 10 and Figure 11.

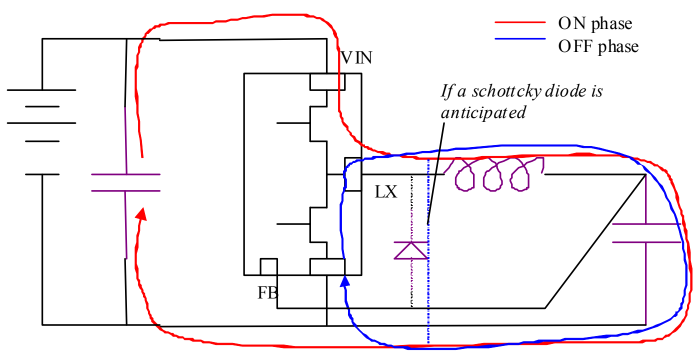

Figure 10. Current flow on a buck converter.

There are paths of 2 colors and paths with only one-color. Special attention must be paid to the one-color paths, because there the current alternates between zero and full value. These one-color paths are areas with high di/dt, that generate a significant magnetic field around the PCB traces.

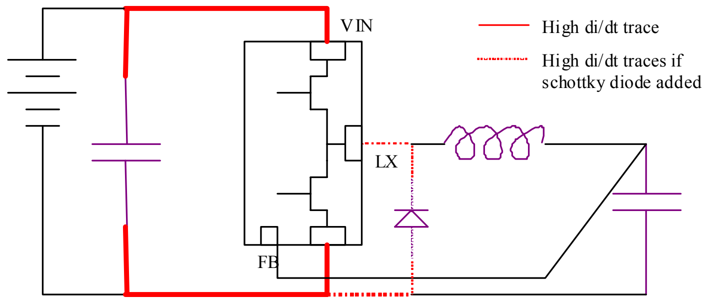

Figure 11. Critical traces of a buck converter.

It is important that all of these critical traces must be kept as short as possible. Each trace has an inductance proportional to the length. Inductance cannot tolerate high di/dt, so a high di/dt in long traces will result in a high ringing dv/dt. A wide trace is not a compensating solution for a long trace, as inductance is NOT inversely proportional to the width of the trace.

Traces must be very short and fairly wide (large amount of current flow in these traces), and should not go through any vias, as they also add impedance and inductance. Switcher components such as inductors and capacitors should be as close to the IC as possible to achieve a proper trace length.

Make sure that each trace is capable of handling the current it will carry. As a rule of thumb, it can be considered that a 10 mil trace with a thickness of 1.0 oz/ft^2, is capable of handling 1.0 ampere. Therefore, a trace that will carry 1.3 A in a 1.0 oz/ft^2 copper layer (as could be the case with an SW1 signal, because of the transient off the caps), must be 13 mils wide.

The switcher output to output capacitor connections should introduce negligible parasitic inductance, with regard to the coil inductance. Nevertheless, the switcher output capacitor to load connections are critical traces with high di/dt, and must have a maximum parasitic inductance of 1.0 nH, and an ohmic impedance of less than 20 mΩ.

6.2 Input Capacitor

An input capacitor is recommended to ensure a stable input voltage of the switcher during large load transients. It will provide the necessary energy to source current to the switcher until the battery supply is able to fill the demand. Ceramic capacitors fit well into applications, as they have a very small ESR.

The placement of this capacitor on the PCB is very important.

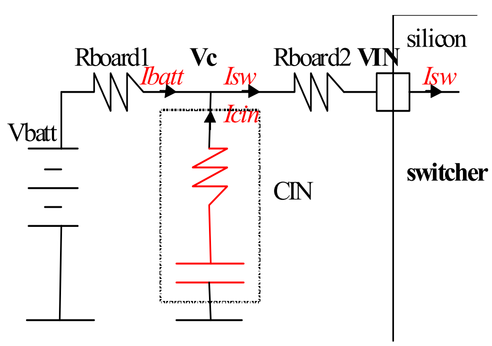

Figure 12. Input Capacitor Diagram.

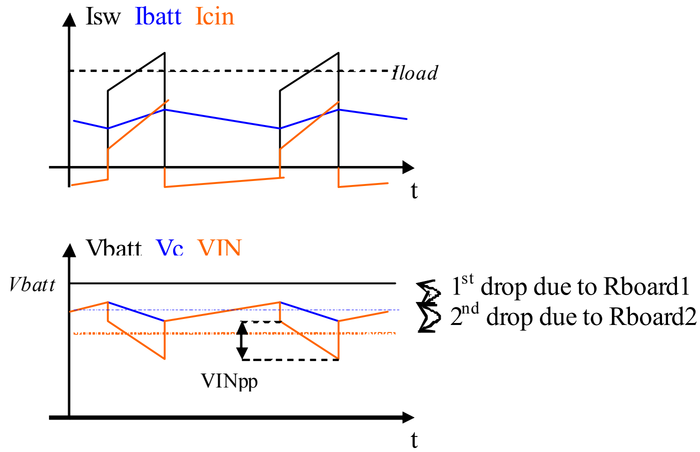

Figure 13. Current and Voltage Signals on a Buck Converter.

Figures 12 and 13 (ESR effect of CIN disregarded) bring out the effect of a resistive path Rboard1 and Rboard2, that must be minimized as much as possible. Rboard2 must be kept as small as possible, as all the switcher current (transient steady state and also local transient peaks) flows through this resistive path. Place CIN ACAP (as close as possible) to the chip**.**

Depending board constraints, it may not be possible to put the switchers close to CIN. In this case, it is recommendable to add an extra, small capacitor Cin_sw (still ceramic) ACAP to the switcher input. This extra cap will provide the main transient current during crossover transition of the switcher, whereas CIN will continue to prevent a drop on the input supply during large load transients.

Note: The recommended value for this capacitor on this application is 4.7 µF.

6.3 Switching Node

The components associated with this node must be placed as close as possible to one another to assure the switching currents are small enough not to contaminate other signals. However, care must be taken to ensure the copper traces joining these components together on this node are capable of handling the necessary current.

Figure 14 shows the placement and layout philosophy for a recommended PCB:

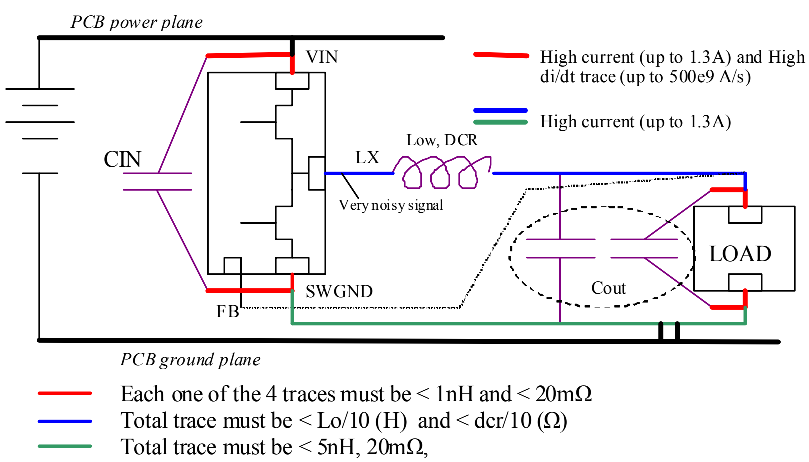

Figure 14. Placement and Layout Philosophy for a Recommended PCB.

6.4 Boost converter

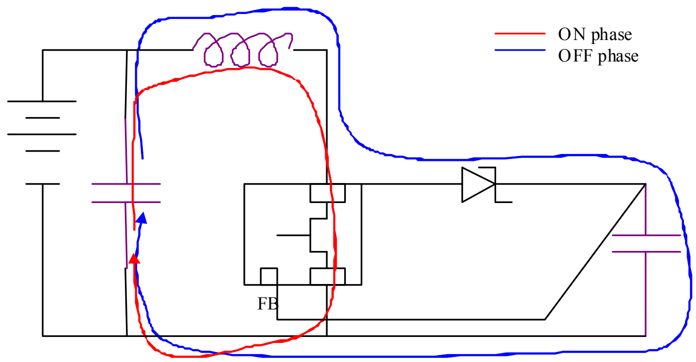

Figure 15. Current Flow on a Boost Converter.

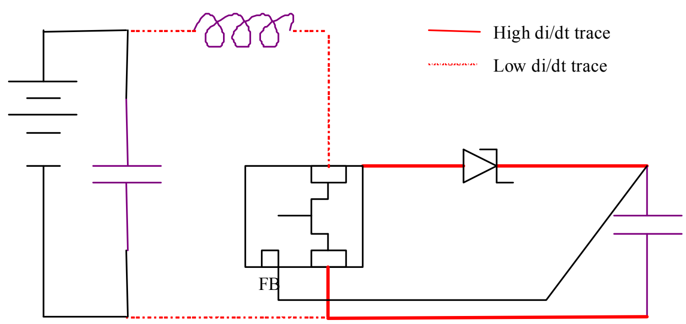

Figure 16. Critical Traces on a Boost Converter.

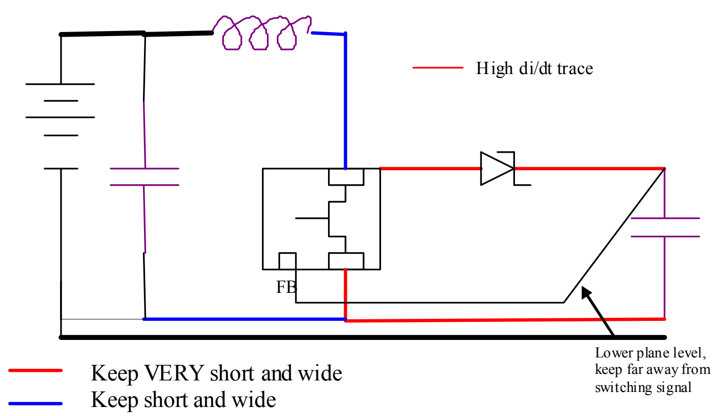

Figure 17. Placement and Layout Philosophy for a Recommended PCB.

7 Feedback Signals

To compensate for the voltage drop on the MC13892 power management IC switchers line due to the PCB wire resistance, the PCB wire resistance needs to be placed inside the closed loop of the switcher. The goal is to stabilize the voltage on that switcher line output.

The capacitor and coil components L and C are usually placed close to the MC13892 package. The voltage, SWxOUT, is equal to the programmed output switcher voltage, minus the dropout caused by the PCB trace. This dropout is also dependent on the DC load current on SWxOUT. In a typical configuration, the feedback loop is not usually shielded.

The feedback signal is the core of the loop, with the functional information fed back and compared for reference (this trace must be shielded from other signals). Moreover, it is a very high-impedance signal, so keep its trace thin and far from the switching signal (the length of this trace does not matter).

Freescale recommends following the L and C configuration as designated. The output capacitor should be placed near the point where the current is drawn on the output side of the PCB wire resistance, as shown in Figure 15. The PCB wire resistance is now inside the closed loop of the switcher, so it does not impact the DC voltage at SWxOUT.

The switcher feedback trace must be shielded, as this line is attached to a high-impedance point in the MC13892. Any perturbation on this line must be minimized to ensure the stability of the switcher.

Figure 18 shows the recommended configuration for the MC13892 power management IC, to stabilize the voltage on the switcher line.

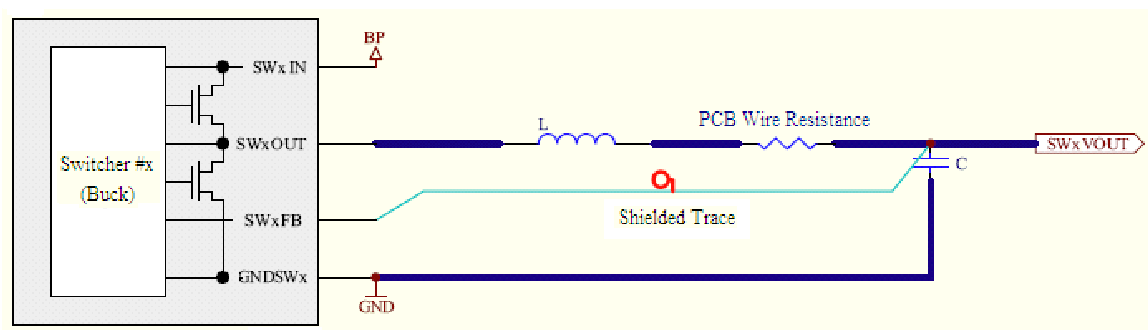

Figure 18. Recommended Configuration.

8 LDO and Battery Charger Routing

The LDOs and battery charger do not handle much current in this application, so their routing is not critical. The same philosophy must be followed for current handling on the traces though.

For a proper functionality of these supplies, bypass and output capacitors must be placed near the IC to achieve a good width and shortness of the traces. The ESR of the output capacitors of the external PNP LDOs must be between 20 and 100 mΩ, in order to achieve good stability. If they are not within these values, an additional resistor will be needed. This resistance can be achieved with a copper trace on the board and is also a cost saving.

The critical signals for the charger that must not be contaminated by high frequency or power ones are highlighted in Figure 19.

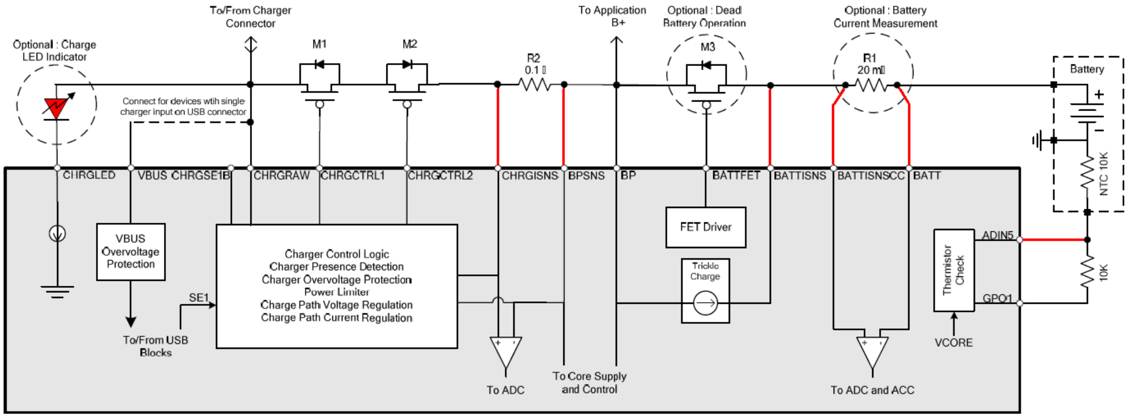

Figure 19. Critical Signals on the Battery Charger.

The sense lines should be routed from the sense resistor endpoints and should not be included in high current charge path. They should also have a maximum of 1.0 nH parasitic inductance and 30 mΩ of resistance.

Charge path can handle up to 1600 mA, so following the rule listed previously, for 1.0 oz copper, the trace width must be at least 16 mils.

As a placement suggestion, the thermistor must be located as close to the battery as possible for a correct temperature reading.

9 References

Document Number and Description		URL
MC13892	Data Sheet	http://www.freescale.com/files/analog/doc/data_sheet/MC13892.pdf

10 Revision History

Revision	Date	Description of Changes
2.0	4/2013	• Initial Release

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