*Click **here** for production status of specific part numbers.*

DS4520

9-Bit I²C Nonvolatile I/O Expander Plus Memory

General Description

The DS4520 is a 9-bit nonvolatile (NV) I/O expander with 64 bytes of NV user memory controlled by an I²C-compatible serial interface. The DS4520 offers users a digitally programmable alternative to hardware jumpers and mechanical switches that are being used to control digital logic nodes. Furthermore, the digital state of each pin can be read through the serial interface. Each I/O pin is independently configurable. The outputs are open drain with selectable pullups. Each output has the ability to sink up to 12mA. Since the device is NV, it powers up in the desired state allowing it to control digital logic inputs immediately on power-up without having to wait for the host CPU to initiate control.

Applications

- RAM-Based FPGA Bank Switching for Multiple Profiles
- Selecting Between Boot Flash
- Setting ASIC Configurations/Profiles
- Servers
- Network Storage
- Routers
- Telecom Equipment
- PC Peripherals

Features

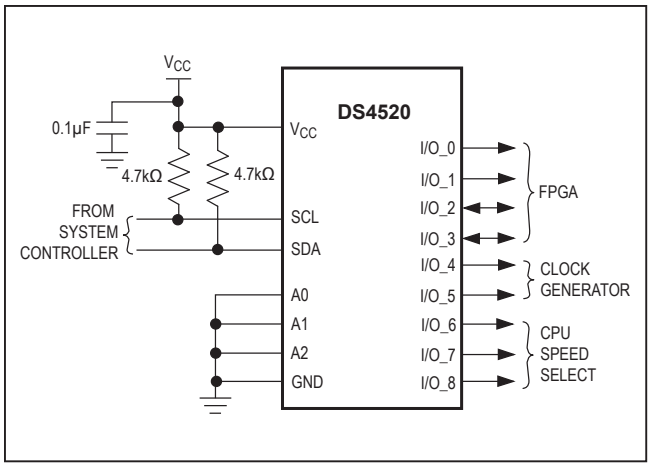
- Programmable Replacement for Mechanical Jumpers and Switches
- Nine NV Input/Output Pins
- 64-Byte NV User Memory (EEPROM)
- I²C-Compatible Serial Interface
- Up to 8 Devices Can be Multidropped on the Same I²C Bus
- Open-Drain Outputs with Configurable Pullups
- Outputs Capable of Sinking 12mA
- Low Power Consumption
- Wide Operating Voltage (2.7V to 5.5V)
- Operating Temperature Range: -40°C to +85°C

Ordering Information

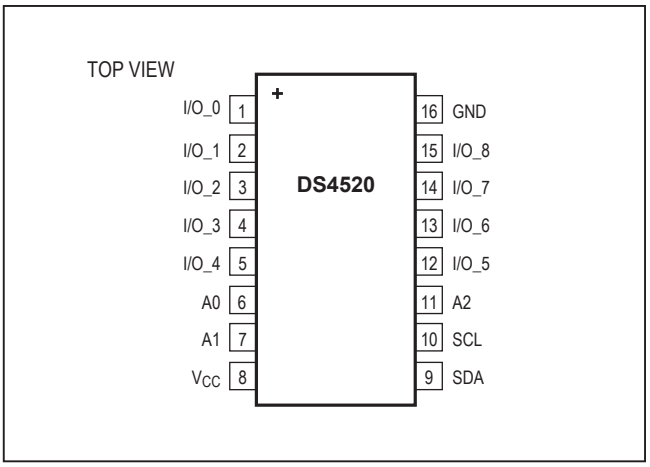
PART	TEMP RANGE	PIN-PACKAGE
DS4520E+	-40°C to +85°C	16 TSSOP

Add "TRL" for tape and reel orders.

Typical Operating Circuit



Pin Configuration



maxim integrated™

Absolute Maximum Ratings

Voltage on V_{CC}, SDA, and SCL Pins Relative to Ground.....-0.5V to +6.0V
Voltage on A0, A1, A2, and I/O_n [n = 0 to 8] Relative to Ground.....-0.5V to (VCC + 0.5V) not to exceed +6.0V

Operating Temperature Range..... -40°C to +85°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature... See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Input Logic 1	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		0.3 x V_{CC}	V

DC Electrical Characteristics

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{STBY}	(Note 2)		2	10	µA
Input Leakage	I_L		-1.0		+1.0	µA
Input Current each I/O Pin	$I_{I/O}$	0.4V < $V_{I/O}$ < 0.9V_{CC} (Note 3)	-1.0		+1.0	µA
Low-Level Output Voltage (SDA)	$V_{OL\ SDA}$	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	
I/O Pin Low-Level Output Voltage	$V_{OL\ I/O}$	12mA sink current			0.4	V
I/O Pin Pullup Resistors	R_{PU}		4.0	5.5	7.5	kΩ
I/O Capacitance	$C_{I/O}$	(Note 4)			10	pF
Power-On Reset Voltage	V_{POR}			1.6		V

AC Electrical Characteristics (See Figure 2)

(V_{CC} = +2.7V to +5.5V; T_A = -40°C to +85°C, unless otherwise noted. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 5)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 6)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 6)	20 + 0.1C_B		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 6)			400	pF
EEPROM Write Time	t_{WR}	(Note 7)		10	20	ms

Nonvolatile Memory Characteristics

(V_{CC} = +2.7V to +5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		+70°C (Note 4)	50,000			

Note 1: All voltages referenced to ground.

Note 2: I_{STBY} is specified with SDA = SCL = V_{CC}, outputs floating, and inputs connected to V_{CC} or GND.

Note 3: The DS4520 does not obstruct the SDA and SCL lines if V_{CC} is switched off as long as the voltages applied to these inputs do not violate their minimum and maximum input voltage levels.

Note 4: Guaranteed by design.

Note 5: Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

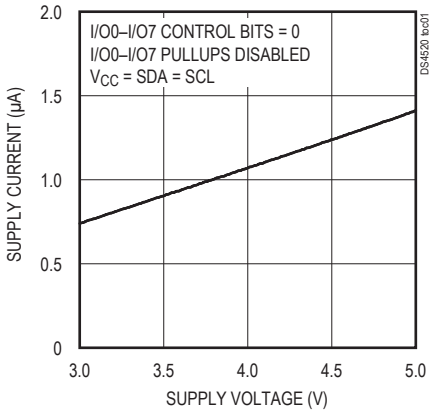
Note 6: C_B—total capacitance of one bus line in picofarads.

Note 7: EEPROM write time applies to all the EEPROM memory and SRAM shadowed EEPROM memory when SEE = 0. The EEPROM write time begins after a stop condition occurs.

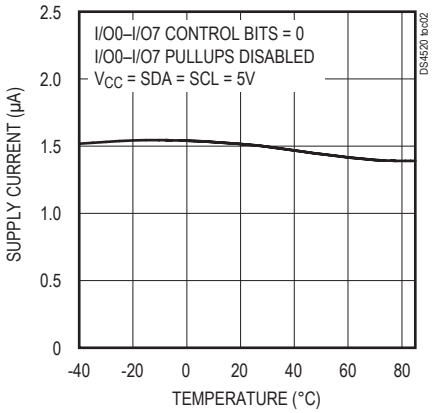
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

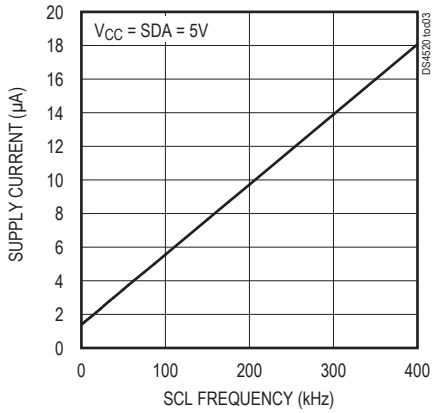
SUPPLY CURRENT vs. SUPPLY VOLTAGE



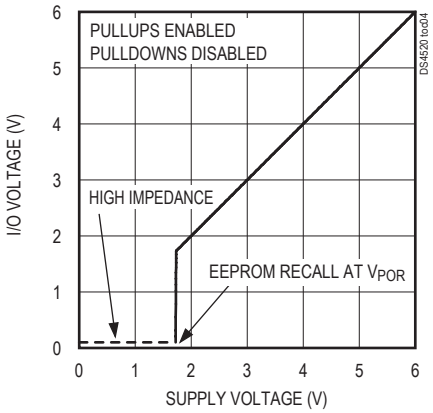
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SCL FREQUENCY



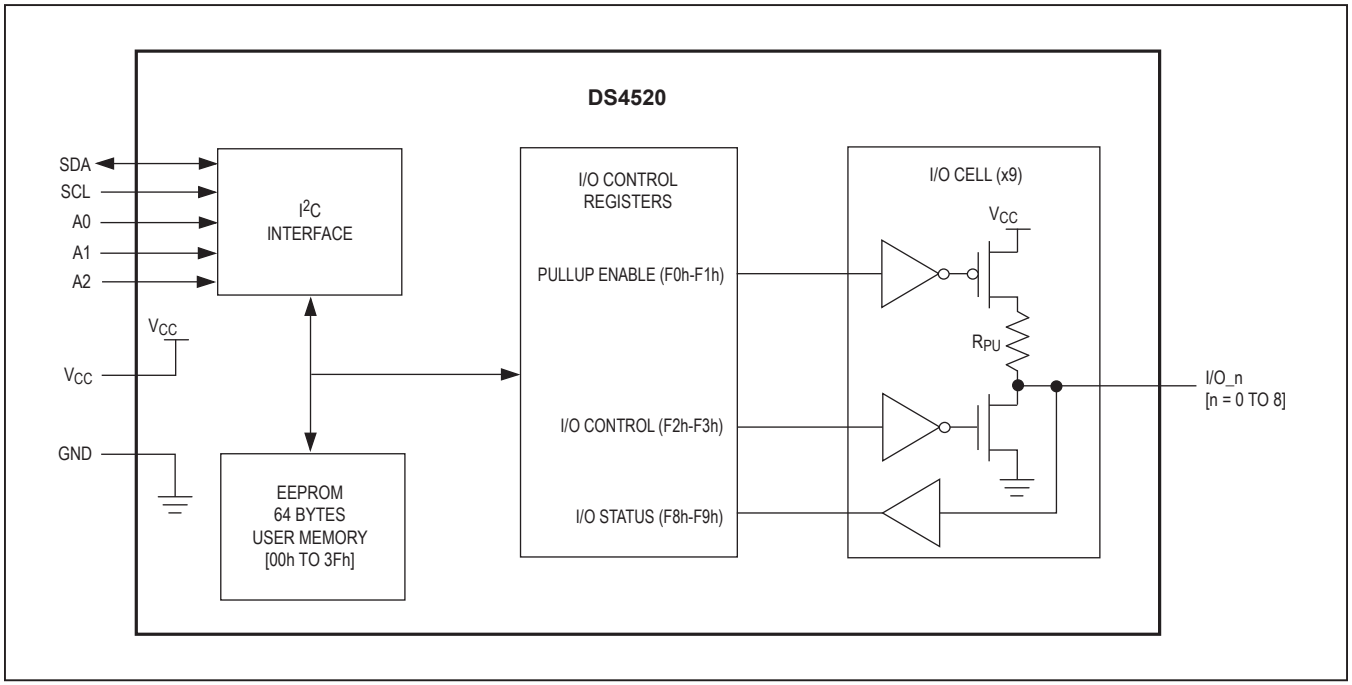
I/O OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	I/O_0	Input/Output 0. Bidirectional I/O pin.
2	I/O_1	Input/Output 1. Bidirectional I/O pin.
3	I/O_2	Input/Output 2. Bidirectional I/O pin.
4	I/O_3	Input/Output 3. Bidirectional I/O pin.
5	I/O_4	Input/Output 4. Bidirectional I/O pin.
6	A0	I²C Address Input. Inputs A0, A1, and A2 determine the I²C slave address of the device.
7	A1	I²C Address Input. Inputs A0, A1, and A2 determine the I²C slave address of the device.
8	V_{CC}	Power-Supply Voltage
9	SDA	I²C Serial Data Open-Drain Input/Output
10	SCL	I²C Serial Clock Input
11	A2	I²C Address Input. Inputs A0, A1, and A2 determine the I²C slave address of the device.
12	I/O_5	Input/Output 5. Bidirectional I/O pin.
13	I/O_6	Input/Output 6. Bidirectional I/O pin.
14	I/O_7	Input/Output 7. Bidirectional I/O pin.
15	I/O_8	Input/Output 8. Bidirectional I/O pin.
16	GND	Ground

Block Diagram



Detailed Description

The DS4520 contains nine bidirectional, NV, input/output (I/O) pins, and a 64-byte EEPROM user memory. The I/O pins and user memory are accessible through an I²C-compatible serial bus.

Programmable NV I/O Pins

Each programmable I/O pin consists of an input and an open-collector output with a selectable internal pullup resistor. To enable the pullups for each I/O pin, write to the Pullup Enable Registers (F0h and F1h). To pull the output low or place the pulldown transistor into a high-impedance state, write to the I/O Control Registers (F2h and F3h). To read the voltage levels present on the I/O pins, read the I/O Status Registers (F8h and F9h). To determine the status of the output register, read the I/O Control Registers and the Pullup Resistor Registers. The I/O Control Registers and the Pullup Enable Registers are all SRAM shadowed EEPROM registers. It is possible to disable the EEPROM writes of the registers using the SEE bit in the Configuration Register. This reduces the time required to write to the register and increases the amount of times the I/O pins can be adjusted before the EEPROM is worn out.

Memory Map and Memory Types

The DS4520 memory map is shown in Table 1. Three different types of memory are present in the DS4520: EEPROM, SRAM shadowed EEPROM, and SRAM. Memory locations specified as EEPROM are NV. Writing to these locations results in an EEPROM write cycle for a time specified by t_{WR} in the *AC Electrical Characteristics* table. Locations specified as SRAM shadowed EEPROM can be configured to operate in one of two modes specified by the SEE bit (the LSB of the Configuration Register, F4h). When the SEE bit = 0 (default), the memory location acts like EEPROM. However, when SEE = 1, shadow SRAM is written to instead of the EEPROM. This eliminates both the EEPROM write time, t_{RW}, as well as the concern of wearing out the EEPROM. This is ideal for applications that wish to constantly write to the I/Os. Power-up default states can be programmed for the I/Os in EEPROM (with SEE = 0) and then once powered-up, SEE can be written to a 1 so the I/Os can be updated periodically in SRAM. The final type of memory present in the DS4520 is standard SRAM.

Slave Address and Address Pins

The DS4520's slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 1. Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions. I²C communication is described in detail in a later section.

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers**.**

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, start, and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the timing diagram for applicable timing.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 2). Data is shifted into the device during the rising edge of the SCL.

Table 1. DS4520 Memory Map

ADDRESS	TYPE	NAME	FUNCTION	FACTORY DEFAULT
00h to 3Fh	EEPROM	User Memory	64 bytes of general-purpose user EEPROM.	00h
40 to E7h	—	Reserved	Undefined address space for future expansion. Reads and writes to this space have no effect on the device.	—
E8 to EFh	EEPROM	Reserved	—	—
F0h	SRAM Shadowed EEPROM_ [EEPROM writes are disabled if the SEE bit = 1]	Pullup Enable 0	Pullup enable for I/O_0 to I/O_7. I/O_0 is the LSB and I/O_7 is the MSB. Set the corresponding bit to enable the pullup; clear the bit to disable the pullup.	00h
F1h		Pullup Enable 1	Pullup enable for I/O_8. I/O_8 is the LSB. Only the LSB is used. Set the LSB bit to enable the pullup on I/O_8; clear the LSB to disable the pullup.	00h
F2h		I/O Control 0	I/O control for I/O_0 to I/O_7. I/O_0 is the LSB and I/O_7 is the MSB. Clearing the corresponding bit of the register pulls the selected I/O pin low; setting the bit places the pulldown transistor into a high-impedance state. When the pulldown is high impedance, the output floats if no pullup/down is connected to the pin.	FFh
F3h		I/O Control 1	I/O control for I/O_8. I/O_8 is the LSB. Only the LSB is used. Clearing the LSB of the register pulls the I/O_8 pin low; setting the LSB places the pulldown transistor into a high-impedance state. When the pulldown is high impedance, the output floats if no pullup/down is connected to the pin.	01h
F4h		Configuration	Configuration register. The LSB is the SEE bit. When set, this bit disables writes to the EEPROM; writing only affects the shadow SRAM. When set to 0, both the EEPROM and the shadow SRAM is written.	00h
F5h to F7h		User Memory	3 bytes of general-purpose user EEPROM.	00h
F8h	SRAM	I/O Status 0	I/O status for I/O_0 to I/O_7. I/O_0 is the LSB and I/O_7 is the MSB. Writing to this register has no effect. Read this register to determine the state of the I/O_0 to I/O_7 pins.	—
F9h		I/O Status 1	I/O status for I/O_8. I/O_8 is the LSB. Only the LSB is used; the other bits could be any value when read. Writing to this register has no effect. Read this register to determine the state of the I/O_8 pin.	
FAh to FFh		SRAM User Memory	6 bytes of general-purpose SRAM.	

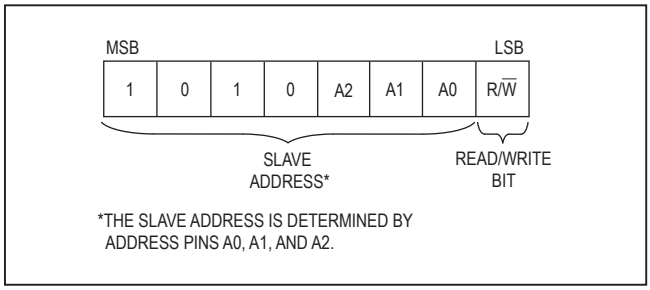


Figure 1. DS4520 Slave Address Byte

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read (see Figure 2). The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 2) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgement that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a start condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS4520's slave address is determined by the state of the A0, A1, and A2 address pins as shown in Figure 1. Address pins connected to GND result in a '0' in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a '1' in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in A0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1, (A1h in this case), the master is indicating it will read from the slave.

If an incorrect slave address is written, the DS4520 assumes the master is communicating with another I²C device and ignores the communication until the next start condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

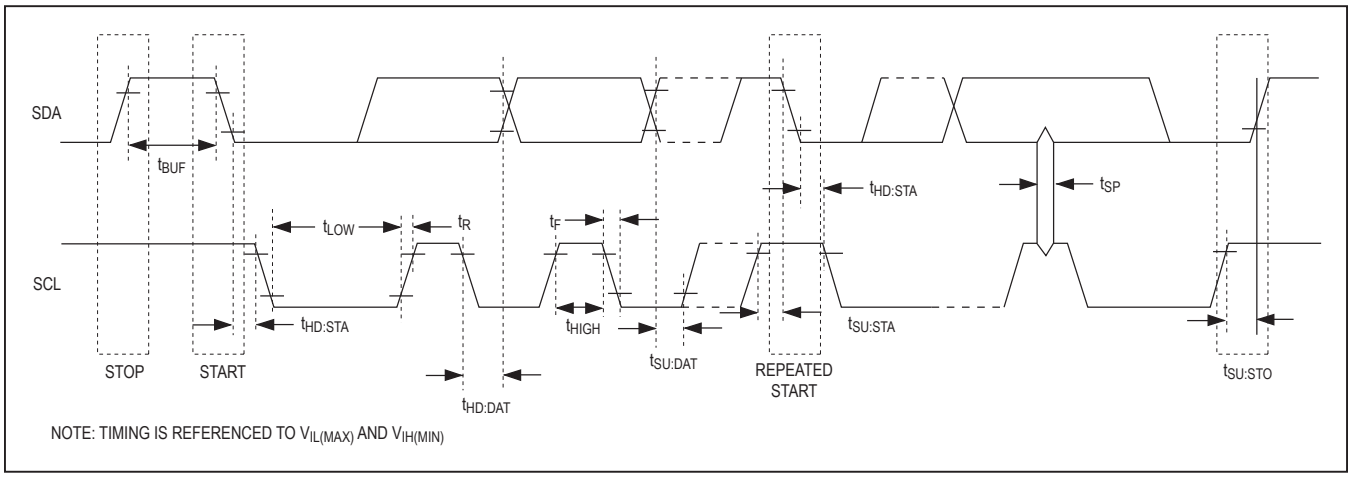


Figure 2. I²C Timing Diagram

I²C Communication

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a stop condition.

The DS4520 is capable of writing up to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page. Attempts to write to additional pages of memory without sending a stop condition between pages results in the address counter wrapping around to the beginning of the present row. The first row begins at address 00h and subsequent rows begin at multiples of 8 there on (08h, 10h, 18h, 20h, etc).

To prevent address wrapping from occurring, the master must send a stop condition at the end of the page, and then wait for the bus free or EEPROM write time to elapse. Then the master can generate a new start condition, write the slave address byte (R/$\overline{W}$ = 0), and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time an EEPROM page is written, the DS4520 requires the EEPROM write time (t_W) after the stop condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS4520, which allows communication to continue as soon as the device is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM Write Cycles: When EEPROM writes occur, the DS4520 writes the whole EEPROM memory page even if only a single byte on a page was modified. Writes that do not modify all 8 bytes on the page are valid and do not corrupt any other bytes on the same page. Because the whole page is written, even bytes on the page that were not modified during the transaction are still subject to a write cycle. The DS4520's EEPROM write cycles are specified in the Nonvolatile Memory Characteristics table. The specification shown is at the worst-case temperature. It is capable of handling approximately 10x that many writes at room temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a start condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a stop condition.

See Figure 3 for a read example using the repeated start condition to specify the starting memory location.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a stop condition.

Applications Information

Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power-supply pins. Typical values of decoupling capacitors are 0.01µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.

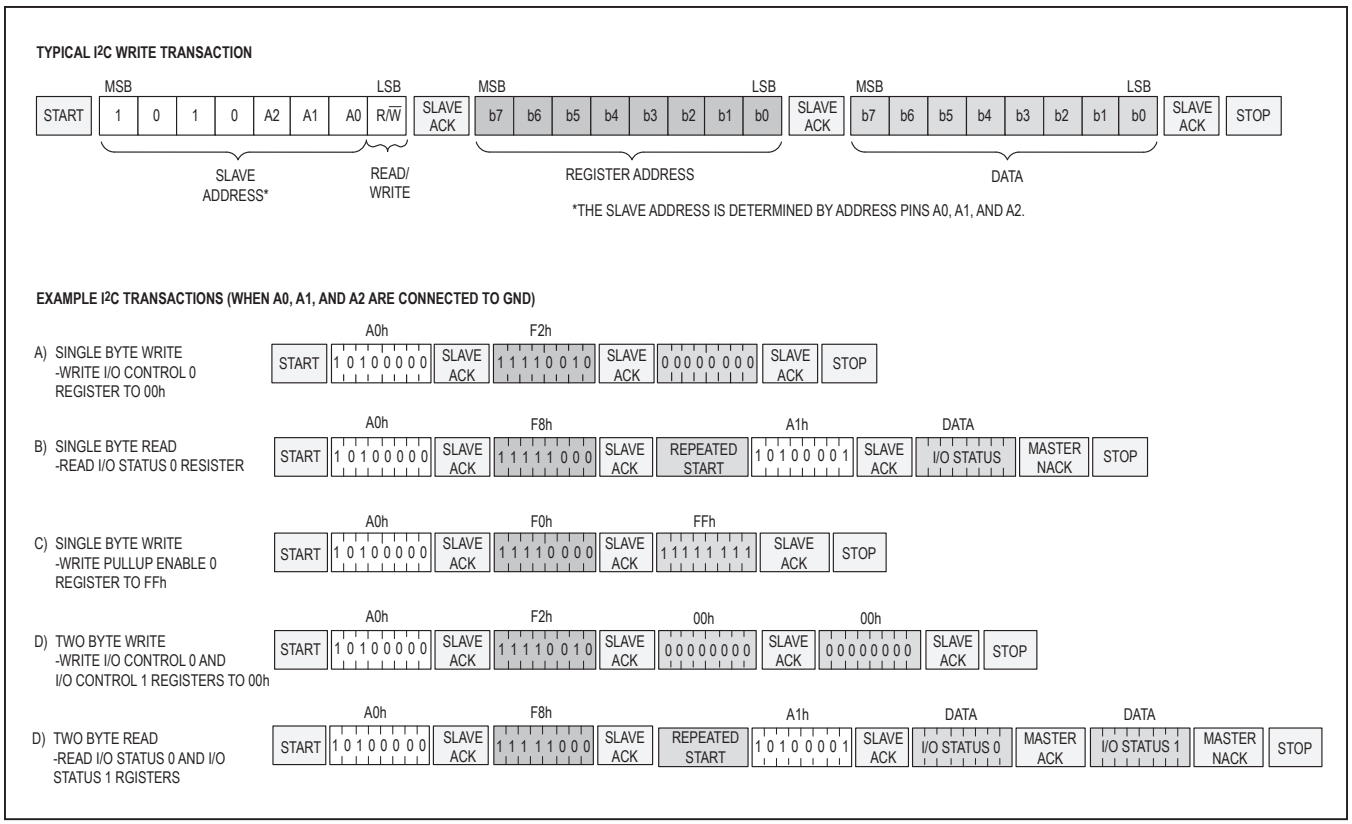


Figure 3. I²C Communication Examples

Chip Information

TRANSISTOR COUNT: 14,398

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
DS4520E+	U16-1	21-0066	90-0117

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/04	Initial release	—
1	7/18	Updated *Ordering Information*	1

