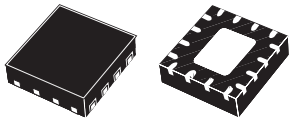
STG3482

Low voltage dual SP4T switch

Features

- Ultra low power dissipation:
  - I_{CC} = 0.1 µA (max.) at T_A = 25 °C
- Low “ON” resistance:
  - R_{ON} = 4.6 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
  - R_{ON} = 5.8 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range:
  - V_{CC} (Opr) = 1.65 to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 to 3.0 V
- Typical bandwidth (-3dB) at 300 MHz on all channels
- Latch-up performance exceeds 300 mA per JESD 78, Class II
- ESD performance exceeds JESD22
  - 2000-V Human body model (A114-A)



QFN16L (2.6 x 1.8 mm)

Description

The STG3482 is a high-speed CMOS low voltage dual analog SP4T (single pole four throw) switch or 4:1 multiplexer/demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65 to 4.3 V, making this device ideal for portable applications.

By controlling the SEL1 and SEL2, one of the independent channels will be connected to the common channel. An /OE pin is also available in this device to disconnect all the switches.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

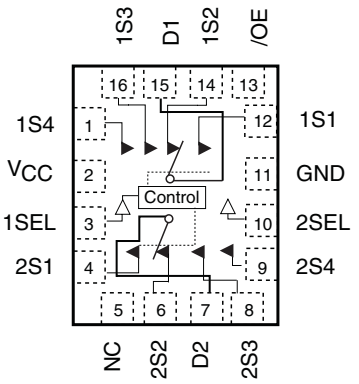
Table 1. Device summary

Order code	Package	Packaging
STG3482QTR	QFN16L (2.6 x 1.8 mm)	Tape and reel

Contents

1 Pin settings

Figure 1. Pin connection (top through view)



1.1 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	1S4	Independent channel
2	V_{CC}	Positive supply voltage
3	1SEL	Control
4	2S1	Independent channel
5	NC	No connect
6	2S2	Independent channel
7	D2	Common channels
8	2S3	Independent channel
9	2S4	Independent channel
10	2SEL	Control
11	GND	Ground (0V)
12	1S1	Independent channel
13	/OE	Output enable (active low)
14	1S2	Independent channel
15	D1	Common channel
16	1S3	Independent channel

Note: Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

2 Device summary

Figure 2. Input equivalent circuit

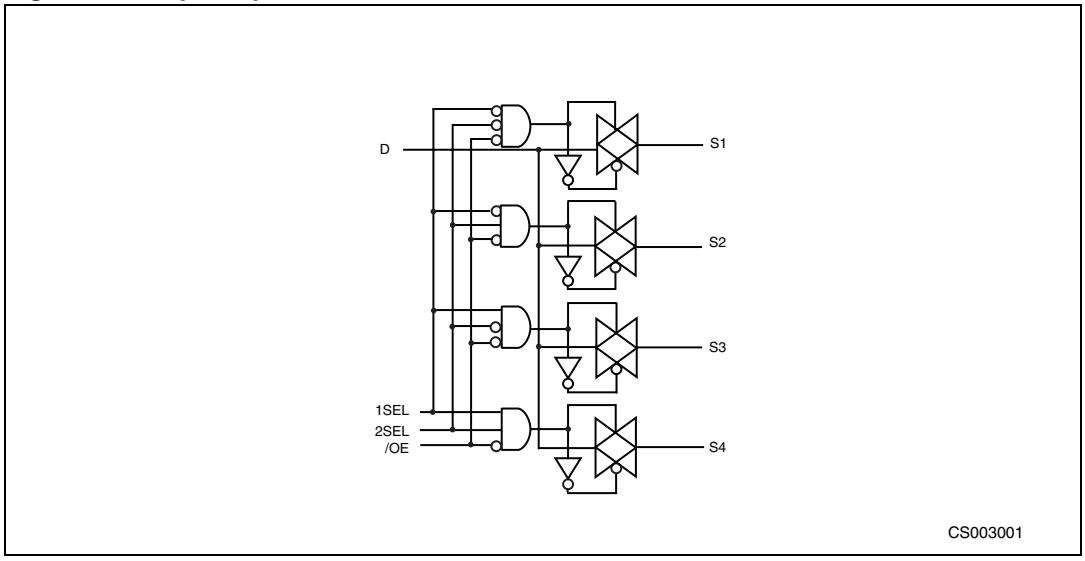


Table 3. Truth table

/OE	1SEL	2SEL	Switch connection
H	X	X	High-Z
L	L	L	D1-1S1, D2-2S1
L	L	H	D1-1S2, D2-2S2
L	H	L	D1-1S3, D2-2S3
L	H	H	D1-1S4, D2-2S4

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL}<0V)	-50	mA
I_{IK}	DC input diode current (V_{SEL}<0V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70ºC(1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 ºC by 18.5 mW/C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.3 V	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value				Unit
		Vcc (V)		TA = 25 °C		-40 to 85 °C		
				Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 –1.95				0.65 V_{CC}		V
		2.3 –2.5				1.2		
		2.7 –3.0				1.3		
		3.3 –3.6				1.4		
		4.3				1.6		
V_{IL}	Low level input voltage	1.65 –1.95			0.25		0.25	V
		2.3 –2.5			0.25		0.25	
		2.7 –3.0			0.25		0.25	
		3.3 –3.6			0.30		0.30	
		4.3			0.40		0.40	
R_{PEAK}	Switch on peak resistance	1.8	V_S = 0 V to V_{CC} I_S = 8 mA	12.0	16.0			Ω
		2.7		6.3	8.0			
		3.0		5.8	7.5			
		3.7		5.0	6.5			
		4.3		4.6	6.0			
R_{ON}	Switch ON resistance	3.0	V_S = 3 V I_S = 8 mA	4.0	5.2			Ω
		3.0	V_S = 0.8 V I_S = 8 mA	5.0	6.5			
ΔR_{ON}	ON resistance match between channels (1)	1.8	V_S @ R_{ON} Max I_S = 8mA	0.3				Ω
		2.7		0.3				
		3.0		0.3				
		3.7		0.3				
		4.3		0.3				
R_{FLAT}	ON resistance flatness (2)	1.8	V_S = 0V to V_{CC} I_S = 8mA	5.9				Ω
		2.7		1.9				
		3.0		1.6				
		3.7		1.4				
		4.3		1.6				

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value				Unit
		Vcc (V)		TA = 25 °C		-40 to 85 °C		
				Typ	Max	Min	Max	
I_{OFF}	OFF state leakage current (SN), (D)	4.3	V_S = 0.3 or 4 V		±20		±100	nA
I_{IN}	Input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3 V		±0.1		±1	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = V_{CC} or GND		±0.1		±1.0	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{1SEL}, V_{2SEL} = 1.65 V	±37	±50		±100	µA
			V_{1SEL}, V_{2SEL} = 1.80 V	±33	±40		±50	
			V_{1SEL}, V_{2SEL} = 2.60 V	±12	±20		±30	
			V_{1SEL}, V_{2SEL} = 0 V_{OE} = 1.65 V	±19	±25		±50	
			V_{1SEL}, V_{2SEL} = 0 V_{OE} = 1.80 V	±17	±20		±25	
			V_{1SEL}, V_{2SEL} = 0 V_{OE} = 2.60 V	±6	±10		±15	

1. ΔRon = Ron(max) - Ron(Min)
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq 5$ ns)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 –1.95			0.30				ns
		2.3 –2.7			0.30				
		3.0 –3.3			0.27				
		3.6 –4.3			0.28				
t_{ON}	Turn-ON time	1.65 –1.95	V_S = 0.8 V		37				ns
		2.3 –2.7	V_S = 1.5 V		20	30		34	
		3.0 –3.3			15	25		26	
		3.6 – 4.3			12	18		20	
t_{OFF}	Turn-OFF time	1.65 – 1.95	V_S = 0.8		23				ns
		2.3 – 2.7	V_S = 1.5 V		17	23		17	
		3.0 – 3.3			12	18		12	
		3.6 – 4.3			10	15		10	
t_D	Break before make time delay	1.65 –1.95	C_L = 35 pF R_L = 50 Ω V_S = 1.5 V	1	24				ns
		2.3 – 2.7		1	15				
		3.0 –3.3		1	11				
		3.6 – 4.3		1	9				
Q	Charge injection	1.65	C_L= 100 pF V_{GEN} = 0 V R_{GEN} = 0 Ω		10				pC
		2.3			11				
		3.0			11				
		4.3			11				

Table 8. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR	OFF Isolation (1)	1.65 — 4.3	V_S = 1V_{RMS}, f = 1 MHz Signal = 0 dBm		-75				dB
			V_S = 1V_{RMS}, f = 10 MHz Signal = 0 dBm		-58				
Xtalk	Crosstalk	1.65 — 4.3	V_S = 1V_{RMS}, f = 1 MHz Signal = 0 dBm		-77				dB
			V_S = 1V_{RMS}, f = 10 MHz Signal = 0 dBm		-60				
THD	Total harmonic distortion	3.7	f = 20 Hz to 20 kHz R_L = 32 Ω, C_L= 50 Ω V_{IN} = 2.8 V_{P-P} V_{DC} = V_{CC}/2		0.01	0.02			%
PSRR	Power supply rejection ratio	3.7	f = 217 Hz, R_L = 32 Ω, C_L = 50 Ω V_{ripple} = 150 mV V_{DC} = V_{CC}/2		-60				dB
BW	-3dB bandwidth	3.0 — 4.3	R_L = 50 Ω Bias = 1 V		300				MHz
D_G	Differential gain	3.0 — 4.3	RL = 150 Ω		0.64				%
D_P	Differential phase	3.0 — 4.3	RL = 150 Ω		0.1				deg
C_{IN}	Control pin input capacitance		V_{CC} = 0 V		1.5				pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	f = 1 MHz		6.7				
C_{OFF}	Sn port capacitance when switch is disabled	3.3	f = 1 MHz		2.8				

1. Off Isolation = 20Log10 (V_D/V_S), V_D = output. V_S = input to off switch.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 3. QFN16L (2.6 x 1.8 mm) package outline

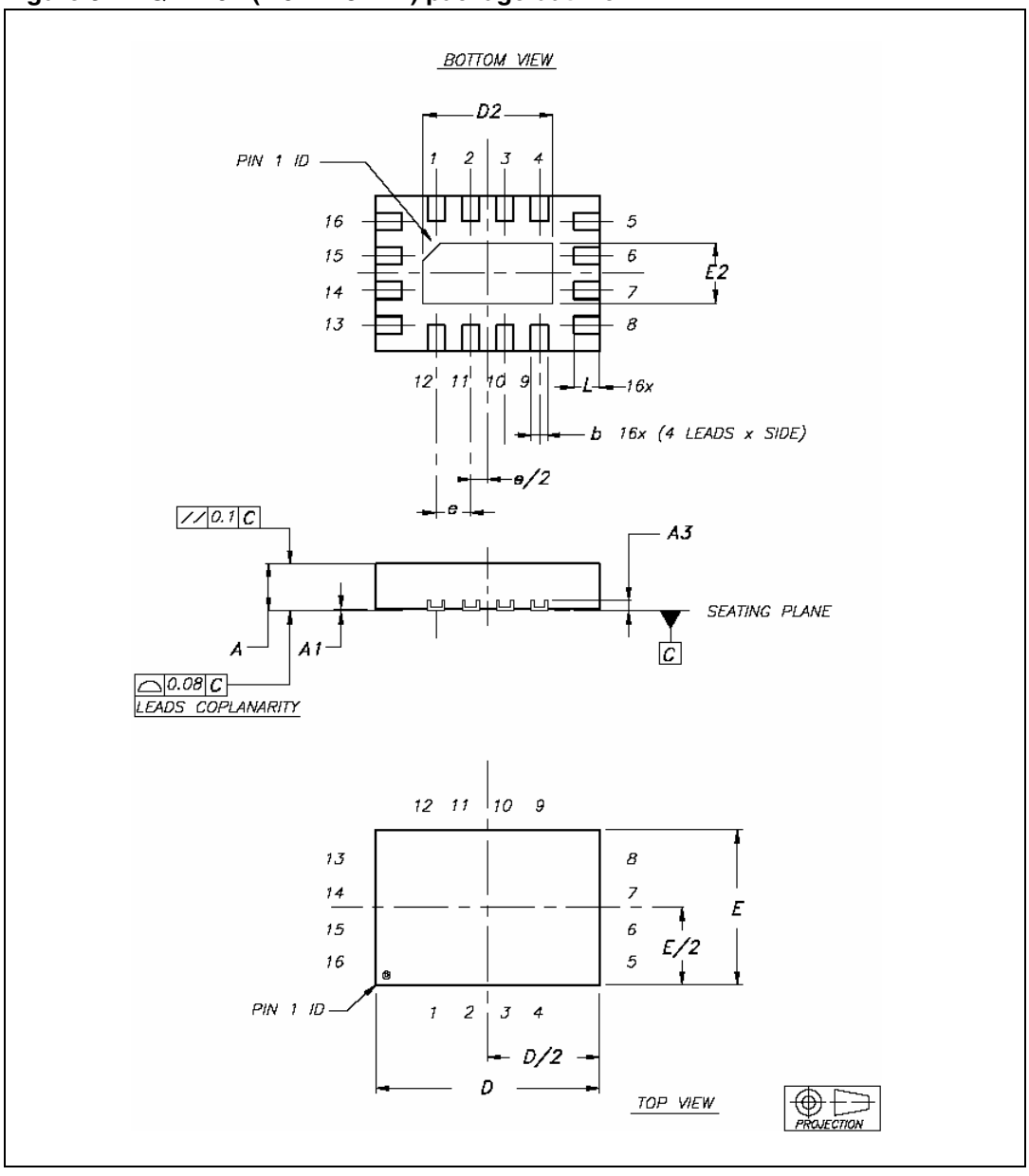
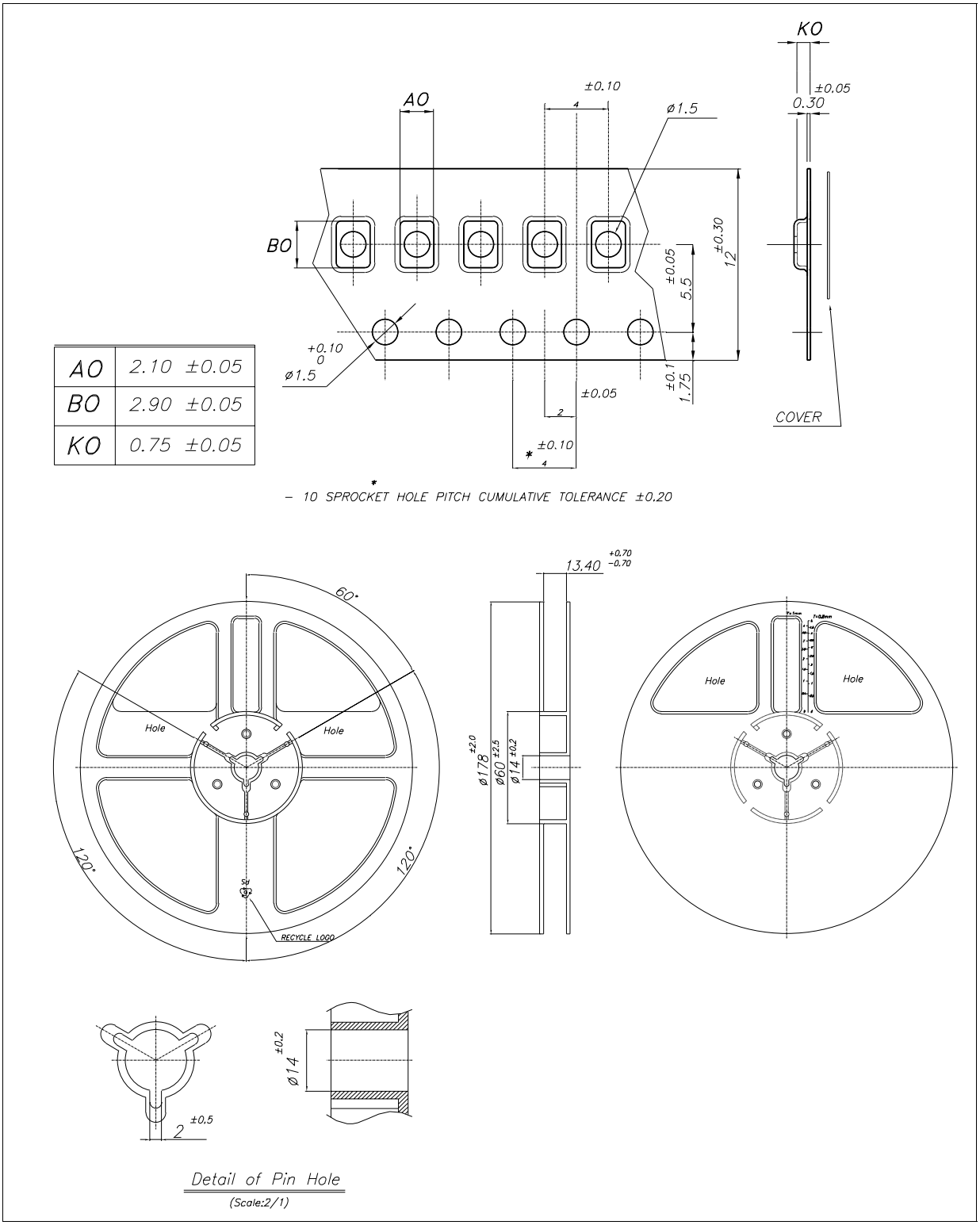


Table 9. QFN16L (2.6 x 1.8 mm) mechanical data

Symbol	Millimeters		
	Typ	Min	Max
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127		
b	0.20	0.15	0.25
D	2.60	2.50	2.70
D2	1.50	1.40	1.60
E	1.80	1.70	1.90
E2	0.70	0.60	0.80
e	0.40		
L	0.30	0.25	0.35

1. VFQFPN - standard for thermally enhanced vey fine pitch quad flat package no leads.
2. The leads size is comprehensive of the thickness of the leads finishing material.
3. Dimensions do not include mold protusion.
4. Package outline exclusive of metal burrs dimensions.
5. Shipping media tape and reel units: 3000

Figure 4. QFN16L (2.6 x 1.8 mm) tape and reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Nov-2006	1	Initial release.
20-Nov-2007	2	Updated latch-up performance value in *Features section n on page 1*, minor text changes, updated *Figure 1 on page 3*, *Table 2 on page 3*, *Table 5 on page 5*, *Table 6 on page 6*, *Table 7 on page 8*

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