

**NOT RECOMMENDED FOR NEW DESIGNS  
RECOMMENDED REPLACEMENT PART  
ISL97519A**

**ISL97702**

Boost with Dual Reference Outputs

FN7462  
Rev 0.00  
October 13, 2005

The ISL97702 represents a high efficiency, boost converter with integrated boost FET, boost diode and input disconnect FET. A dual feedback circuit allows simple switching between two pre-defined output voltages using a single logic input.

With an input voltage of 2.3V to 5.5V the ISL97702 has an output capability of up to 50mA at 18V using integrated 500mA switches. Efficiencies are up to 87%. The integrated protection FET is used to disconnect the boost inductor from the input supply whenever an output fault condition is detected, or when the device is disabled. This gives 0 output current in the disabled mode, compared to standard boost converters where current can still flow when the device is disabled.

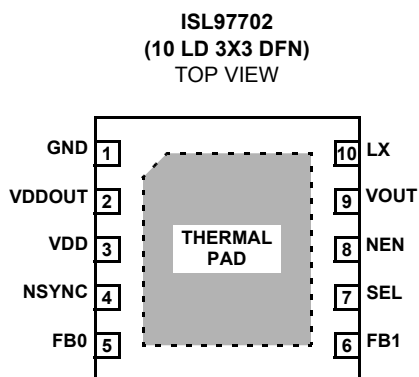
The ISL97702 comes in the 10 Ld 3x3 DFN package and is specified for operation over the -40°C to 85°C temperature range.

**Ordering Information**

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL97702IRZ (Note)	97702IRZ	-	10 Ld 3x3 DFN (Pb-Free)	MDP0047
ISL97702IRZ-T7 (Note)	97702IRZ	7"	10 Ld 3x3 DFN (Pb-Free)	MDP0047
ISL97702IRZ-T13 (Note)	97702IRZ	13"	10 Ld 3x3 DFN (Pb-Free)	MDP0047

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pinout**



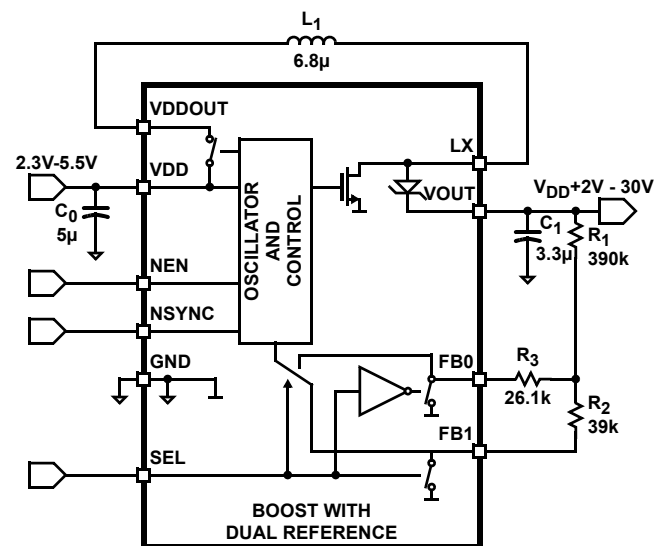
**Features**

- Up to 87% efficiency
- 2.3V to 5.5V input
- Up to 28V output
- 50mA at 18V
- Integrated boost Schottky diode
- Input voltage disconnect switch
- Dual output voltage selectable
- Synchronization input
- Chip enable
- 10 Ld 3x3 DFN package
- Pb-free plus anneal available (RoHS compliant)

**Applications**

- OLED display power
- LED display power
- Adjustable power supplies

**Typical Application Diagram**



$$V(VOUT)_0 = (390k + 39k) / 39k * 1.15V = 12.65V$$

$$V(VOUT)_1 = (390k + 26.1k) / 26.1k * 1.15V = 18.33V$$

NEN	SEL	V <sub>OUT</sub>
1	X	High Z
0	0	V <sub>OUT0</sub>
0	1	V <sub>OUT1</sub>

**Block Diagram**

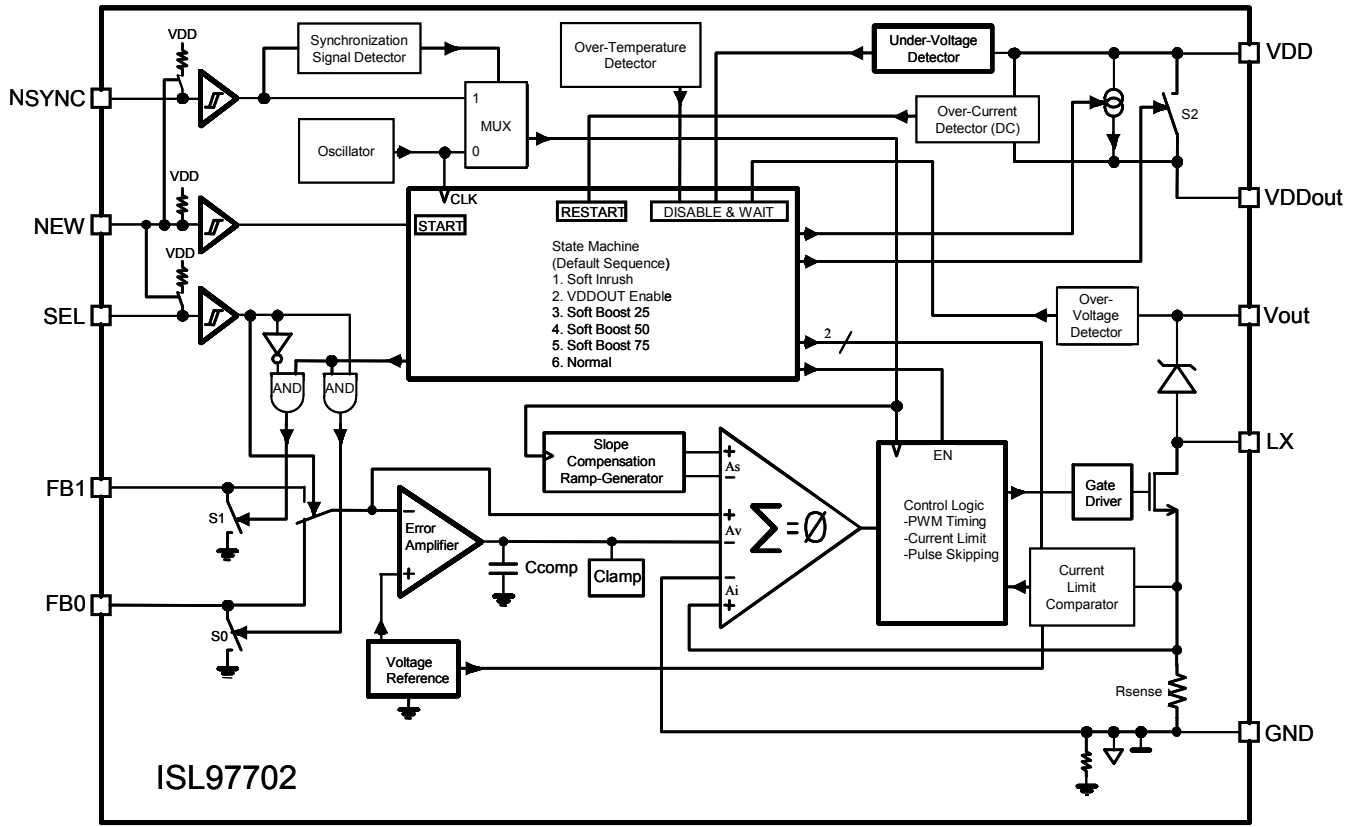


FIGURE 1. ISL97702 BLOCK DIAGRAM

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

VDD to GND	-0.3 to 6V	Continuous Current in VDD, GND, VDDOUT, LX	650mA
V <sub>OUT</sub> to GND	-0.3 to 31V	Continuous Current in NSYNC, FB0, FB1, SEL, NEN	10mA
LX to GND	V <sub>OUT</sub> +1V	Storage Temperature	-65°C to +150°C
VDDOUT, NSYNC, FB0, FB1, SEL, NEN to GND	-0.3V to VDD+0.3V	T <sub>A</sub> Ambient Operating Temperature	-40°C to +85°C
		T <sub>J</sub> Operating Junction Temperature	+125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed.

**Electrical Specifications** VDD = 3.6V, GND = NEN = 0V, SEL = NSYNC = VDD, R1 = 390k, R2 = 39k, R3 = 26.1k,  
L = 10μH, T<sub>A</sub> = -40°C to +85°C unless otherwise stated

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
VDD	Supply Operating Voltage Range		2.3		5.5	V
I <sub>DIS</sub>	Supply Current when Disabled	NEN = VDD		0.1	3	μA
<b>LOGIC INPUTS – NEN, NSYNC, SEL</b>						
R <sub>up</sub>	Pull-up Resistor	Enabled, Input at GND	150	250	350	kΩ
I <sub>IL</sub>	Leakage Current when Disabled	Disabled, Input at GND	-1		1	μA
V <sub>HI</sub>	Logic High Threshold		1.8			V
V <sub>LO</sub>	Logic Low Threshold				0.7	V
<b>POWER-ON RESET – VDD</b>						
V <sub>RES_ON</sub>	Power On Reset Threshold	VDD rising		2.2	2.3	V
V <sub>RES_OFF</sub>	Power Off Threshold	VDD falling	1.9	2		V
<b>LX OUTPUT DRIVER</b>						
f <sub>osc</sub>	LX Switching Frequency with Internal Oscillator		0.9	1	1.1	MHz
f <sub>sync</sub>	LX Switching Frequency when Externally Synchronized at NSYNC			f (NSYNC)		-
ton-min	Minimum On-Time	FB1 = 0V, I(LX) > I <sub>lim</sub> (LX)		60		ns
toff-min	Minimum Off-time (≥ Maximum Duty Cycle)	FB1 = 0V, I(LX) < I <sub>lim</sub> (LX)		60		ns
R <sub>on</sub>	LX On-Resistance	I(LX) = 100mA		0.4		Ω
I <sub>leak</sub>	LX Leakage Current	NEN = VDD, V(LX) = 30V		1	5	μA
I <sub>peak</sub>	LX Peak Current Limit	t > 8.32ms (end of soft-start)		1200		mA
<b>SCHOTTKY DIODE – LX, V<sub>OUT</sub></b>						
V <sub>diode</sub>	Forward Voltage from LX to V <sub>OUT</sub>	I = 10mA, T <sub>A</sub> = +25°C	0.4	0.5	0.6	V
		I = 10mA, T <sub>A</sub> = -40°C to +85°C	0.3	0.5	0.7	V
<b>FEEDBACK INPUTS AND SELECTION – FB0, FB1, SEL</b>						
V <sub>refFB0</sub>	Input Reference Voltage on FB0	SEL = GND, T <sub>A</sub> = +25°C	1.13	1.15	1.17	V
		SEL = GND, T <sub>A</sub> = -40°C to +85°C	1.12	1.15	1.18	V
V <sub>refFB1</sub>	Input Reference Voltage on FB1	SEL = VDD, T <sub>A</sub> = +25°C	1.135	1.15	1.165	V
		SEL = GND, T <sub>A</sub> = -40°C to +85°C	1.125	1.15	1.175	V
I <sub>FB0</sub>	Input Current in FB0	SEL = GND, FB0 = 1.3V	-0.2		0.2	μA
I <sub>FB1</sub>	Input Current in FB1	SEL = VDD, FB1 = 1.3V	-0.2		0.2	μA

**Electrical Specifications** VDD = 3.6V, GND = NEN = 0V, SEL = NSYNC = VDD, R1 = 390k, R2 = 39k, R3 = 26.1k,  
L = 10 $\mu$ H, T<sub>A</sub> = -40°C to +85°C unless otherwise stated **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
R <sub>FB0</sub>	FB0 Pull-Down Switch Resistance	SEL = VDD, I <sub>FB0</sub> = 10mA		15	25	$\Omega$
R <sub>FB1</sub>	FB1 Pull-Down Switch Resistance	SEL = GND, I <sub>FB1</sub> = 10mA		15	25	$\Omega$
<b>SYNCHRONIZATION INPUT – NSYNC</b>						
f <sub>NSYNC</sub>	External Sync. Frequency Range		600		1400	kHz
t <sub>dNSYNC</sub>	NSYNC Falling Edge to LX Falling Edge Delay	f <sub>NSYNC</sub> = 600kHz		80	100	ns
<b>OVERVOLTAGE DETECTOR - V<sub>OUT</sub></b>						
V <sub>OUT</sub>	Overvoltage Threshold	FB1 = GND	31	35		V
<b>OVERCURRENT DETECTOR</b>						
I <sub>OCTVDDOUT</sub>	Overcurrent Threshold	t > 2.048ms, DC current		800		mA
<b>OVER-TEMPERATURE DETECTOR</b>						
t <sub>off</sub>	Shut-Down Temperature Threshold	T rising		135		°C
t <sub>on</sub>	Turn-On Temperature Threshold	T falling		100		°C
<b>FAULT SWITCH – VDD, VDDOUT</b>						
R <sub>onFS</sub>	On-Resistance from VDD to VDDOUT	I <sub>O</sub> = 50mA, t > 2.048ms		0.2		$\Omega$
I <sub>leakVDDOUT</sub>	Leakage Current	VDDOUT = 0V		0.01	3	$\mu$ A
I <sub>SS_VDDOUT</sub>	Soft Inrush Current Source at VDDOUT	VDD-VDDOUT = 0.5V, t <sub>on</sub> < 2.048ms		50		mA
<b>REGULATION</b>						
ACC	Output Voltage Accuracy, Assuming Resistor Divider Tolerances of 0.1% or Better	I <sub>O</sub> = 10mA, T <sub>A</sub> = +25°C	-1.5		1.5	%
		I <sub>O</sub> = 10mA, T <sub>A</sub> = -40°C to +85°C	-2.5		2.5	%
$\Delta V_{OUT}/\Delta I_{O}$	Load Regulation	I <sub>O</sub> = 0mA to 50mA		0.05		%
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	VDD = 3.6V to 2.6V, I <sub>O</sub> = 30mA		0.1		%/V

Typical Performance Curves

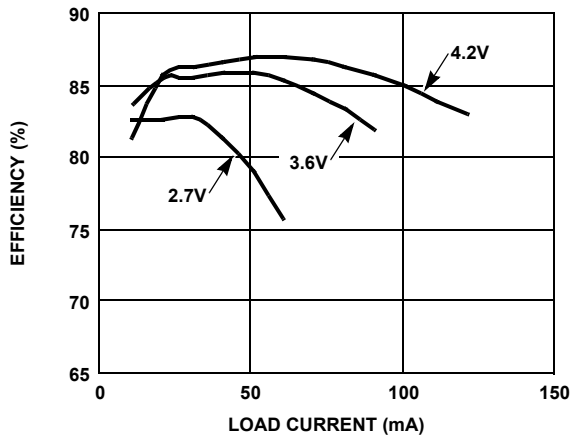


FIGURE 2. EFFICIENCY vs LOAD CURRENT ( $V_{OUT} = 18.3V$ )  
 $L = 10\mu H$  (CDRH4D28C-100NC)  $C = 6.6\mu F$

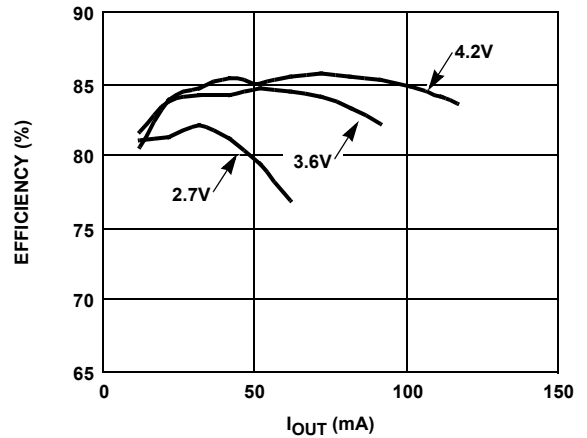


FIGURE 3. EFFICIENCY vs  $I_{OUT}$  ( $V_{OUT} = 18.3V$ )  
 $L = 6.8\mu H$  (TDK RLF7030)  $C = 6.6\mu F$

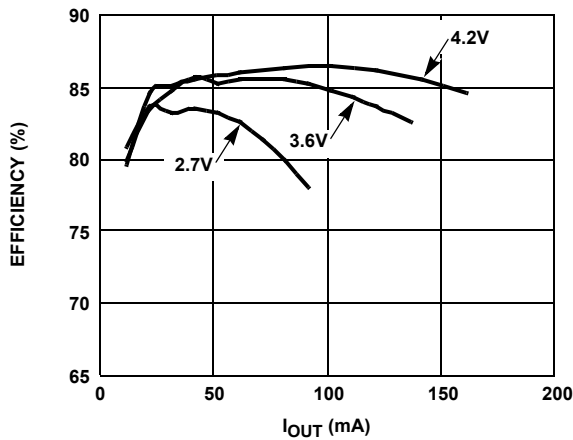


FIGURE 4. EFFICIENCY vs  $I_{OUT}$  ( $V_{OUT} = 12.6V$ )  
 $L = 6.8\mu H$  (TDK RLF7030)  $C = 6.6\mu F$

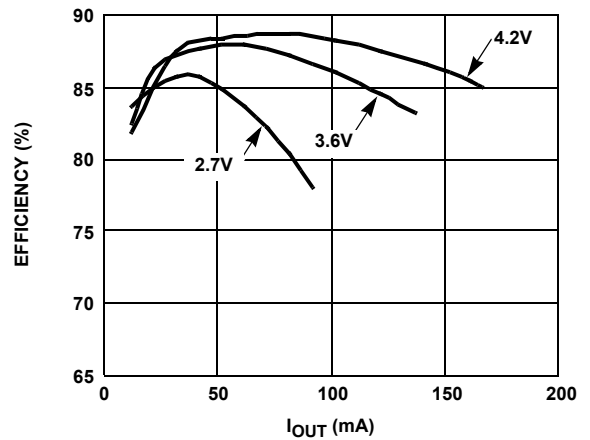


FIGURE 5. EFFICIENCY vs  $I_{OUT}$  ( $V_{OUT} = 12.7V$ )  
 $L = 10\mu H$  (CDRH4D28C-100NC)  $C = 6.6\mu F$

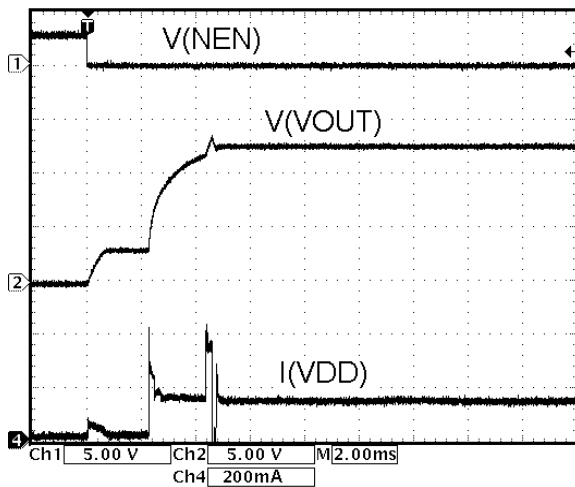


FIGURE 6. START-UP TO 12V @ SEL = 0  
 $(V_{DD} = 3.6V, R_L = 360\Omega)$

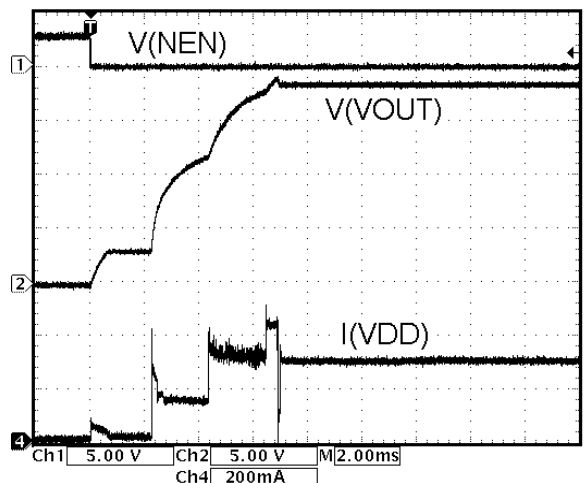


FIGURE 7. START-UP TO 18V @ SEL = 1  
 $(V_{DD} = 3.6V, R_L = 360\Omega)$

Typical Performance Curves (Continued)

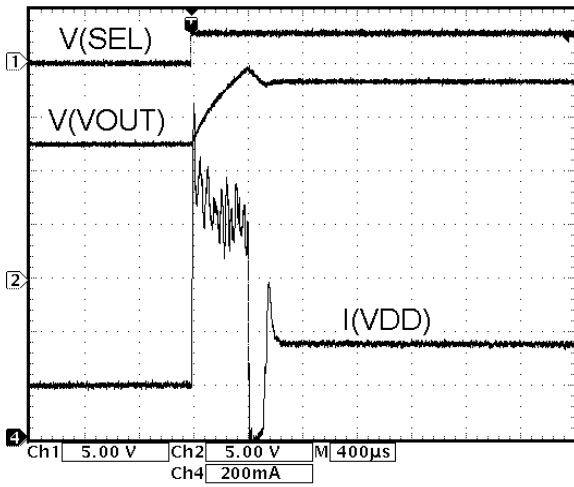


FIGURE 8. 12V->18V TRANSITION ( $V_{DD} = 3.6V$ ,  $R_L = 360\Omega$ )

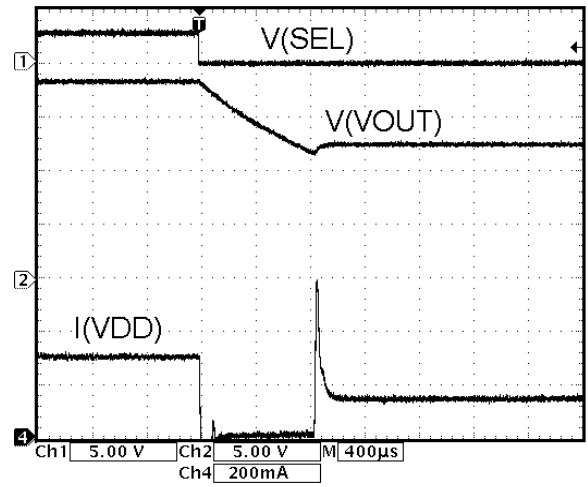


FIGURE 9. 18V->12V TRANSITION ( $V_{DD} = 3.6V$ ,  $R_L = 360\Omega$ )

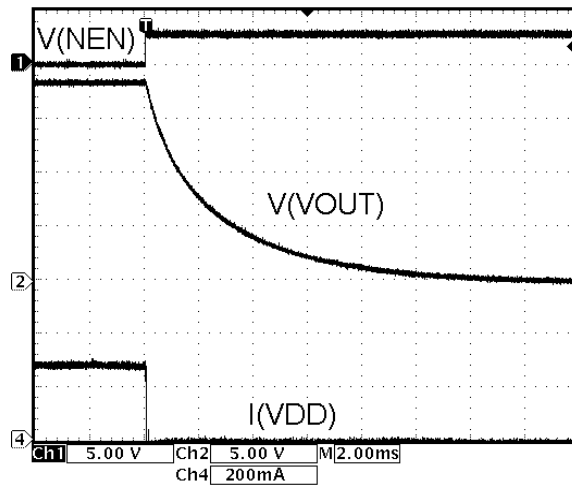


FIGURE 10. SHUT DOWN @ SEL = 1 ( $V_{DD} = 3.6V$ ,  $R_L = 360\Omega$ )

**Typical Performance Curves** (Continued)

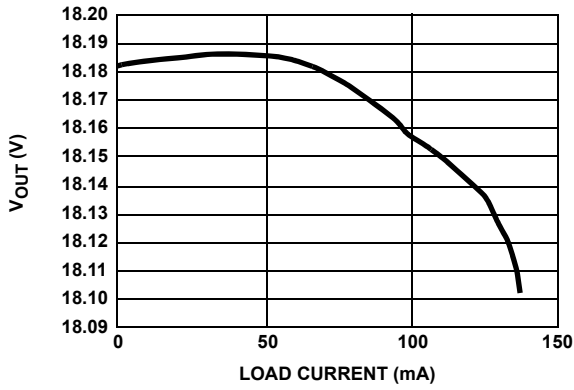


FIGURE 11. LOAD REGULATION (V<sub>IN</sub> = 3.6V)

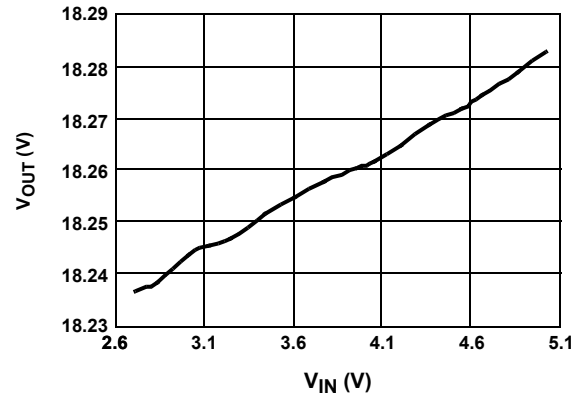


FIGURE 12. LINE REGULATION (I<sub>OUT</sub> = 30mA)

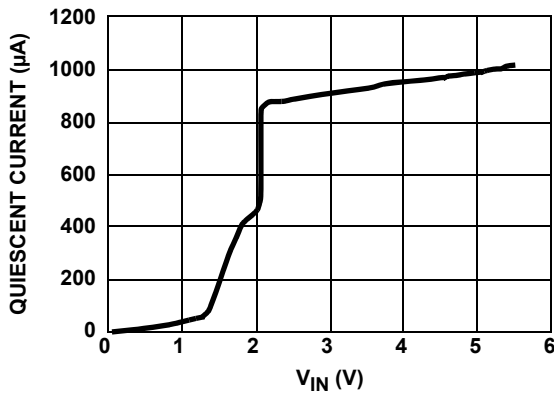
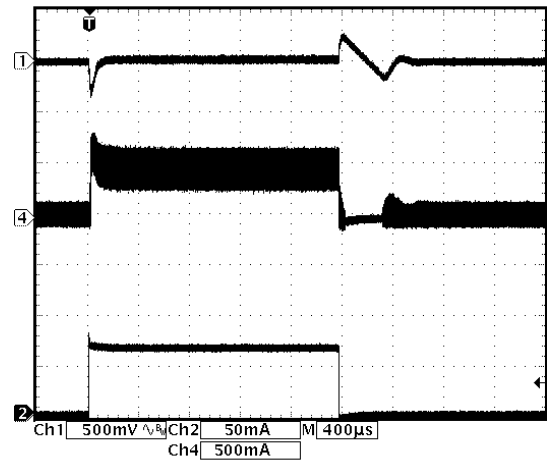


FIGURE 13. QUIESCENT CURRENT vs V<sub>IN</sub>



(CH1 = V<sub>OUT</sub>; CH4 = i<sub>L</sub>; CH2 = I<sub>OUT</sub>)

FIGURE 14. TRANSIENT RESPONSE (V<sub>IN</sub> = 3.3V; V<sub>OUT</sub> = 18.3V; STEP LOAD CURRENT FROM 2.6mA TO 70mA)

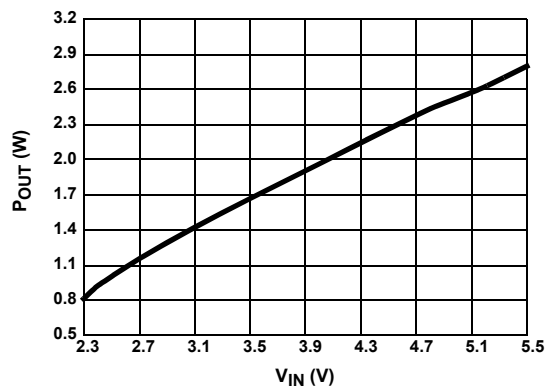


FIGURE 15. RECOMMENDED MAXIMUM OUTPUT POWER vs INPUT VOLTAGE

## Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	GND	Ground
2	VDDOUT	Protection Switch Output
3	VDD	Supply Input
4	NSYNC	Synchronization Input (Falling Edge)
5	FB0	Feedback Input 0
6	FB1	Feedback Input 1
7	SEL	Select Input
8	NEN	Enable Input (Active Low)
9	V <sub>OUT</sub>	Boost Output Voltage
10	LX	Boost FET

## Function Overview

The ISL97702 is a high frequency, high efficiency boost regulator which operates in constant frequency PWM mode. The boost converter generates a stable, higher output voltage from a variable, low voltage input source (e.g. Li-Ion battery). Two output voltage levels are pin selectable with values defined from the feedback resistor network.

The switching frequency is either generated from the fixed 1MHz internal oscillator or provided externally at the synchronization pin in the range from 600kHz to 1.4MHz. The compensation network and soft-start functions are built in with fixed parameters without any need for further external components.

To stop battery discharge into the output load when disabled the inductor is disconnected from the input supply with a low on resistance power switch.

Built in fault protection monitors inductor current and output voltage as well as junction temperature in order to interrupt the high current circuit path through the inductor and diode in the event of a load failure.

Low logic input thresholds allow the ISL97702 to interface directly to micro controllers with lower supply voltage. Alternatively the internal pull-up resistors on all logic inputs provide level shifting when driven from open collector outputs.

## Description of Operation

### Enable Pin (active low) - NEN

If NEN is high the ISL97702 shuts down all its internal functions and deactivates its I/Os. Only the internal pull-up resistor at NEN remains active. If NEN is high the input disconnect switch between VDD and VDDOUT interrupts the circuit path from the input voltage VDD through inductor and diode to the output load at V<sub>OUT</sub>. If shut down the total supply current in VDD is typically less than 0.1µA.

When NEN is driven low the ISL97702 begins with the start-up sequence.

### Start-Up Sequence

After pin NEN is pulled low or a restart is triggered from Fault Control during operation, the ISL97702 goes through a start-up sequence with the following six states: *Soft Inrush* -> *VDDOUT Enable* -> *Soft Boost 25* -> *Soft Boost 50* -> *Soft Boost 75* -> *Normal*.

If the sequence has completed, the ISL97702 stays in the "Normal" state until NEN is high again or any fault is detected.

### Soft Inrush: State Duration ~2.048ms

The switch at VDDOUT is configured as current source and provides a limited current through the inductor to pre-charge the capacitor at V<sub>OUT</sub>.

### VDDOUT Enable: State Duration ~128µs

The switch at VDDOUT is fully enabled and connects the inductor to VDD with a low on-resistance.

### Soft Boost 25 -> 50 -> 75: State Duration 3x ~2.048ms

The boost regulator begins to switch at LX.

The LX current limit increases in three steps representing 25%, 50% 75% of its final value.

### Normal

If no fault was detected Normal state is entered ~8.256ms after NEN is pulled low.

The LX current limit steps up to 100%.

In all states Fault Control can force the sequence to restart or even to shut down (see Table 1).



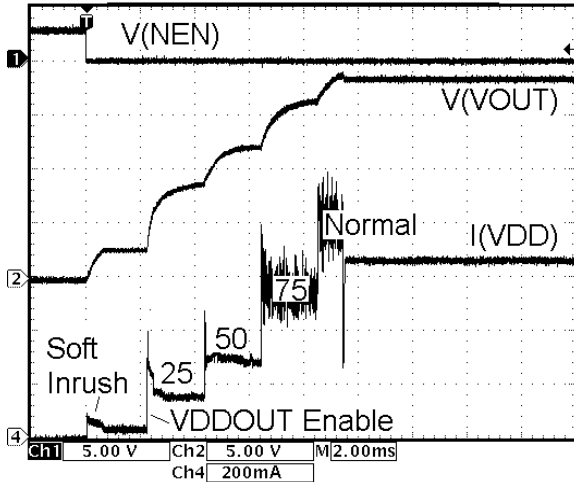


FIGURE 16.

**Fault Control**

The input voltage at VDD, current in the VDDOUT switch, voltage at V<sub>OUT</sub> and junction temperature T<sub>j</sub> are continuously monitored and can either restart the start-up sequence or in some cases disable the ISL97702 boost function as long as the fault is present.

TABLE 1. FAULT PROTECTION

FAULT DESCRIPTION	FAULT CONDITION	ISL97702 FAULT REACTION
Undervoltage at VDD	V(VDD) < V(VDD) <sub>off</sub>	Disables I/Os and waits until V(VDD) reaches V(VDD) <sub>on</sub> to begin with the start-up sequence
Overcurrent drawn from VDDOUT	I(VDDOUT) > I <sub>t</sub> (VDDOUT) <sub>err</sub>	Disables VDDOUT switch and LX driver and immediately restarts the start-up sequence
Overvoltage at VOUT	V(VOUT) > V <sub>t</sub> (VOUT) <sub>err</sub>	Disables VDDOUT switch and LX driver and waits until output voltage V(VOUT) drops to V <sub>t</sub> (VOUT) to restart the start-up sequence
Over Temperature on chip	T <sub>j</sub> > T <sub>off</sub>	Disables VDDOUT switch and LX driver and waits until junction temp drops to “Ton” to restart the start-up sequence

**Maximum Duty Cycle – LX**

The maximum duty cycle D<sub>max</sub>, at which the power FET can operate defines the upper limit of the regulator output to input voltage ratio according to the formula: V<sub>OUT</sub>/V<sub>IN</sub> = 1/(1-D<sub>max</sub>). In the ISL97702, D<sub>max</sub> is defined from the minimum off-time toff(LX)<sub>min</sub> and the switching frequency.

If NSYNC is tied to VDD the internal oscillator defines D<sub>max</sub> to:

$$D_{max}(f_{osc}) = 1 - toff(LX)_{min} * f_{osc}$$

With external synchronization at pin NSYNC

$$D_{max}(NSYNC) = 1 - toff(LX)_{min} * f(NSYNC)$$

The duty cycle at LX can be 0% (**pulse skipping**), if the output voltage exceeds the target voltage set with the feedback resistors.

**Internal Schottky Diode – LX, V<sub>OUT</sub>**

The inductor node LX internally connects to the power FET and to the anode of the integrated power Schottky diode. The cathode of the diode is pin V<sub>OUT</sub>. An overvoltage detector at V<sub>OUT</sub> continuously monitors the cathode voltage and immediately disables the boost regulator if the voltage exceeds the maximum allowable voltage.

**Feedback Input Pins – FB0, FB1**

Each feedback pin is either configured as feedback input pin or as ground reference output pin for the external feedback resistor chain. Configured as output the feedback pin is switched to the internal reference ground via a low Ron MOS transistor to achieve maximum accuracy of the regulated output voltage. A current limit at FB0 and FB1 prevents overloading in a fault condition.

TABLE 2. PIN FEEDBACK CONFIGURATION DEPENDENT ON SEL

SEL	FB0	FB1
0	Feedback Input	Ground Reference Output
1	Ground Reference Output	Feedback Input

**External Synchronization Pin - NSYNC**

Pin NSYNC can be used to synchronize the LX output pin with an external clock signal in the range from 600kHz to 1.4MHz.

A frequency detector monitoring NSYNC enables external synchronization if f(NSYNC) is higher than about 300kHz. If the pin is e.g. static high the internal oscillator defines the LX output frequency and phase. When externally synchronized all falling edges at LX are timed from the falling edge of the clock signal applied at NSYNC. The timing of the rising edge at LX is defined by the boost controller.

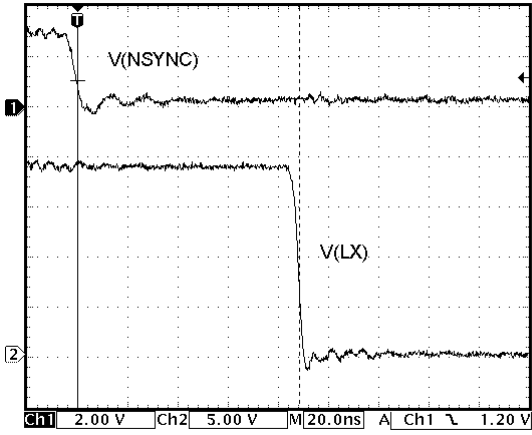


FIGURE 17. NSYNC TO LX SYNCHRONIZATION DELAY

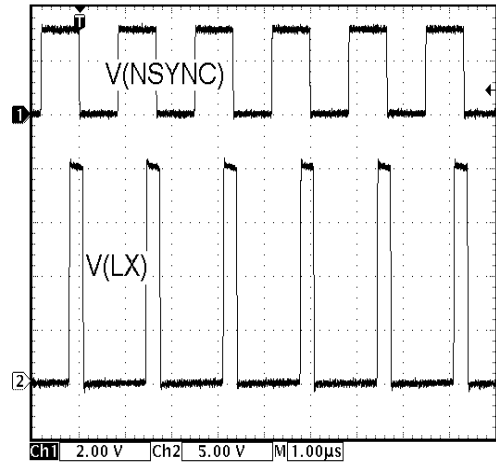


FIGURE 18. LX SYNCHRONIZATION WITH  $f(\text{SYNC}) = 600\text{kHz}$

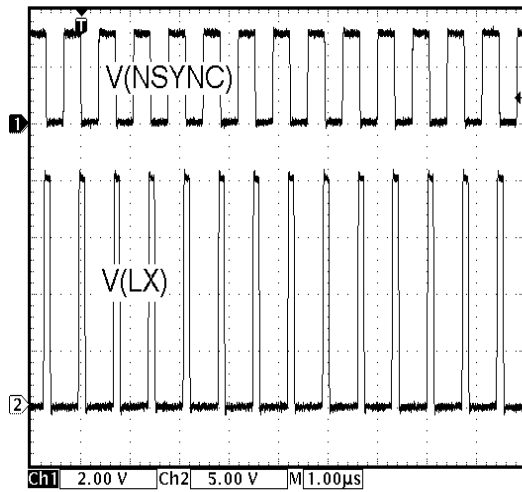


FIGURE 19. LX SYNCHRONIZATION WITH  $f(\text{SYNC}) = 1.4\text{MHz}$

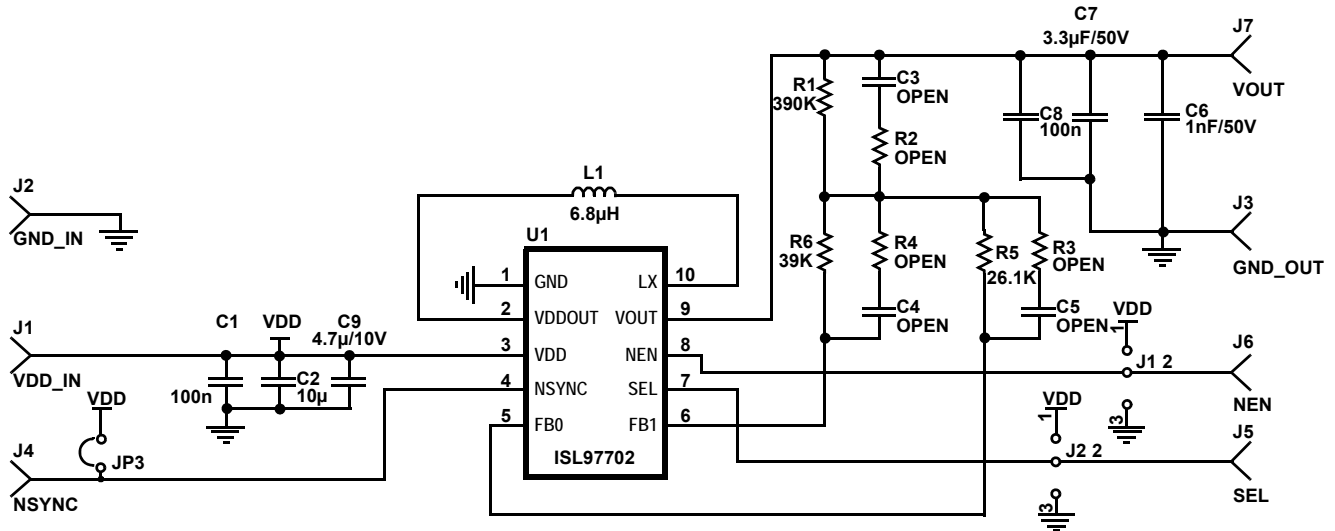


FIGURE 20. ISL97702 APPLICATION BOARD

**Typical Application**

Typical applications are passive- or active-matrix organic light emitting diode displays (PMOLED, AMOLED) in handheld devices. Applications with low power or screen saver/ reduced brightness modes are also directly supported.

Motivation: In the low power mode the OLED display brightness (~pixel current) is reduced so that the display drivers can operate with equally reduced power. Usually the supply voltage is kept at the same level, although the pixel voltage drops by several volts when the pixel current levels are reduced. Here a further power reduction can be achieved if the supply voltage for the display drivers is reduced according to the pixel diode characteristic.

The ISL97702 allows selection between a nominal and a reduced output voltage level in order to supply more effectively OLED display drivers.

**Components Selection**

The input capacitance is normally 10µf~15µF and the output capacitor is 3.3µf to 6.6µF. X5R or X7R type of ceramic capacitor with correct voltage rating is recommended. The output capacitor value will affect the output voltage ripple. Higher value of the output capacitor, lower ripple of the output voltage.

When choosing an inductor, make sure the inductor can handle the average and peak currents given by following formulas (80% efficiency assumed):

$$I_{LAVG} = \frac{I_{OUT} \cdot V_{OUT}}{0.8 \cdot V_{IN}} \tag{EQ. 1}$$

$$I_{LPK} = I_{LAVG} + \frac{1}{2} \cdot \Delta I_L \tag{EQ. 2}$$

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{L \cdot V_{OUT} \cdot f_{OSC}} \tag{EQ. 3}$$

Where:

- ΔI<sub>L</sub> is the peak-to-peak inductor current ripple in Amperes
- L inductance in H
- f<sub>OSC</sub> switching frequency, typically 1.0MHz

Optimal combination of the boost inductor L and the output capacitor Cout are listed in table:

INDUCTOR (µH)	CAPACITOR (µF)	
	MIN	MAX
4.7	2.2	10
6.8	3.3	10
10	4.7	10
15	6.8	10

Recommended Inductor and Ceramic capacitor manufactures are listed in the following table:

INDUCTOR	CERAMIC CAPACITOR
Sumida: <a href="http://www.sumida.com">www.sumida.com</a>	Taiyo Yuden: <a href="http://www.t-yuden.com">www.t-yuden.com</a>
TDK: <a href="http://www.tdk.co.jp">www.tdk.co.jp</a>	AVX: <a href="http://www.avxcorp.com">www.avxcorp.com</a>
Toko: <a href="http://www.tokoam.com">www.tokoam.com</a>	Murata: <a href="http://www.murata.com">www.murata.com</a>

**PCB layout Considerations**

The layout is very important for the converter to function properly. To ensure the high pulse current in the power ground does not interfere with the sensitive feedback signals, the current loops (V<sub>IN</sub>-L1-LX-GND, and V<sub>IN</sub>-L1-V<sub>OUT</sub>-C<sub>OUT</sub>-GND) should be as short as possible. For the DFN package, there is

no separated GND. All return GNDs should be connected in GND pin but with no sharing branch.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad

is preferable. In addition, a solid ground plane is helpful for the EMI performance.

The demo board is a good example layout based on the principle. The overview, top layer and bottom layer of the demo board layout are shown in Figures 21, 22 and 23.

**Demo Board Layout**

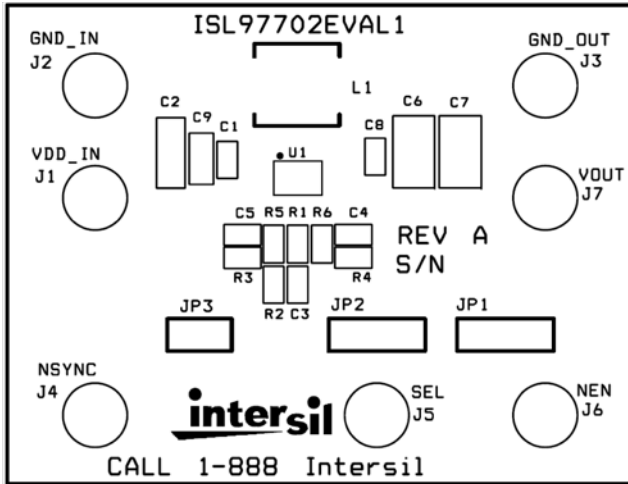


FIGURE 21. OVERVIEW of DEMO BOARD

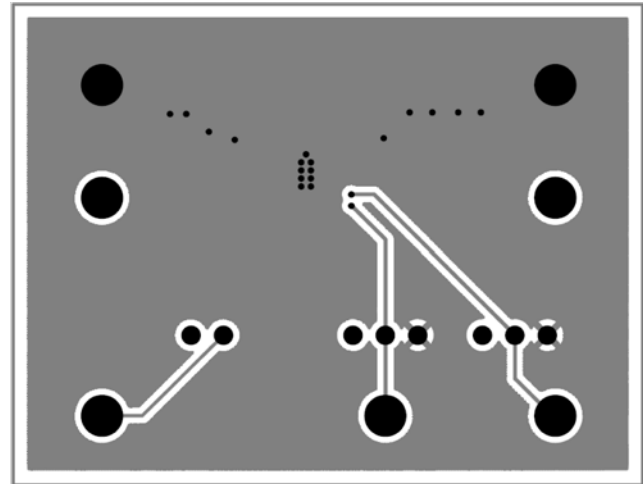


FIGURE 22. BOTTOM LAYER of the DEMO BOARD

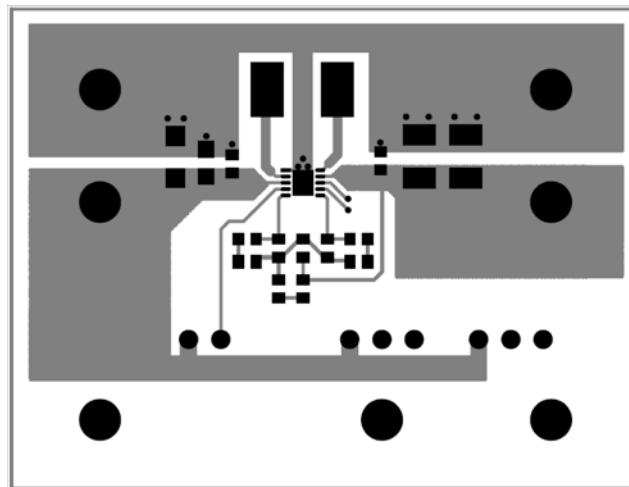


FIGURE 23. TOP LAYER of the DEMO BOARD

© Copyright Intersil Americas LLC 2005. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

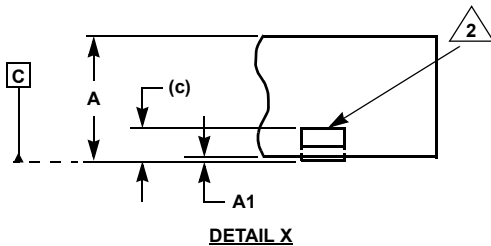
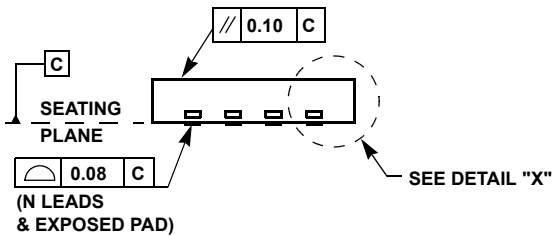
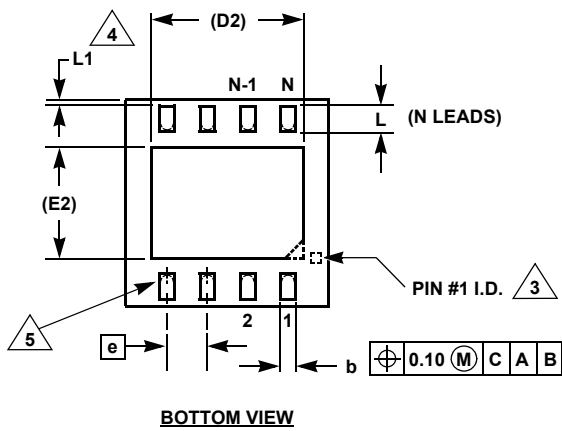
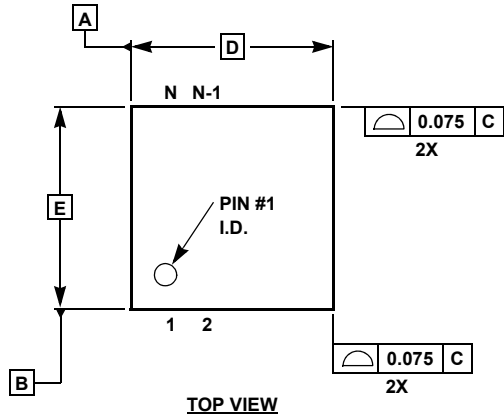
For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

**Dual Flat No-Lead Package Family (DFN)**



**MDP0047**

DUAL FLAT NO-LEAD PACKAGE FAMILY (JEDEC REG: MO-229)

SYMBOL	DFN8	DFN10	TOLERANCE
A	0.85	0.90	±0.10
A1	0.02	0.02	+0.03/-0.02
b	0.30	0.25	±0.05
c	0.20	0.20	Reference
D	4.00	3.00	Basic
D2	3.00	2.25	Reference
E	4.00	3.00	Basic
E2	2.20	1.50	Reference
e	0.80	0.50	Basic
L	0.50	0.50	±0.10
L1	0.10	0	Maximum

Rev. 1 10/03

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Exposed lead at side of package is a non-functional feature.
3. Bottom-side pin #1 I.D. may be a diepad chamfer, an extended tiebar tab, or a small square as shown.
4. Exposed leads may extend to the edge of the package or be pulled back. See dimension "L1".
5. Inward end of lead may be square or circular in shape with radius (b/2) as shown.
6. N is the total number of leads on the device.