

PCN Number:	20211111000.2	PCN Date:	Nov. 19, 2021
Title:	Qualify UMC12A for C021.A Process as alternate source		
Customer Contact:	PCN Manager	Dept:	Quality Services
Proposed 1st Ship Date:	May 19, 2022	Estimated Sample Availability:	Date provided at sample request
Change Type:	<input type="checkbox"/> Assembly Site <input type="checkbox"/> Assembly Process <input type="checkbox"/> Assembly Materials <input type="checkbox"/> Mechanical Specification <input type="checkbox"/> Packing/Shipping/Labeling		
	<input type="checkbox"/> Design <input type="checkbox"/> Data Sheet <input type="checkbox"/> Part number change <input type="checkbox"/> Test Site <input type="checkbox"/> Test Process		
	<input type="checkbox"/> Wafer Bump Site <input type="checkbox"/> Wafer Bump Material <input type="checkbox"/> Wafer Bump Process <input checked="" type="checkbox"/> Wafer Fab Site <input checked="" type="checkbox"/> Wafer Fab Materials <input type="checkbox"/> Wafer Fab Process		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of Wafer Fab site UMC12A in the C021.A process as an alternate source.

Current Fab Site			Alternate Fab Site		
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter
DMOS6	C021.A	300 mm	UMC12A	C021.A	300 mm

Process Difference Summary

Description	Current Wafer Fab	Alternate Wafer Fab
Wafer Fab site	DMOS6	UMC12A
Dielectric Material	LK SiOC/TEOS (k value = 3.1)	LK SiOC (k value = 3.1)
Top Protective Layer or Passivation Layer Material	PO Oxide (TEOS/SiON)	TEOS/SiN

Reason for Change:

Continuity of Supply.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None.

Changes to product identification resulting from this PCN:

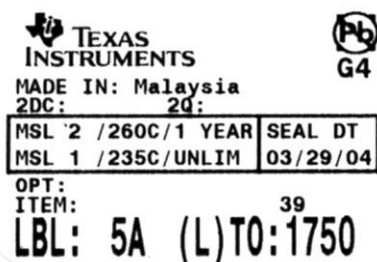
Current:

Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DMOS6	DM6	USA	Dallas

New Fab Site:

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
UMC12A	F12	TWN	Tainan

Sample Product Shipping Label (not actual product label)



(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T) LOT: 3959047MLA
(4W) TKY (1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CSO: SHE (21L) CCO: USA
(22L) ASO: MLA (23L) ACO: MYS

Product Affected:

DP83TC811RWRNDRQ1
 DP83TC811RWRNDTQ1
 DP83TC811SWRNDRQ1
 DP83TC811SWRNDRQ1

Automotive New Product Qualification Summary

(As per AEC-Q100 and JEDEC Guidelines)

Approved 27-October-2021**Product Attributes**

Attributes	Qual Device: DP83TC811RWRNDRQ1	QBS Process Reference: DS90UB964TRGCRQ1	QBS Product Reference: PDP83TC811RWRNDRQ1	QBS Package Reference: DS90UB960WRTD	QBS Package Reference: DS90UH949TRGCRQ1
Automotive Grade Level	Grade 1	Grade 2	Grade 1	Grade 2	Grade 2
Operating Temp Range	-40 to +125 C	-40 to +105 C	-40 to +125 C	-40 to +105 C	-40 to +105 C
Wafer Fab Supplier	UMC12A	UMC12A	DMOS6	DMOS6	DMOS6
Die Revision	A1	A1	A0	A0	A
Assembly Site	AP1	CLARK AT	AP1	AP1	CLARK AT
Package Type	VQFN	VQFN	VQFN	VQFN	VQFN
Package Designator	RND	RGC	RND	RTD	RGC
Ball/Lead Count	36	64	36	64	64

- QBS: Qual By Similarity

- Qual Devices qualified at LEVEL3-260C: DS90UB934TRGZRQ1

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name / Condition	Duration	Qual Device: DP83TC811RW RNDRQ1	QBS Process Reference: DS90UB964TRGCRQ1	QBS Product Reference: PDP83TC811RWR NDRQ1	QBS Package Reference: DS90UB960WRTD	QBS Package Reference: DS90UH949 TRGCRQ1
Test Group A – Accelerated Environment Stress Tests											
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 3-260C	-	3/Pass	3/1058/0	2/Pass	1/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 110C/85%RH	528 Hours	-	3/231/0	-	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	-	3/231/0	2/154/0	1/77/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	192 Hours	-	-	-	2/154/0	1/77/0
AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	192 Hours	-	-	3/231/0	2/154/0	1/77/0
UHAST	A3	JEDEC JESD22-A118	3	77	Unbiased HAST, 110C/85%RH	264 Hours	-	3/231/0	-	-	-
UHAST	A3	JEDEC JESD22-A118	3	77	Unbiased HAST, 130C/85%RH	96 Hours	-	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	-	3/231/0	3/231/0	2/154/0	1/77/0

TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	1000 Cycles	-	3/219/0	-	2/154/0	1/77/0
TC-BP	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Post Temp. Cycle, Bond Pull	Wires	-	1/30/0	3/15/0	1/3/0	-
PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	NA	N/A	NA	NA
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 150C	500 Hours	-	-	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 150C	1000 Hours	-	1/45/0	-	2/90/0	1/45/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 175C	1000 Hours	-	-	3/231/0		
Test Group B – Accelerated Lifetime Simulation Tests											
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125	1000 Hours	1/77/0	3/231/0	3/231/0	3/231/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	24 Hours	-	3/2400/0	-	-	-
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	--	N/A	N/A	N/A	N/A	N/A
Test Group C – Package Assembly Integrity Tests											
WBS	C1	AEC Q100-001	1	30	Bond Shear (Cpk>1.67)	Wires	1/30/0	1/30/0	3/30/0	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0	1/30/0	3/30/0	3/90/0	-
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	8 Hours Steam Age	-	-	3/90/0	3/90/0	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	--	-	3/90/0	3/30/0	3/90/0	-
Test Group D – Die Fabrication Reliability Tests											
EM	D1	JESD61	-	-	Electromigration	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	--	Completed Per Process	Completed Per Process Technology	Completed Per Process Technology	Completed Per Process Technology	Completed Per Process

							Technology Requirements	Requirements	Requirements	Requirements	Technology Requirements	
Test Group E – Electrical Verification Tests												
	HBM	E 2	AEC Q100-002	1	3	ESD - HBM	2000 V	1/3/0	1/3/0	1/3/0	-	-
	CDM	E 3	AEC Q100-011	1	3	ESD - CDM	1000 V	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
	LU	E 4	AEC Q100-004	1	6	Latch-up	(Per AEC Q100-004)	1/6/0	1/6/0	1/6/0	1/6/0	1/6/0
	ED	E 5	AEC Q100-009	3	30	Auto Electrical Distributions	Cpk>1.67	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0

A1 (PC): Preconditioning:

Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I): -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

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