A8522

Wide Input Voltage, Fault Tolerant, Independently Controlled Multi-Channel LED Driver with I²C Interface

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Wide input voltage range of 4.5 to 36 V
- Operates down to 3.9 V (V_{IN} falling) for idle stop, and up to 40 V for load dump
- Integrated boost converter with DMOS switch and OVP protection up to 39 V
- 8 fully integrated LED current sinks, with individually programmable current up to 60 mA per channel
- I²C™ interface for programming LED current, PWM dimming, and various protection thresholds per channel
- Ability to drive multiple loads from a single IC
- Extensive PWM dimming (up to 10,000:1 at 100 Hz), individually programmable for each channel
- Extensive diagnostics and fault reporting
- Thermal warning and derating of LED current at higher temperatures

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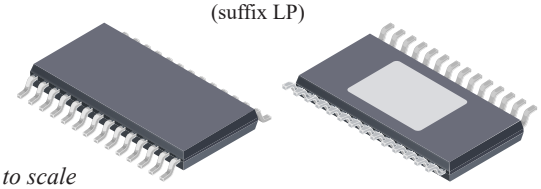
PACKAGE:

28-pin TSSOP with exposed thermal pad
(suffix LP)



Not to scale

DESCRIPTION

The A8522 is a programmable multi-output LED driver for LCD backlighting. It integrates a current-mode boost converter with internal power switch and 8 current sinks. The IC operates from 4.5 to 36 V, and is able to withstand up to 40 V load-dump conditions encountered in automotive systems.

The control loop is optimized to eliminate night flash in display backlight applications.

The I²C interface allows the user to set the LED currents individually, up to 60 mA per LED channel. Adjacent channels may be combined to drive higher-current LED strings. The PWM dimming duty cycle also is independently controlled for each LED channel. This flexibility makes the A8522 a single solution for a wide range of LED applications. Two-way communication allows fault status to be reported.

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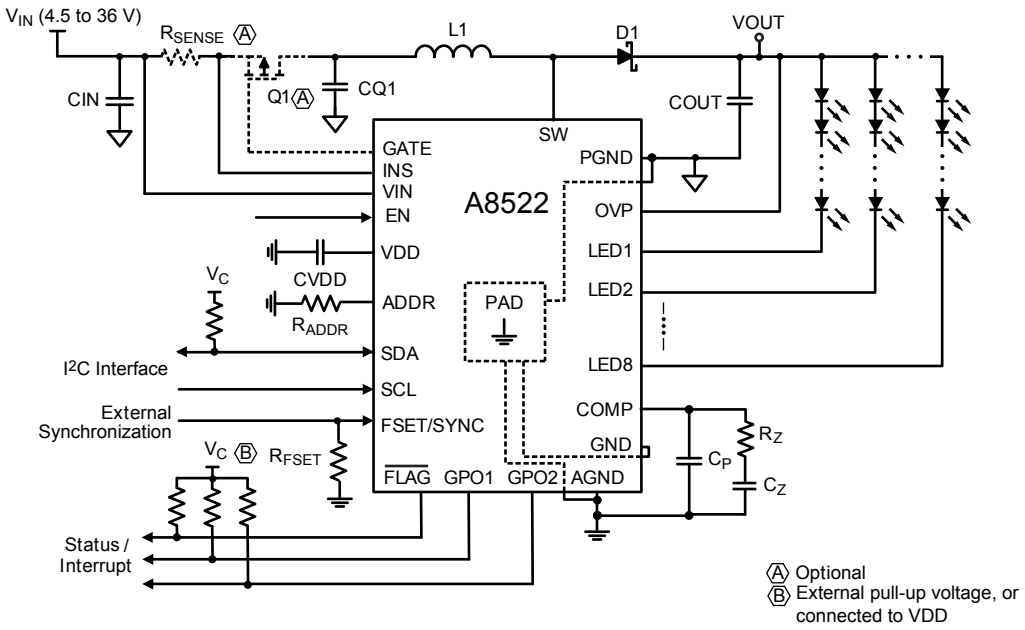
APPLICATIONS:

Automotive:

- Infotainment
- Cluster
- Center-stack lighting
- Head-up display (HUD)
- Daytime running lights (DRL)



Typical Application Drawing

FEATURES AND BENEFITS (continued)

- Buffered PWM dimming control for all channels to facilitate localized dimming applications
- Polyphase PWM dimming: LED currents staggered to reduce light flickering and input ripple current
- Synchronize boost switching frequency: 400 kHz to 2.3 MHz to allow operation below or above the AM band
- Programmable frequency dithering to reduce EMI
- Typical LED current accuracy of 0.7%, and LED-to-LED matching accuracy of 0.8%
- Protection features
  - □ Open/shorted LED pin detection
  - □ Programmable LED string short detection
  - □ Open/shorted external components (including boost inductor, Schottky diode, FSET resistor and so forth)
  - □ Input overcurrent protection against output to GND short
  - □ Cycle-by-cycle switch current limit
  - □ Overtemperature, and output overvoltage and undervoltage protection

DESCRIPTION (continued)

PWM dimming duty cycle also is independently controlled for each LED channel. This flexibility makes the A8522 a single solution for a wide range of LED applications, in some cases offering the ability to replace two or more LED driver ICs with a single device.

The A8522 detects and protects against a wide variety of fault conditions, and two-way communication allows fault status to be reported. It provides protection against output short and overvoltage, open or shorted diode, open or shorted LED pin, shorted boost switch or inductor, and IC overtemperature. A dual cycle-by-cycle current limit protects the internal switch against switch overcurrent. If required, the IC can drive an external PFET as an input-disconnect switch that is triggered by integrated current sense.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A (°C)	Package	Packing [1]	Leadframe Plating
A8522KLPTR-T	–40 to 125	28-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel	100% matte tin

[1] Contact Allegro™ for additional packing options.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pins	V_{LEDx}		–0.3 to 42	V
$\overline{FLAG}$, GPO2, and OVP Pins			–0.3 to 42	V
EN, VIN, INS, and GATE Pins		INS and GATE pins should not exceed V_{IN} by more than 0.4 V	–0.3 to 40	V
SW Pin	V_{SW}	Continuous	–0.6 to 42	V
		t < 50 ns	–1.0 to 46	V
VDD, FSET/SYNC, COMP, GPO1, SDA, SCL, and ADDR Pins			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–65 to 150	°C

[1] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W

[2] Additional thermal information available on the Allegro website.

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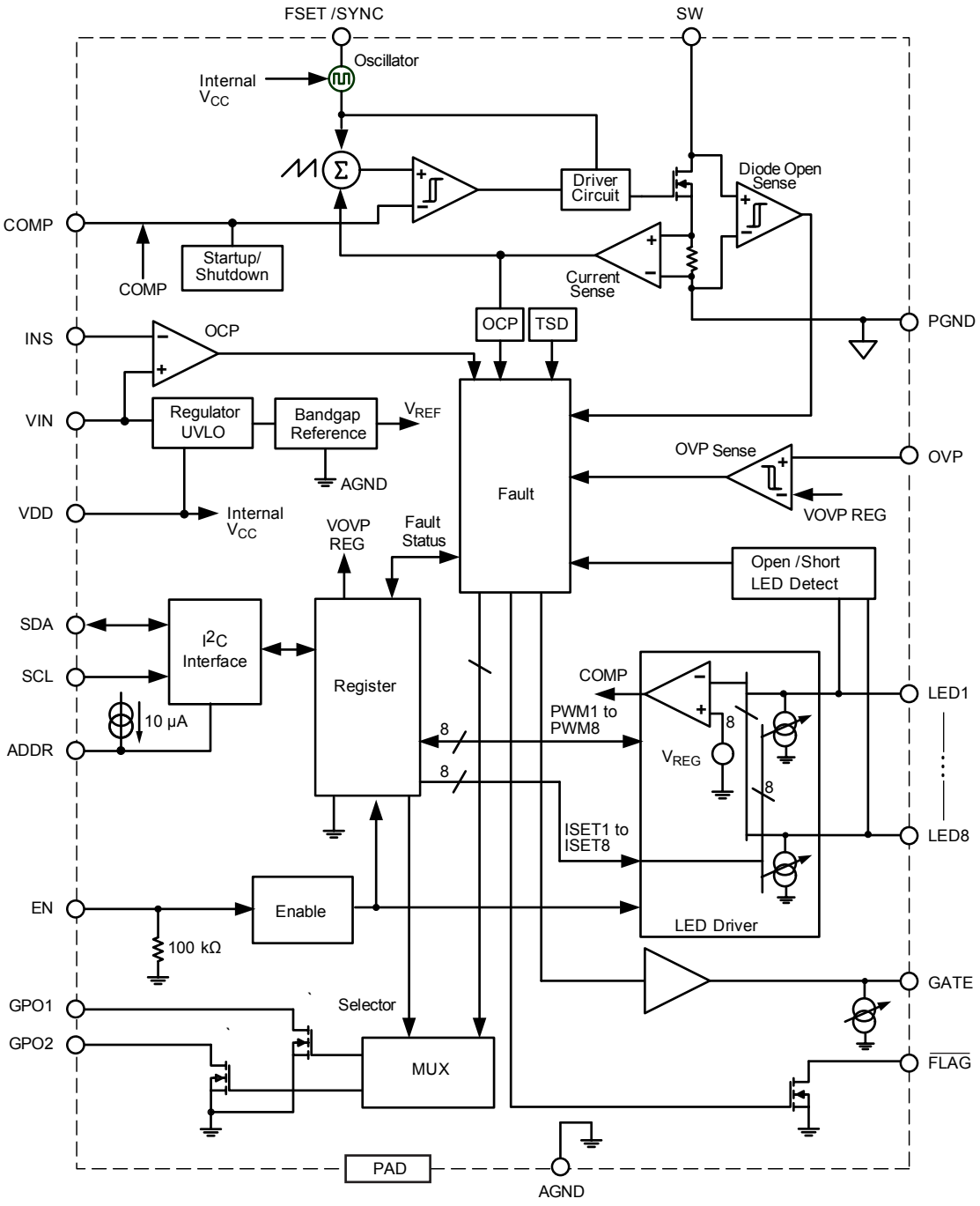

Functional Block Diagram

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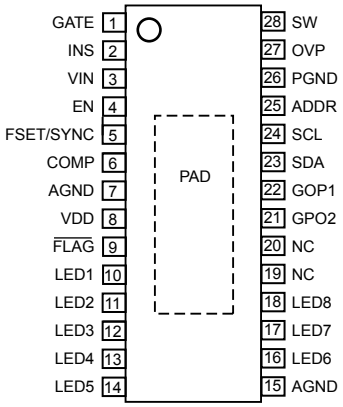

Package LP, 28-Pin TSSOP Pinout Diagram

Terminal List Table

Name	Number	Function
ADDR	25	This pin has 4 levels that allow the user to set up to 4 physical IC addresses based on the voltage level. Connect a resistor to GND to set the voltage level.
AGND	7, 15	Analog ground; connect all noise-sensitive components (especially for COMP) to this quiet ground, and connect to thermal pad.
COMP	6	Output of error amplifier and compensation node; connect a type-2 feedback network from this pin to AGND for control loop compensation.
EN	4	Enable for the A8522; IC stays in shutdown mode as long as EN = $V_{EN(L)}$, enables the part when connected to $V_{EN(H)}$ or to VIN.
$\overline{FLAG}$	9	This active-low, open-drain pin is used to indicate that system attention is required, such as during startup or a fault condition. Connect a resistor with a value from 10 to 100 kΩ between this pin and the target logic level voltage.
FSET/SYNC	5	Frequency/synchronization pin; a resistor, R_{FSET}, from this pin to GND sets the switching frequency, and this pin can also be used to synchronize to an external switching frequency.
GATE	1	Gate driver for optional external PMOS input disconnect switch, that in the event of a fault (such as output shorted to GND) is turned off by this pin being pulled high (turning off input supply); if not used, this pin should be left open.
GPO1	22	General purpose open-drain output 1, programmable by internal register.
GPO2	21	General purpose open-drain output 2, programmable by internal register.
INS	2	Input current sense, used together with VIN pin to detect input overcurrent fault; if not used, this pin should be tied to VIN.
LEDx	10, 11, 12, 13, 14, 16, 17, 18	LED current sink channels 1 through 8. Up to 60 mA per channel. Any unused LEDx pin should be connected to GND through a 4.7 kΩ resistor.
NC	19, 20	No connect. Terminate each pin to GND through a 4.7 kΩ resistor (do not short to GND directly). See page A-8 for important notes on initialization of register 0x00.
OVP	27	Connect this pin to output voltage V_{OUT} to provide output Overvoltage Protection (OVP) and Undervoltage Protection (UVP).
PAD	–	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad, and AGND and PGND pins must be connected to this ground pad on the PCB.
PGND	26	Power ground for internal NMOS switching device; connect this pin to ground terminal of output ceramic capacitor(s) and to thermal pad.
SCL	24	I²C clock signal.
SDA	23	I²C data signal.
SW	28	The drain of the internal NMOS switch of the boost converter.
VDD	8	Output of internal LDO; connect a 0.47 µF decoupling capacitor between this pin and AGND.
VIN	3	Input power to the A8522.

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ELECTRICAL CHARACTERISTICS [1]: Valid at V_{IN} = 16 V , T_A = 25°C, EN = $V_{EN(H)}$, • indicates specifications valid across the full operating temperature range with T_A = T_J = –40°C to 125°C and with typical specifications at T_A = 25°C; unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE							
Input Voltage Range	V_{IN}	Measured at the VIN pin	•	4.5	–	36	V
VIN Pin UVLO Start	$V_{INUV(ON)}$	V_{IN} rising	•	–	–	4.35	V
VIN Pin UVLO Stop	$V_{INUV(OFF)}$	V_{IN} falling	•	–	–	3.90	V
VIN Pin UVLO Hysteresis	$V_{INUV(HYS)}$			–	400	–	mV
INPUT CURRENT							
Input Quiescent Current	I_Q	Measured at the VIN pin, EN = $V_{EN(H)}$, f_{SW} = 2 MHz no load	•	–	15	–	mA
Input Sleep Supply Current	I_{QSLEEP}	Sum of VIN and INS pin currents, V_{IN} = V_{INS} = 16 V, V_{EN} = 0 V	•	–	3.5	10.0	µA
EN (ENABLE) PIN							
EN Input Logic Level - Low	$V_{EN(L)}$	4.5 V < V_{IN} < 36 V	•	–	–	0.4	V
EN Input Logic Level - High	$V_{EN(H)}$	4.5 V < V_{IN} < 36 V	•	1.5	–	–	V
EN Internal Pull-Down Resistance	R_{ENPD}			–	100	–	kΩ
Error Amplifier							
Source Current	$I_{EA(SRC)}$	V_{COMP} = 0.75 V, V_{LEDx} = 0.3 V		–	–200	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 0.75 V, V_{LEDx} = 1.5 V		–	+200	–	µA
COMP Pin Internal Pull-Down Resistance	R_{COMPPD}	During startup and shutdown		–	2000	–	Ω
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION							
Overvoltage Threshold	V_{OVPMIN}	OVP register = xxx0 0000	•	7.5	8	8.5	V
	V_{OVPMAX}	OVP register = xxx1 1111	•	38	39	40	V
Overvoltage Step Size	$V_{OVPSTEP}$			–	1.0	–	V
Undervoltage Threshold	V_{UVPMIN}	OVP register = xxx0 0000		–	0.49	–	V
	V_{UVPMAX}	OVP register = xxx1 1111		–	2.5	–	V
OVP Pin Input Impedance	R_{OVP}	V_{OVP} = 20 V, EN = $V_{EN(H)}$		–	800	–	kΩ
OVP Leakage Current	I_{OVPLKG}	V_{OVP} =16 V, EN = $V_{EN(L)}$	•	–	0.1	1	µA
Secondary Overvoltage Protection	$V_{OVP(sec)}$	Measured at SW pin		–	44	–	V
BOOST Switch							
Switch On-Resistance	$R_{DS(ON)}$	I_{SW} = 0.750 A, V_{IN} = 16 V		–	220	350	mΩ
Switch Leakage Current	I_{SWLKG}	V_{SW} = 16 V, EN = $V_{EN(L)}$, T_A = T_J = –40°C to 85°C		–	0.1	10	µA
		V_{SW} = 16 V, EN = $V_{EN(L)}$, T_A = T_J = 125°C		–	3	–	µA
Cycle-by-Cycle Switch Current Limit	$I_{SW(LIM)}$		•	3.6	4.2	4.8	A
Secondary Switch Current Limit [2]	$I_{SWLIM(sec)}$	Higher than maximum $I_{SW(LIM)}$ at any condition (A8522 latches when detected)	•	5.6	7.0	–	A
Minimum Switch On-Time	$t_{SWONTIME}$	R_{FSET} = 10 kΩ	•	–	85	120	ns
Minimum Switch Off-Time	$t_{SWOFFTIME}$	R_{FSET} = 10 kΩ	•	–	55	85	ns

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SWITCHING FREQUENCY							
Boost Stage Switching Frequency	f_{SW}	R_{FSET} = 10 kΩ	•	1.8	2	2.2	MHz
		R_{FSET} = 20.1 kΩ		–	1	–	MHz
		R_{FSET} = 40.6 kΩ		–	500	–	kHz
FSET/SYNC Pin Voltage	$V_{FSETSYNC}$	R_{FSET} = 10 kΩ		–	1.00	–	V
SYNCHRONIZATION							
Synchronized Boost Stage Switching Frequency	f_{SW_SYNC}		•	400	–	2300	kHz
Synchronization Input Minimum Off-Time	$t_{SYNCPWOFF}$		•	150	–	–	ns
Synchronization Input Minimum On-Time	$t_{SYNCPWON}$		•	150	–	–	ns
Synchronization Input Logic – Low	$V_{SYNCON(L)}$		•	–	–	0.4	V
Synchronization Input Logic – High	$V_{SYNCON(H)}$		•	2	–	–	V
LED CURRENT SINKS							
LEDx Accuracy (Average)	Err_{LEDx}	Measured at I_{LEDMAX} (maximum LED current)	•	–	0.7	3	%
LEDx Matching	ΔI_{LEDx}	Compared to average I_{LEDx} , measured at I_{LEDMAX}	•	–	0.8	3	%
LEDx Regulation Voltage	V_{REG}	ISET register= xx11 1111	•	–	0.85	1.0	V
I_{LEDx} Step Size	$I_{SETSTEP}$	Total 64 steps	•	0.9	1	1.1	mA
Maximum LEDx Current (Average)	I_{LEDMAX}	ISET register = xx11 1111		62	64	66	mA
Minimum LEDx Current	I_{LEDMIN}	ISET register = xx00 0000		–	1	–	mA
LEDx Short-Detect Threshold	V_{LED_SD}	Short-Detect register = 000		–	12	–	V
		Short-Detect register = 111		–	5	–	V
INTERRUPTS (FLAG, GPO1 AND GPO2 PINS)							
Pin Pull-Down Voltage		Fault / Interrupt condition asserted, pull-up current = 0.5 mA	•	–	–	0.4	V
Pin Leakage Current		Fault / Interrupt condition cleared, pull-up to 3.6 V	•	–	–	1	µA
INTERNAL MASTER CLOCK							
Master Clock Period	T_{CLK}		•	120	150	180	ns
Master Clock Temperature Deviation [2]	ΔT_{CLK}	T_{CLK} change over temperature range	•	–2.5	–	2.5	%

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT DISCONNECT							
GATE Pin Sink Current	I_{GSINK}	V_{GATE} = V_{IN}, no input overcurrent fault tripped		–	115	–	µA
GATE Pin Source Current	$I_{GSOURCE}$	V_{GATE} = V_{IN} – 5 V, input overcurrent fault tripped		–	–6	–	mA
GATE Voltage at Off	V_{GSOFF}	EN = $V_{EN(L)}$, or overcurrent fault occurred		–	V_{IN}	–	V
GATE Voltage at On	V_{GSON}	Gate-to-source voltage when gate is on, measured as V_{IN} – V_{GATE}	•	5	–	8	V
GATE Pin Leakage Current	I_{GLKG}	EN = $V_{EN(L)}$, V_{GATE} = V_{IN}	•	–	–	1	µA
INS Pin Sink Current	$I_{INSSINK}$			–	20	–	µA
INS Trip Point	$V_{INSTRIP}$	Measured between VIN and INS	•	90	105	120	mV
INS Trip Detection Time [2]	$t_{INSTRIP}$	Sensed voltage, V_{IN} – V_{INS} = 160 mV		–	2	–	µs
Thermal Protection (TSD)							
Thermal Shutdown Threshold [2]	T_{SD}	Temperature rising		155	170	–	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}			–	20	–	°C
Thermal Warning Threshold	T_{SDWARN}	Temperature rising, measured as difference from TSD		–	20	–	°C
I²C INTERFACE							
Logic Input (SDA, SCL) – Low	$V_{SCL(L)}$			–	–	0.8	V
Logic Input (SDA, SCL) – High	$V_{SCL(H)}$			2.3	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$			–	150	–	mV
Logic Input Current	I_{I2CI}			–1	–	1	µA
Output Voltage SDA	$V_{I2COut(L)}$	SDA = low, pull-up current = 2.5 mA		–	–	0.4	V
Output Leakage SDA	I_{I2CLKG}	EN = low, pull-up to 5.5 V		–	–	1	µA
SCL Clock Frequency	f_{CLK}			–	–	400	kHz
ADDR PIN							
Voltage Level for Address 100,0000	$V_{ADDLEVEL1}$	ADDR connected to GND		0	–	0.5	V
Voltage Level for Address 101,0000	$V_{ADDLEVEL2}$	R_{ADDR} = 110 kΩ from ADDR to GND		0.9	–	1.3	V
Voltage Level for Address 110,0000	$V_{ADDLEVEL3}$	R_{ADDR} = 210 kΩ from ADDR to GND		1.75	–	2.45	V
Voltage Level for Address 111,0000	$V_{ADDLEVEL4}$	ADDR connected to VDD pin or open		3.2	–	3.6	V
ADDR Pull-Up Current	I_{ADDR}	V_{ADDR} = 1 V		–8.5	–10	–11.5	µA
INTERNAL REGULATOR							
Bias Supply Voltage	V_{DD}			–	3.6	–	V

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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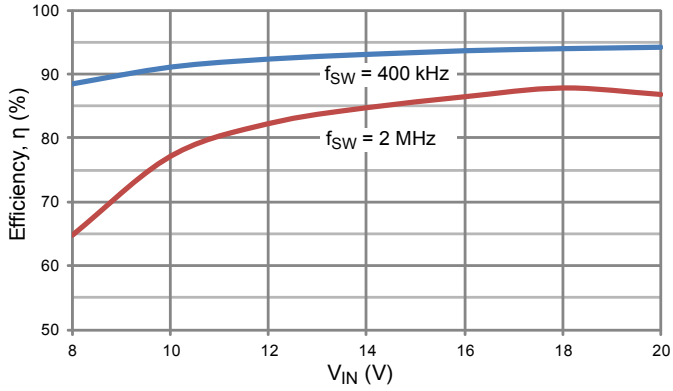
CHARACTERISTIC PERFORMANCE

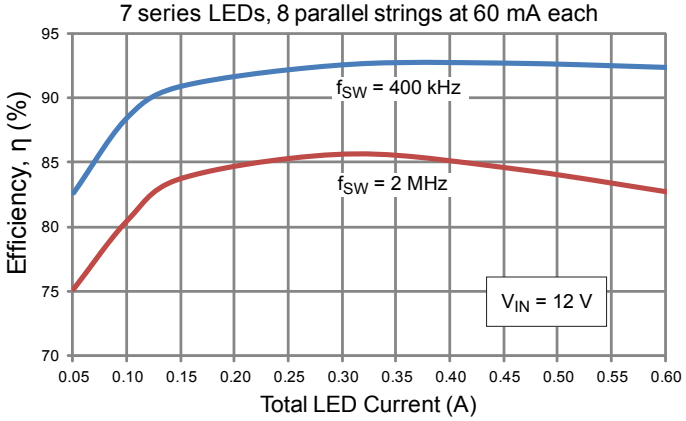
Efficiency versus Input Voltage

7 series LEDs, 8 parallel strings at 60 mA each



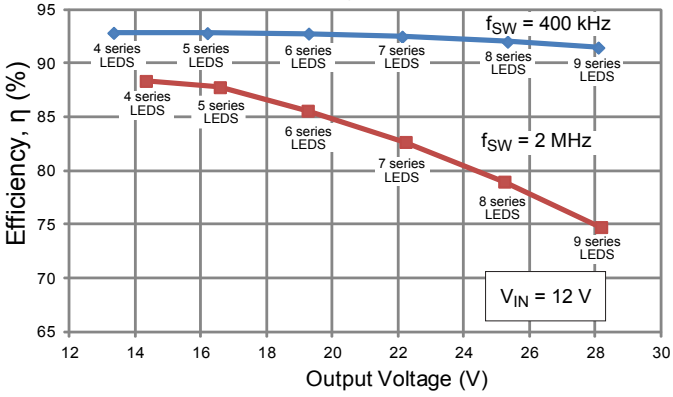
Efficiency versus Output Current

7 series LEDs, 8 parallel strings at 60 mA each



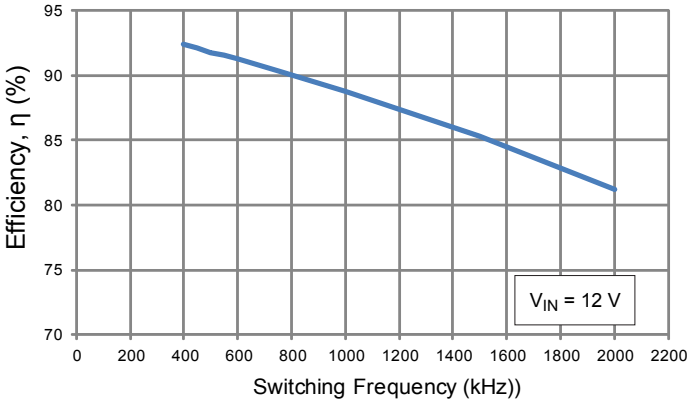
Efficiency versus Output Voltage

8 parallel strings at 60 mA each



Efficiency versus Switching Frequency

9 series LEDs, 8 parallel strings at 50 mA each, L1 = 47 µH



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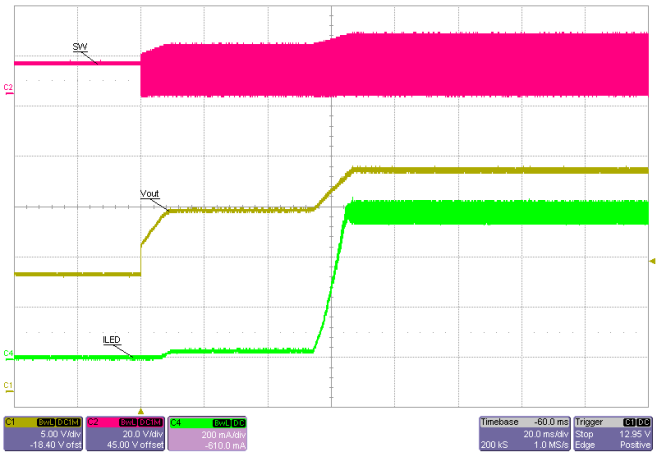
Startup Waveform at V_{IN} = 12 V Dimming PWM Duty Cycle = 100%



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 12 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 100%
Polyphase mode = on

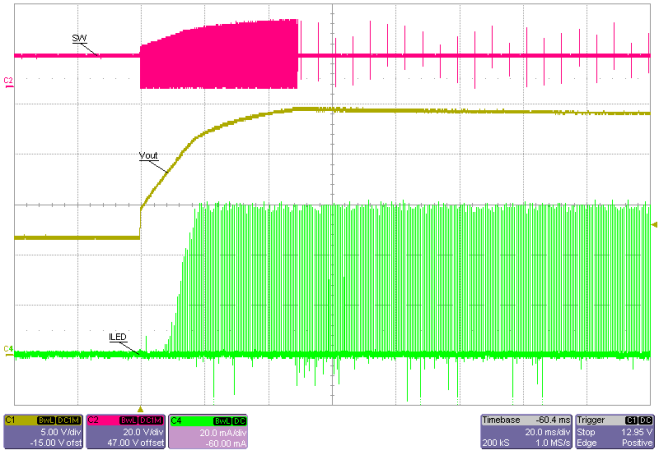
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C2 (Red) = V_{SW} (20 V/div)
C4 (Green) = I_{LED} (200 mA/div)
Time scale = 20 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Startup Waveform at V_{IN} = 12 V Dimming PWM Duty Cycle = 0.02%



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 5.5 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 0.02% at 200 Hz (5000:1)
Polyphase mode = on

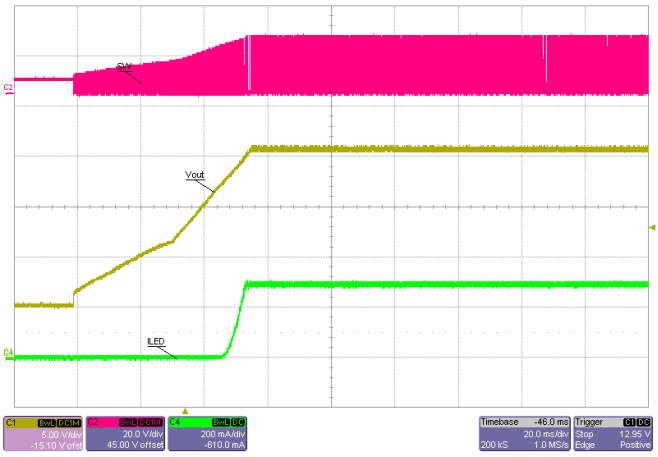
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C2 (Red) = V_{SW} (20 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 20 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Startup Waveform at V_{IN} = 5.5 V Dimming PWM Duty Cycle = 100%



Test conditions:

LED strings = 8 parallel, 30 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 12 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 100%
Polyphase mode = on

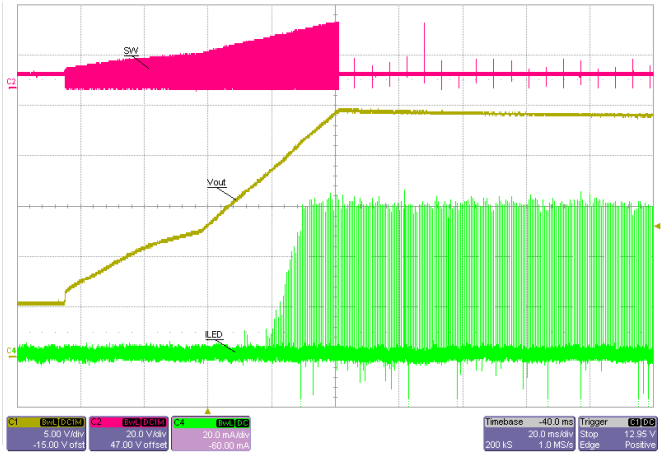
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C2 (Red) = V_{SW} (20 V/div)
C4 (Green) = I_{LED} (200 mA/div)
Time scale = 20 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Startup Waveform at V_{IN} = 5.5 V Dimming PWM Duty Cycle = 0.02%



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 5.5 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 0.02% at 200 Hz (5000:1)
Polyphase mode = on

Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C2 (Red) = V_{SW} (20 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 20 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

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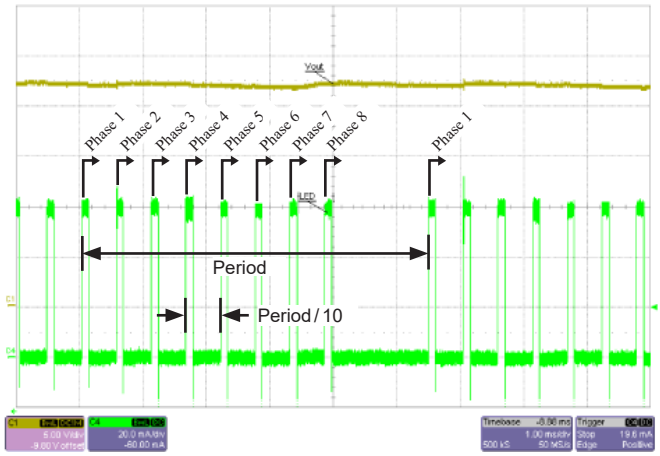
PWM Operation with Polyphase



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 12 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 2% at 200 Hz
Polyphase mode = on (each on at assigned time slot)

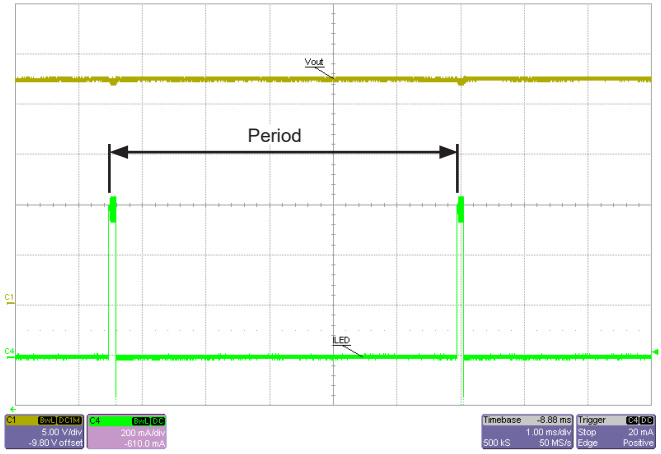
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C4 (Green) = I_{LED} (200 mA/div)
Time scale = 1 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

PWM Operation without Polyphase



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
V_{IN} = 12 V
Dimming PWM duty cycle = 2% at 200 Hz
Polyphase mode = off (all simultaneously on)

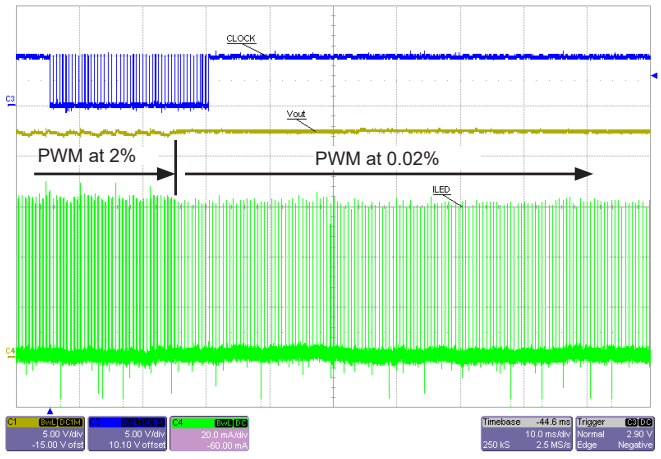
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C4 (Green) = I_{LED} (200 mA/div)
Time scale = 1 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Transient Response to Step-Change In PWM Duty Cycle (2% to 0.02%)



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
V_{IN} = 12 V
Dimming PWM duty cycle = change from 2% to 0.02% at 200 Hz (PWM on-time change from 100 µs to 1 µs)
Polyphase mode = on

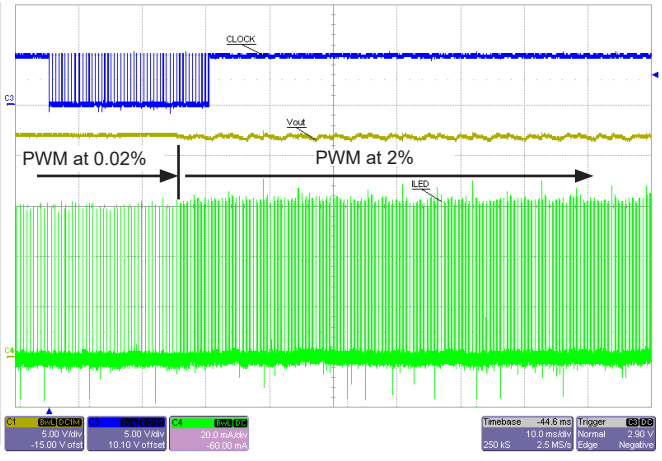
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = I²C clock (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Transient Response to Step-Change In PWM Duty Cycle (0.02% to 2%)



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
V_{IN} = 12 V
Dimming PWM duty cycle = change from 0.02% to 2% at 200 Hz (PWM on-time change from 1 µs to 100 µs)
Polyphase mode = on

Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = I²C clock (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

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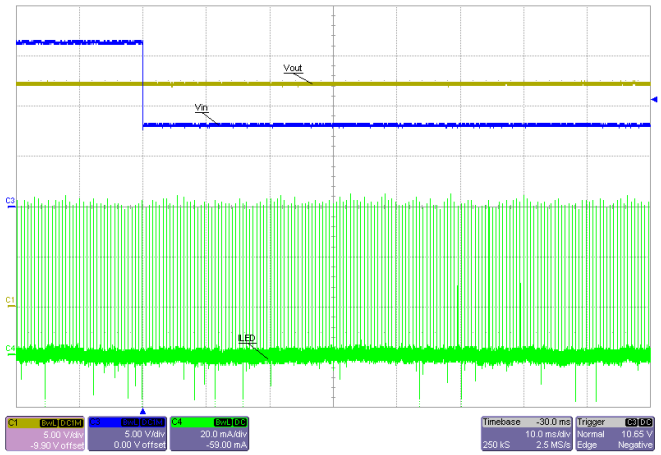
Transient Response to Step-Change In V_{IN} (16 V to 8 V) PWM Duty Cycle 0.02%



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
V_{IN} = change from 16 V to 8 V
Dimming PWM duty cycle = 0.02% at 200 Hz

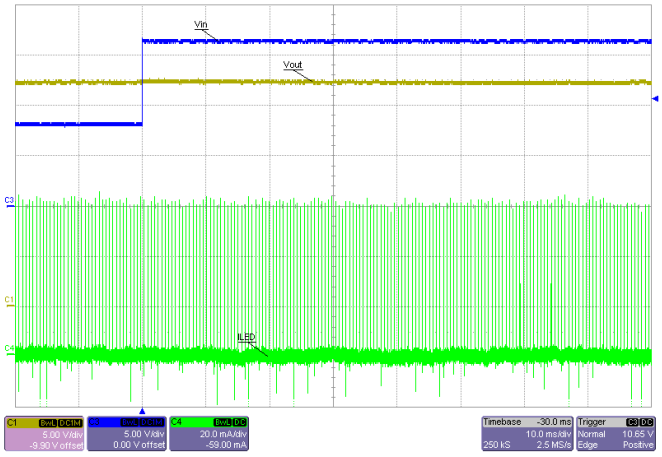
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = V_{IN} (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Transient Response to Step-Change In V_{IN} (8 V to 16 V) PWM Duty Cycle 0.02%



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
V_{IN} = change from 8 V to 16 V
Dimming PWM duty cycle = 0.02% at 200 Hz

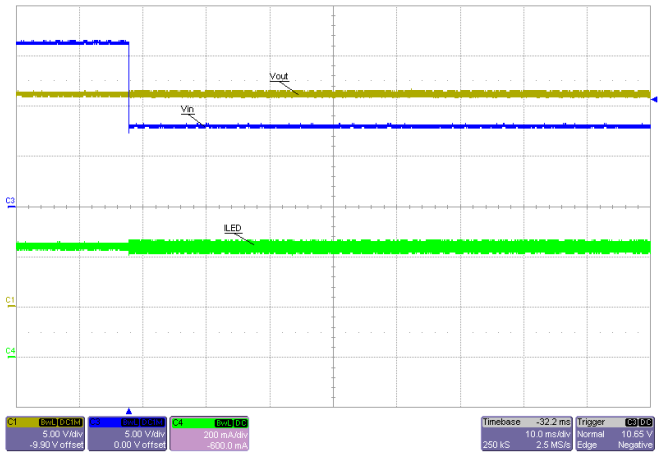
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = V_{IN} (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Transient Response to Step-Change In V_{IN} (16 V to 8 V) PWM Duty Cycle 100%



Test conditions:

LED strings = 8 parallel, 45 mA each
LEDs = 7 series each string
V_{IN} = change from 16 V to 8 V
Dimming PWM duty cycle = 100%

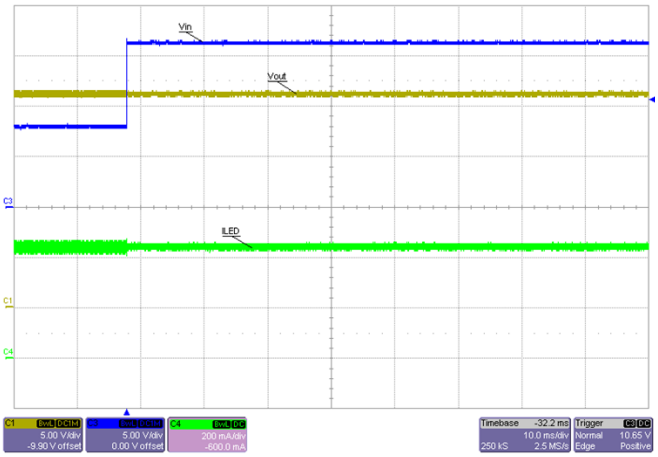
Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = V_{IN} (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Transient Response to Step-Change In V_{IN} (8 V to 16 V) PWM Duty Cycle 100%



Test conditions:

LED strings = 8 parallel, 45 mA each
LEDs = 7 series each string
V_{IN} = change from 8 V to 16 V
Dimming PWM duty cycle = 100%

Scope traces:

C1 (Yellow) = V_{OUT} (5 V/div)
C3 (Blue) = V_{IN} (5 V/div)
C4 (Green) = I_{LED} (20 mA/div)
Time scale = 10 ms/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

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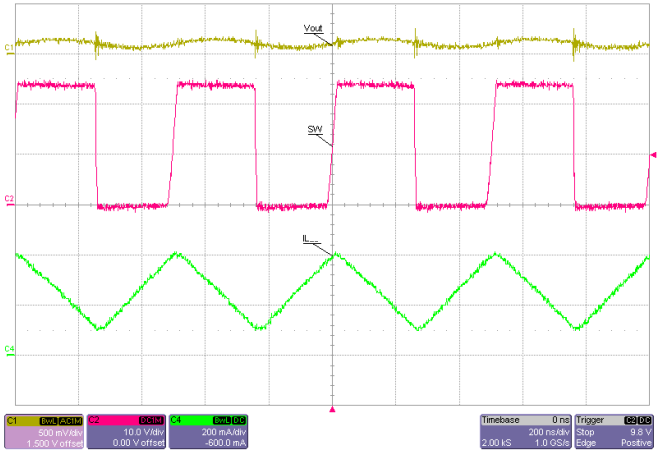
Switch Node, AC Output Voltage Ripple, And Inductor Current



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
LED V_{REG} = 0.85 V
V_{IN} = 12 V
V_{OUT} hysteresis = 0.45 V
Dimming PWM duty cycle = 20%
Polyphase mode = on

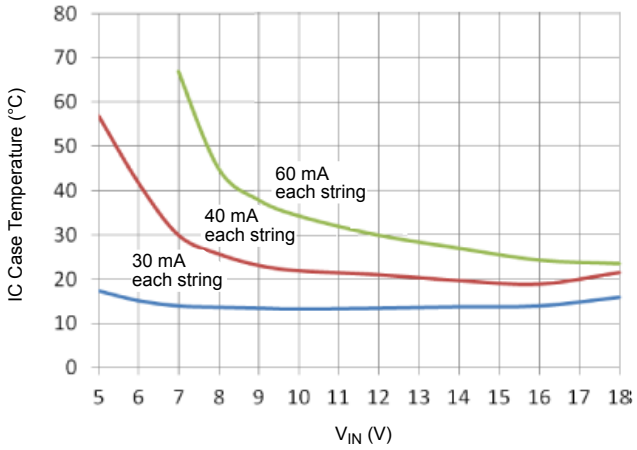
Scope traces:

C1 (Yellow) = V_{OUT} (500 mV, AC/div)
C2 (Red) = V_{SW} (10 V/div)
C4 (Green) = I_L (inductor current)(200 mA/div)
Time scale = 200 ns/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Temperature Rise versus V_{IN} 7 series LEDs in 8 parallel strings



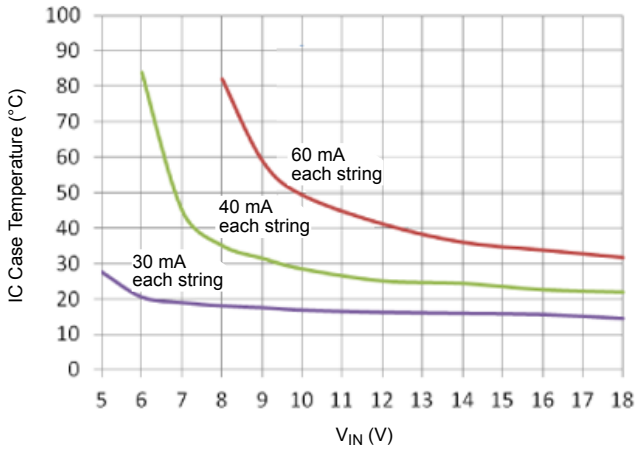
Test conditions:

LED strings = 8 parallel
LEDs = 7 series each string
f_{SW} = 2 MHz
Dimming PWM duty cycle = 100%
Polyphase mode = on

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Temperature Rise versus V_{IN} 8 series LEDs in 8 parallel strings



Test conditions:

LED strings = 8 parallel
LEDs = 8 series each string
f_{SW} = 2 MHz
Dimming PWM duty cycle = 100%
Polyphase mode = on

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

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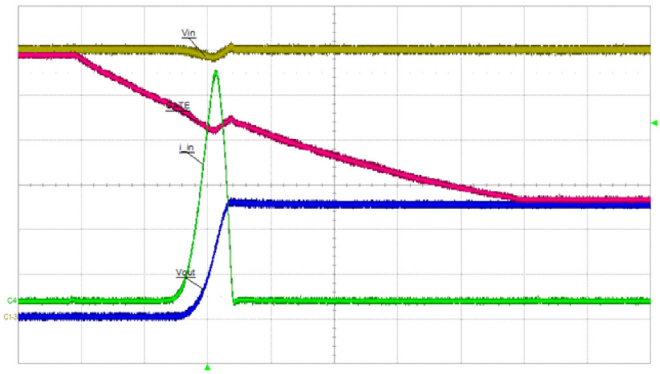
FAULT HANDLING

Input Overcurrent Protection

Case 1: Normal startup when using input disconnect switch



Test conditions:

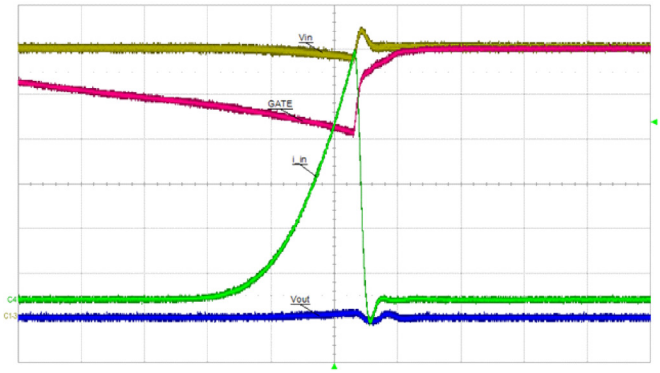
Q1 = AO4421
C_{GS} = 10 nF
V_{IN} = 12 V
R_{SENSE} = 18 mΩ

GATE is being slowly pulled down (from V_{IN} to V_{IN} – 6.8 V) to control the inrush current.

Scope traces:

C1 (Yellow) = V_{IN} (2 V/div)
C2 (Red) = V_{GATE} (2 V/div)
C3 (Blue) = V_{OUT} (5 V/div)
C4 (Green) = I_{IN} (1 A/div)
Time scale = 200 µs/div

Case 2: Output-to-GND short fault occurred before startup



Test conditions:

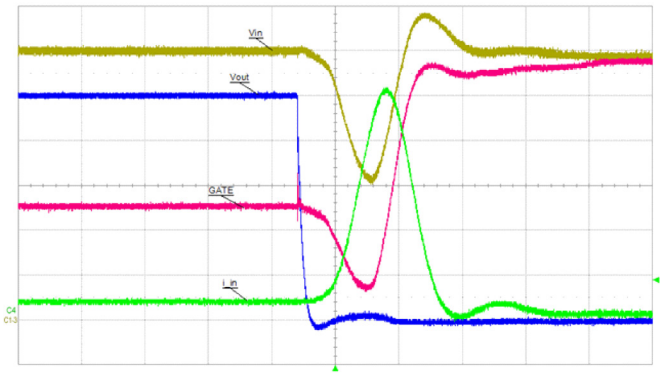
Q1 = AO4421
C_{GS} = 10 nF
V_{IN} = 12 V
R_{SENSE} = 18 mΩ

Startup into a VOUT-to-GND short. GATE is pulled high as soon as the input current > 5.8 A, in order to turn off the input disconnect switch.

Scope traces:

C1 (Yellow) = V_{IN} (2 V/div)
C2 (Red) = V_{GATE} (2 V/div)
C3 (Blue) = V_{OUT} (5 V/div)
C4 (Green) = I_{IN} (1 A/div)
Time scale = 50 µs/div

Case 3: Output-to-GND short occurred during normal operation



Test conditions:

Q1 = AO4421
C_{GS} = 10 nF
V_{IN} = 12 V
R_{SENSE} = 18 mΩ

Output shorted to GND during normal operation, causing a huge inrush current. GATE is pulled high, in order to turn off the input disconnect switch and prevent damage to the power supply.

Scope traces:

C1 (Yellow) = V_{IN} (2 V/div)
C2 (Red) = V_{GATE} (2 V/div)
C3 (Blue) = V_{OUT} (5 V/div)
C4 (Green) = I_{IN} (5 A/div)
Time scale = 10 µs/div

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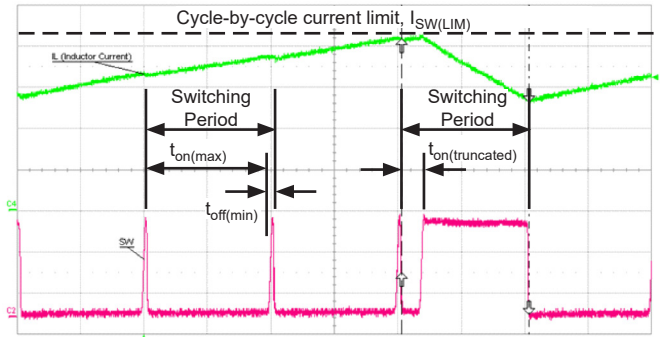
Switch Overcurrent Protection



Test conditions:

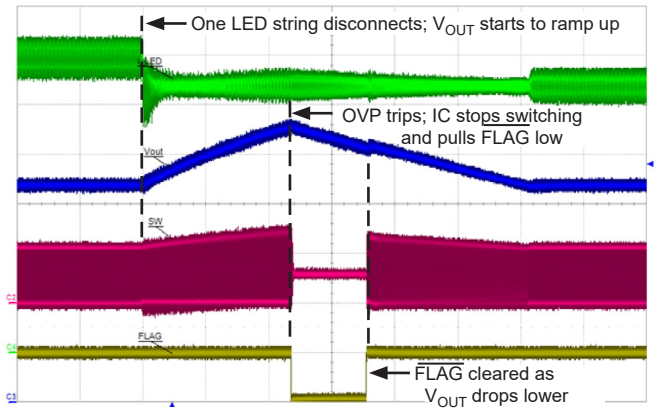
LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
f_{SW} = 1 MHz
V_{IN} = 6.5 V

V_{IN} intentionally lowered to the point where SW cycle-by-cycle current limit is tripped. SW operating at maximum on-time initially. Inductor current ramps up and trips cycle-by-cycle current limit (≈ 4.2 A). Present on-time is truncated immediately. Next switching cycle starts normally.

Scope traces:

C2 (Red) = V_{SW} (10 V/div)
C4 (Green) = I_L (1 A/div)
Time scale = 500 ns/div

LED String Open Fault Detection



Test conditions:

LED strings = 8 parallel, 60 mA each
LEDs = 7 series each string
f_{SW} = 2 MHz
V_{IN} = 12 V

One LED string is disconnected during normal operation. After output trips OVP, the offending LED string is removed from regulation, while other strings continue to function correctly.

Scope traces:

C1 (Yellow) = V_{FLAG} (5 V/div)
C2 (Red) = V_{SW} (10 V/div)
C3 (Blue) = V_{OUT} (5 V/div)
C4 (Green) = I_{LED} (100 mA/div)
Time scale = 200 µs/div

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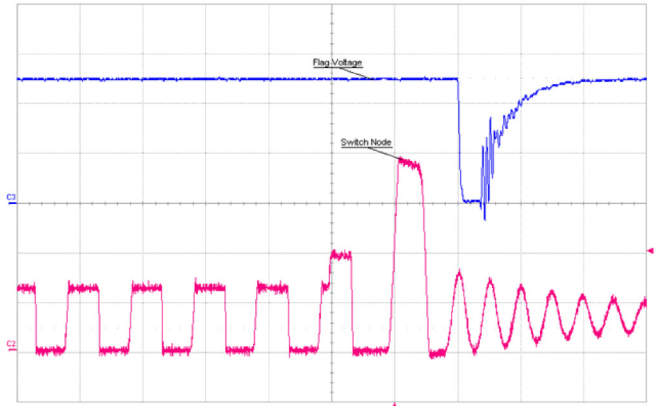
Protection Against Open/Missing BOOST Diode

Case 1: BOOST diode becomes open during normal operation



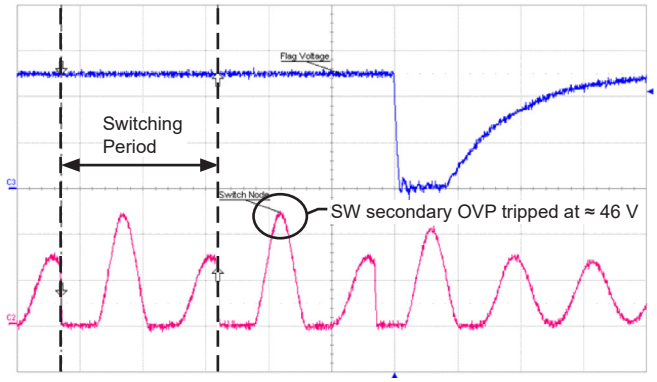
Test conditions:

BOOST diode becomes open during normal operation. Energy stored in inductor causes a high voltage across SW. SW DMOS conducts at V_{SW} > 75 V to discharge the energy safely. IC shuts off after detecting an overvoltage condition at the SW pin.

Scope traces:

C2 (Red) = V_{SW} (20 V/div)
C3 (Blue) = V_{FLAG} (2 V/div)
Time scale = 500 ns/div

Case 2: BOOST diode missing during startup



Test conditions:

BOOST diode is missing during startup. Energy stored in inductor gradually builds up, causing higher and higher voltage across the SW pin. Eventually the IC shuts off after detecting an overvoltage fault at the SW pin (V_{SW} > 50 V).

Scope traces:

C2 (Red) = V_{SW} (20 V/div)
C3 (Blue) = V_{FLAG} (2 V/div)
Time scale = 200 ns/div

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FUNCTIONAL DESCRIPTION

The A8522 is an I²C programmable, multi-channel LED driver for automotive lighting applications. It incorporates a current-mode boost controller with internal DMOS boost switch, and 8 integrated current sinks to regulate currents through up to 8 LED strings. Each LED string can be independently enabled or disabled, with its own LED current and PWM duty cycle programmed through I²C registers.

Enabling the IC

The IC turns on when a logic high signal, $V_{EN(H)}$, is applied on the EN pin, and the input voltage present on the VIN pin is greater than the UVLO threshold, $V_{INUV(ON)}$. The EN pin is rated for 40 V, so it can be tied directly to V_{IN} for certain applications (see Application Information section). In addition, if the FSET/SYNC pin is pulled low, the IC does not power up.

The A8522 performs a detailed startup sequence, flow chart and timing diagram are shown in figures 4a to 4c. Before the LEDs are enabled, the device goes through a system check to determine if there are any possible fault conditions that might prevent the system from functioning correctly. Once the LEDs pass the “LED short during start up” test the $\overline{FLAG}$ pin will be pulled low for a short period of time. If no subsequent faults are detected during this startup sequence, the IC pulls down the GPO2 pin to signal to the system controller that the A8522 is ready to receive I²C commands.

The system controller programs the A8522 internal registers through I²C Write commands, in order to configure individual LED strings before they can be turned on. On initial startup I²C should first send a clear command to bit 2 of register bank number 56, this ensures that an erroneous fault does not prevent the LEDs turning on. This command is only required on power up and/or enable (via EN pin) of the A8522. I²C can now communicate regularly with the A8522. Ensure I²C only enables populated LED’s. If I²C tries to enable unpopulated LED strings an illegal action is declared and no LEDs will turn on.

In the event of a genuine fault during start up, the $\overline{FLAG}$ pin is pulled low, and the system controller can issue I²C Read commands to investigate the status of fault registers. In this instance I²C should not clear bit 2 of register bank number 56.

The device enters into shutdown mode when the EN pin is pulled low, $V_{EN(L)}$.

Frequency Selection and Synchronization

The internally-generated switching frequency of the boost converter, f_{SW}, is set by the resistor R_{FSET}, connected from the FSET/SYNC pin to GND. The frequency can be set in the range from 400 kHz to 2.3 MHz. The switching frequency is determined according to the following equation:

$$f_{SW}\,(MHz) = 19.9 / R_{FSET}\,(k\Omega) + 0.01 \qquad (1)$$

Figure 1 illustrates how f_{SW} varies with R_{FSET}.

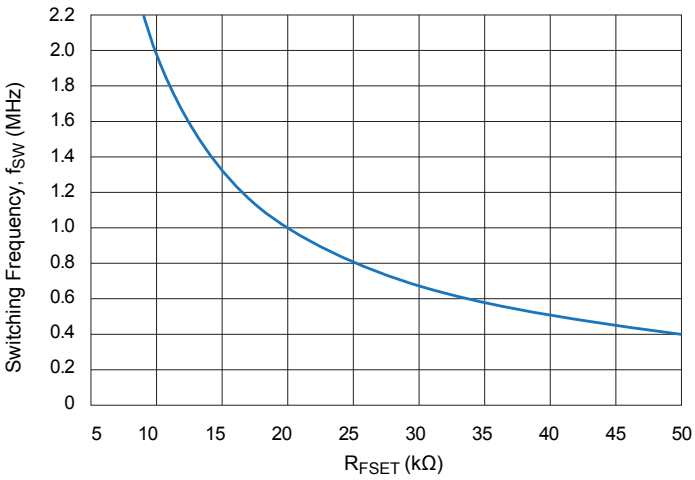

Figure 1: Switching Frequency versus Value of the R_{FSET} Resistor

Alternatively, the switching frequency can also be synchronized using an external clock signal on the FSET/SYNC pin. The external clock should be a logic signal between 400 kHz and 2.3 MHz. When an external clock is applied, the R_{FSET} resistor is ignored. If the A8522 is started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation, then one of the following happens:

1. If the external SYNC signal becomes high impedance (open), the A8522 waits for approximately 6 µs from the last edge detected, before it resumes normal operation at the switching frequency set by RFSET. No fault flag is generated.
2. If the external SYNC signal gets stuck low (shorted to ground), the A8522 will still attempt to operate at switching frequency set by RFSET. However, since RFSET is shorted to GND by the external SYNC signal, it will trip the FSET to GND short fault and shut down the output. The Fault Flag is pulled low in this case.

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To avoid the outcome of the second scenario above, the circuit shown in Figure 2 can be used. In this case, after the external SYNC signal goes low, the A8522 will continue to operate normally at the switching frequency set by R_{FSET}.

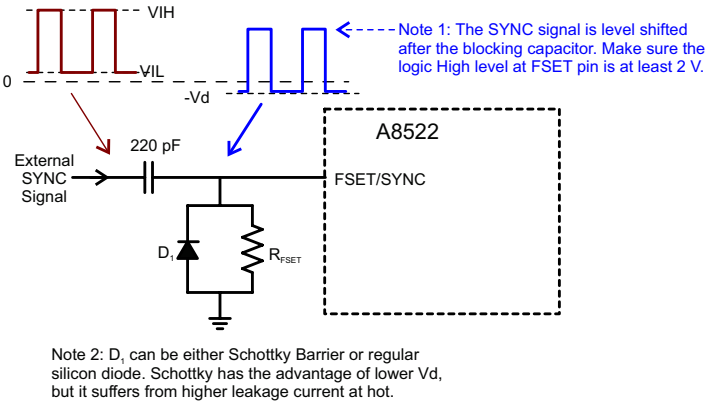

Figure 2: Low FSET_SYNC Signal Fault Counteraction Circuit

PWM Dimming

The PWM dimming period (hence the PWM frequency) is defined by the 13-bit PWM_Period register. It is programmable at any time through the I²C interface, in 1.5 µs increments, as:

$$PWM\_Period = (N + 1) \times 1.5\ (\mu s) \qquad (2)$$

where N is the value contained in the register.

The PWM on-time (hence the PWM duty cycle) for each LED string is defined by the corresponding 16-bit register. The PWM on-time can be adjusted in 0.15 µs increments. This is illustrated in Figure 4. The smallest PWM on-time is 1 µs. This corresponds to a 5000:1 ratio at a 200 Hz PWM frequency.

Output Current and Voltage

The current through each LED string can be programmed through I²C registers to between 1 and 64 mA, in 1 mA steps.

For optimal efficiency, the output of the boost stage is dynamically adjusted to the minimum voltage required for all active LED strings. This is expressed by the following equation:

$$V_{OUT} = MAX(V_{LED1}, V_{LED2}, \ldots V_{LED8}) + V_{REG} + V_{HYST} \qquad (3)$$

where

V_{LEDx} is the voltage drop across an LED string (only the enabled LED strings are considered),

V_{REG} is the regulation voltage of the LED current sink (0.85 V (typ)), and

V_{HYST} is the hysteresis control voltage at the output (typically 0.25 V).

The boost output voltage is protected by the OVP threshold, which can be programmed up to 39 V. This is sufficient for driving up to 10 white LEDs in series.

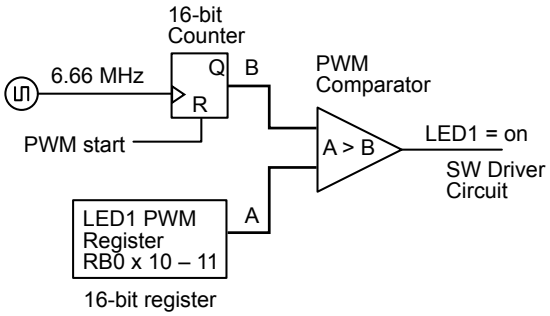

Figure 3: PWM On-time Comparator Circuit

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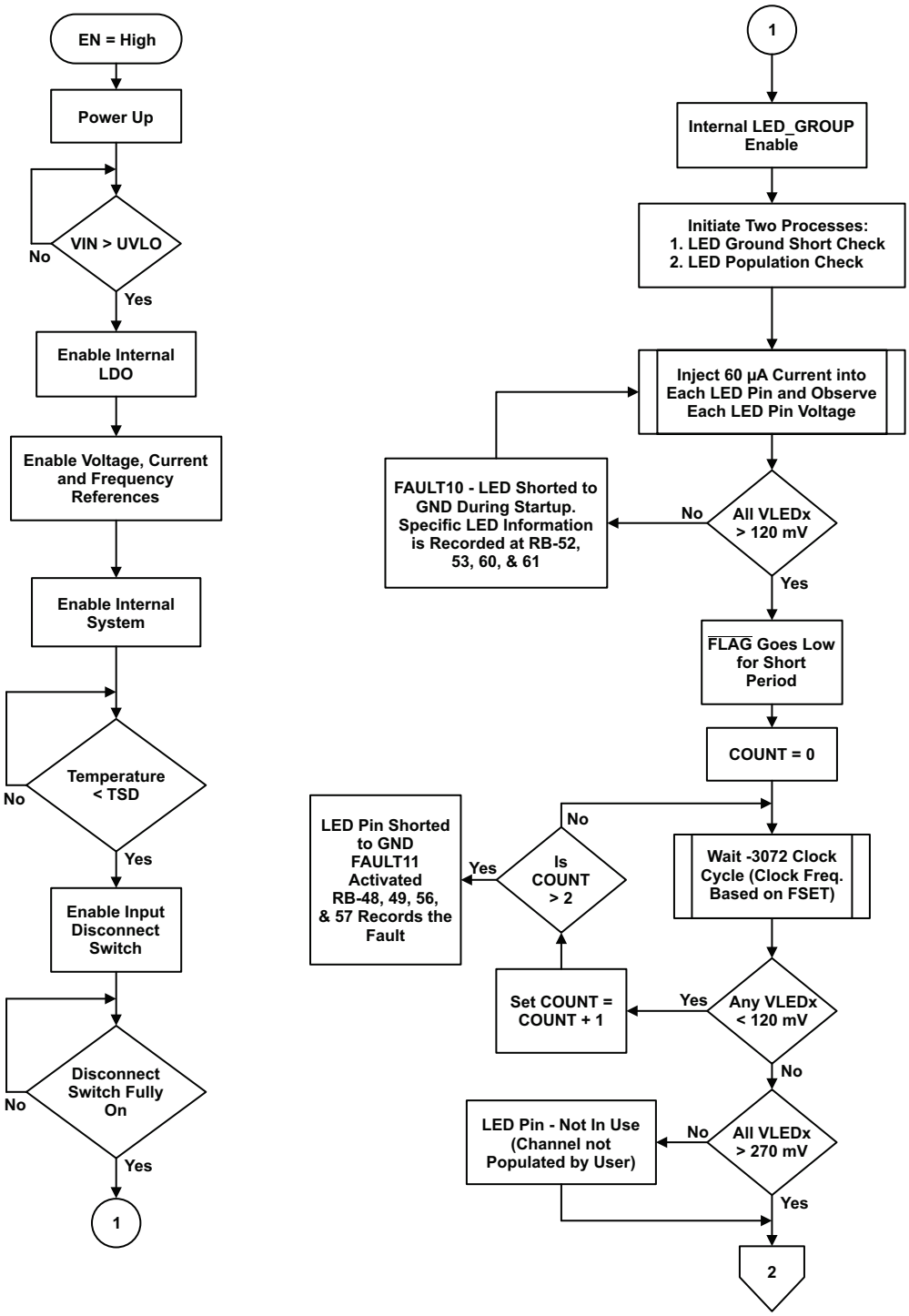

Figure 4a: A8522 Startup and Fault 11 Detect Flow Chart

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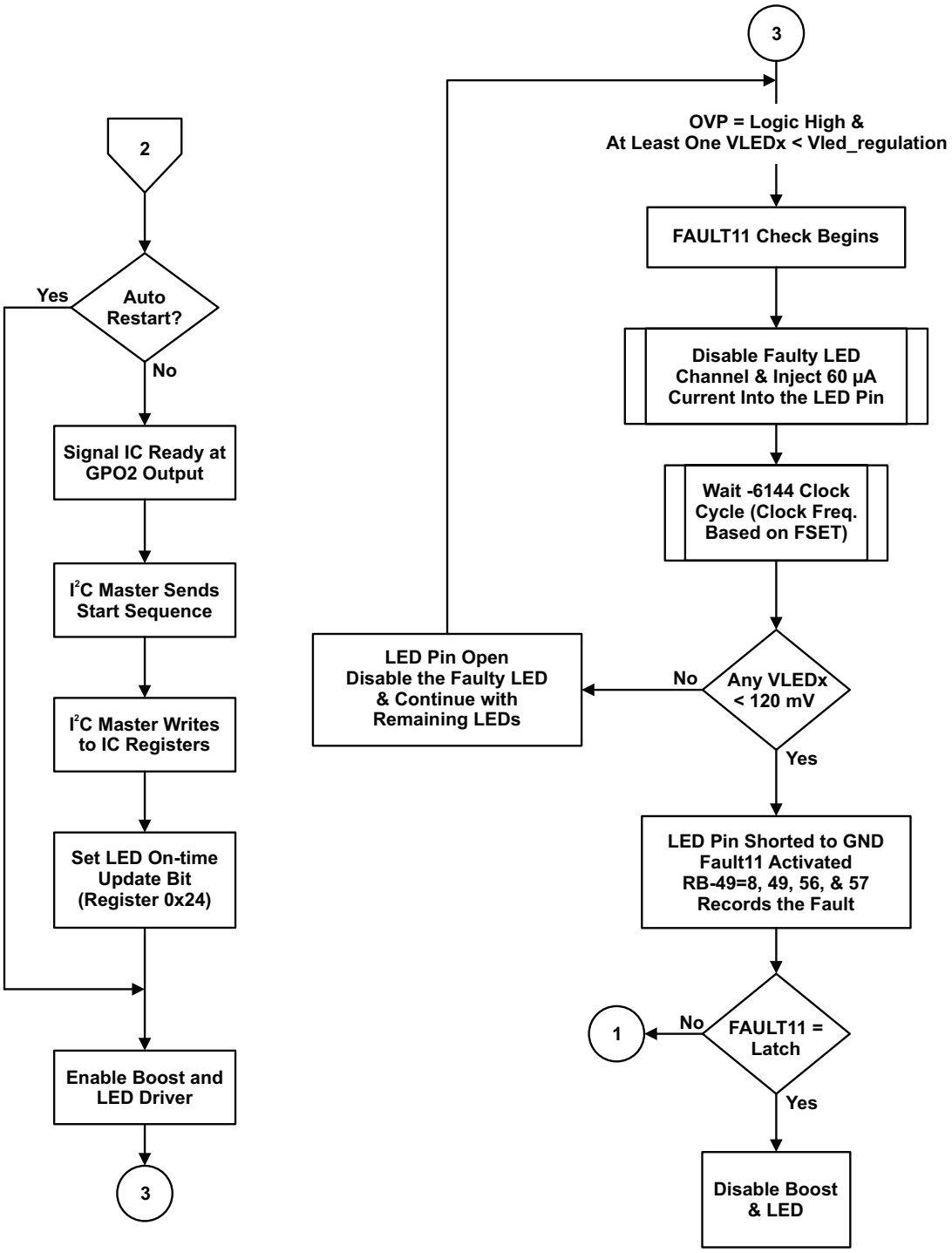

Figure 4b: A8522 Startup and Fault 11 Detect Flow Chart (Cont.)

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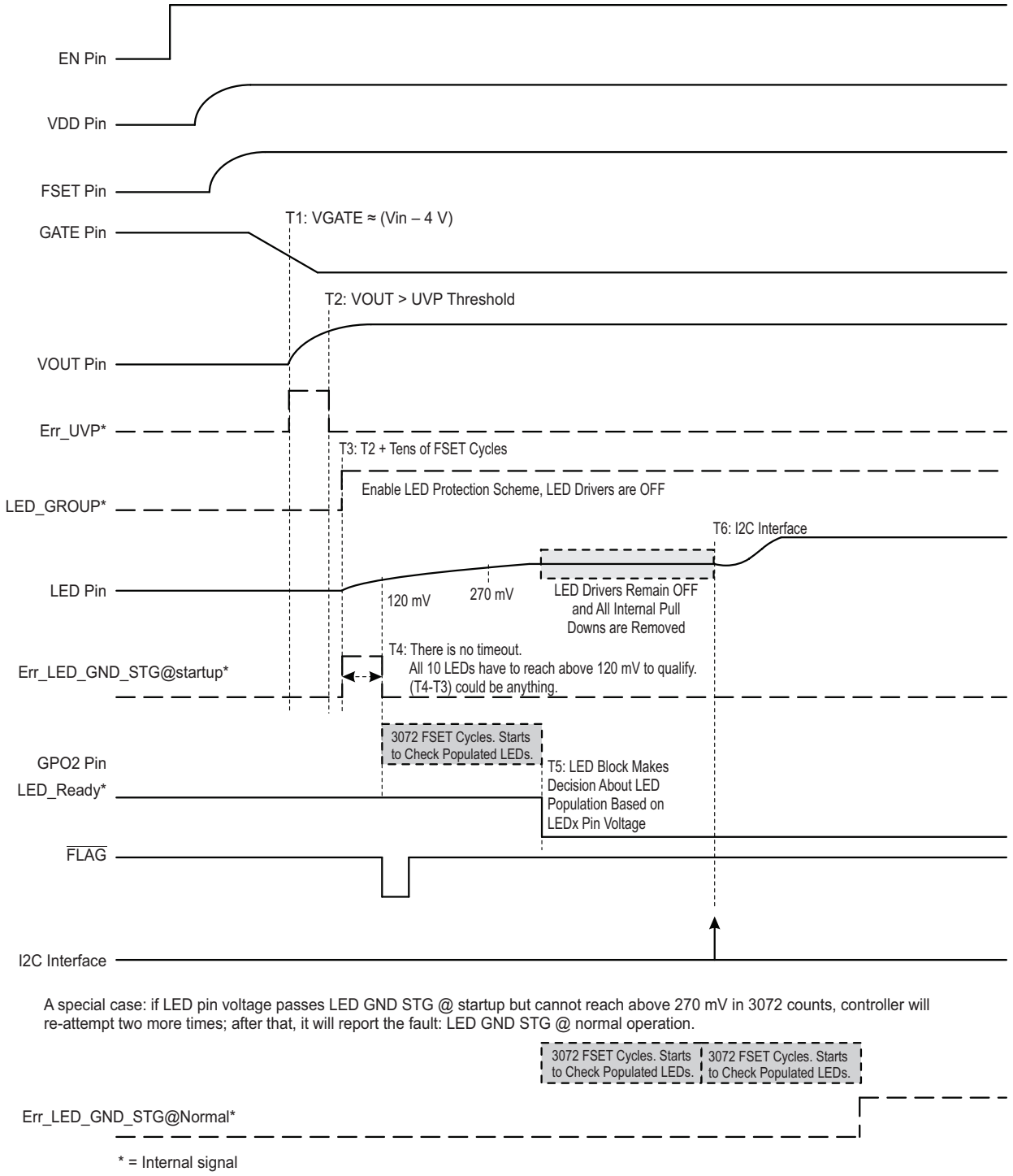

Figure 4c: A8522 Startup Timing Diagram

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Boost Frequency Dithering

The Boost Dithering function allows the user to randomize the main switching frequency within a certain frequency range. By shifting the main switching frequency of the regulator in a pseudo-random fashion around the main switching frequency, the overall system noise magnitude can be greatly reduced. Note that the frequency dithering function is not available when an external synchronization signal is used at the FSET/SYNC pin.

This spread spectrum functionality is achieved by a programmable register (0x05[BD1:BD0]. A non-zero number enables the boost dithering and sets the modulation index of 5%, 10%, or 15% of f_{SW}. For example, if 10% dithering is selected, then the switching frequency will jump between a low of 1.8 MHz and a high of 2.2 MHz, as governed by the pseudo-random pattern.

Every two switching cycles, the switching frequency may randomly jump between low and high levels. The random pattern repeats itself after 92 switching cycles. This is illustrated by the timing diagram in Figure 5.

Polyphase Grouping

During PWM operation, by default each of the ten LED channels starts at a separate time slot, or phase, (Figure 6, top panel) and with a specified on-time setting. If required, two or more adjacent LED channels can be grouped by programming to turn on and off simultaneously (Figure 6, bottom panel). By tying the corresponding pins together on the PCB, it is possible to combine several channels to drive higher-current LED strings (see Typical Application schematics).

Each LED channel has an LED channel enable bit (register 0x01) and an LED PWM on-time setting register (0x10 to 0x1F). In normal PWM operation, any enabled LED channel is turned on starting at its own time slot, and remains on for the duration controlled by its own PWM on-time register. By staggering the time slots for LED channels, the input ripple current is reduced during PWM operation.

If necessary, such as when more than 1 channel is required to drive an LED string at current higher than 60 mA, the user can group two or more adjacent LED channels together, so that they turn on/off simultaneously. Grouping is done by setting the corresponding bits in the Polyphase Grouping registers (0x08 and 0x09).

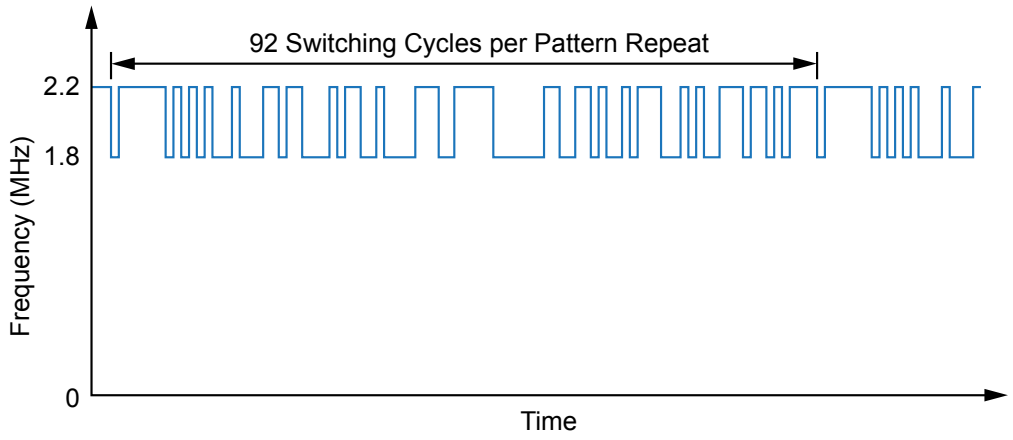

Figure 5: A8522 Dithering Scheme at 2 MHz ±10%

(frequency jumps between 1.8 MHz and 2.2 MHz, as governed by a 46-bit pseudorandom pattern)

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A grouped LED channel starts in the same time slot as the lower-numbered channel, and inherits the PWM Dimming On-Time of that lower-numbered channel (the original time slot of the grouped channel is not used). If more than one adjacent channels are grouped, the entire group starts at the time slot of the lowest-numbered channel in the group, and inherits that on-time setting.

For example, in Figure 6, LED1 and LED2 are grouped together, so they start at PWM slot 1 and follow the on-time of LED1. Similarly, LED3, LED4, and LED5 are grouped together, so they start at PWM slot 3 and follow the on-time of LED3.

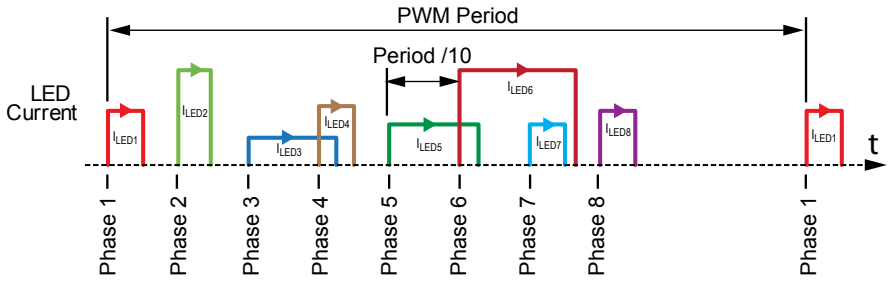
If the first LED channel in a polyphase group is disabled through the LED enable register, then all the LEDs in this group are disabled. If any other LED channels in a group are disabled, all of the other LED channels in the group remain enabled, with the PWM on-time of the first LED channel in the group.

Boost Output Voltage Regulation

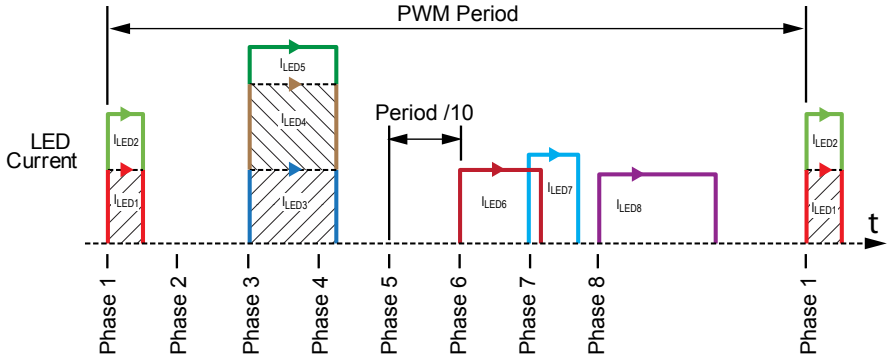
Output from the boost stage is adaptively adjusted, based on the voltage required by all the enabled LED strings. This ensures minimum power loss at the LED current sinks, and reduces input power consumption.

During operation, the LED string with the highest voltage drop is the dominant string, and it is used to determine the boost output voltage regulation. Because each LED string can be individually enabled/disabled dynamically, which string is dominant can shift at different times.

As an example, assume LED channels 1, 3, and 5 are currently enabled. Further assume that voltage drops across the LED strings are 21 V, 23 V, and 25 V respectively. The boost output voltage will be regulated to the highest LED string voltage (25 V)



Polyphase PWM Operation without Grouping – Each LED channel turns-on at a separate, sequential, periodic time slot. The LED on-times are individually programmable, so any individual phase can overlap later time slots.The LED current for each channel is individually programmed.



Polyphase PWM Operation with Grouping – The starting time slot and the PWM on-time for each group is determined by the time slot and the on-time of the lowest-numbered channel within that group, so all LED channels in the same group turn-on and turn-off together. Each time slot is sequential and periodic, and unused time slots are maintained. Any individual phase can overlap later time slots. The LED current for each channel is individually programmed, regardless of grouping.

Figure 6: Polyphase Operation

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plus the regulation voltage required by the LED current sink (0.85 V typical):

LED Channel #	LED String Voltage Drop (V)	Boost Output Voltage (V)	LEDx Pin Voltage (V)
1	21	25.85 + Hysteresis	4.85 min
3	23		2.85 min
5	25 (dominant)		0.85 min

For LED strings 1 and 3, the extra voltage is absorbed by their current sinks. When the LED string voltages are poorly balanced (as in this example), excessive power loss can build up at the current sinks. Consider adding ballast resistors to the LED strings with lower voltage drops, so that less heat is dissipated by the IC.

Output Hysteresis

The A8522 superposes a minimum output hysteresis of 0.25 V on top of the LED regulation voltage. The OVP pin provides output voltage feedback during hysteresis control mode. An example of output voltage is show in Figure 7.

When the dominant LED is on, boost stage starts switching to keep the corresponding LEDx pin voltage regulated to V_{REG}. After the dominant LED is turned off, the switching continues until boost output reaches $V_{TH(+)}$. The output is then regulated between $V_{TH(–)}$ and $V_{TH(+)}$ through hysteresis control, before the next time dominant LED is on again.

Soft Start Timing

The soft-start function performs the following sequence of operation:

1. At startup, the boost stage initially switches at the minimum SW on-time continuously. This allows output voltage to build-up, even at the minimum PWM duty cycle.
2. The switch on-time increases as the COMP pin voltage starts to rise (the COMP voltage controls the boost stage switching duty cycle, which in turn controls the boost output voltage).
3. Soft start ramp duration is 100 ms, which allows the LED to cycle 10 times at a 100 Hz PWM frequency.
4. Soft start can finish earlier, either due to the LED current reaching regulation, or because output voltage reaches 90% of OVP.
5. To prevent output voltage from reaching 90% of OVP prematurely (while the COMP voltage is still too low), the design should ensure there is sufficient output capacitance, such that it takes longer to build up V_{OUT} at the minimum SW on-time.
6. During soft start, the PWM on-time needs to be at least 1.5 µs to guarantee reliable detection once LED current reached regulation. If the startup on-time is set lower (at 1 µs, for example), soft start may be terminated later when output reached 90% OVP level.

It is important not to set OVP level too much higher than the normal operating voltage of LED strings. In particular, make sure that:

$$V_{LED} + V_{REG} < V_{OVP} < V_{LED} + V_{REG} + V_{SD}$$

where V_{LED} is the worst-case/highest voltage drop across LED strings. V_{REG} is the LED pin regulation volatge (around 1 V). V_{SD} is the LED string short-detect threshold (programmable between 5 and 12 V).

For Boost configuration with 7 to 10 LEDs in series, OVP is typically set at ~5 V above the worst-case LED string voltage. For SEPIC configuration with lower number of LEDs in series, OVP may be set closer to the LED voltage.

Input Disconnect Switch

The A8522 has a gate driver for an external PMOS that can be used to provide an input disconnect protection function. During normal startup, the PMOS is turned on gradually to avoid large inrush current. In the event there is a direct short at the boost stage (either SW or VOUT shorted to GND), high input current will cause the PMOS to turn off.

The input disconnect current threshold is calculated by:

$$I_{INMAX} = V_{INS(TH)} / R_{INS} \quad (4)$$

where $V_{INS(TH)}$ = 105 mV (typ).

Under normal operation, the input current is protected by the cycle-by-cycle boost switch current limit. Only in case of a direct short at boost output or SW pin will the input disconnect switch be activated. Therefore the input disconnect current threshold is typically set slightly higher than the switch current limit. For example, choose R_{INS} = 0.02 Ω to set I_{INMAX} = 5.25 A approximately.

During normal power-up sequence, as soon as EN goes high, the GATE pin will start to be pulled low by a 115 µA (typ) current.

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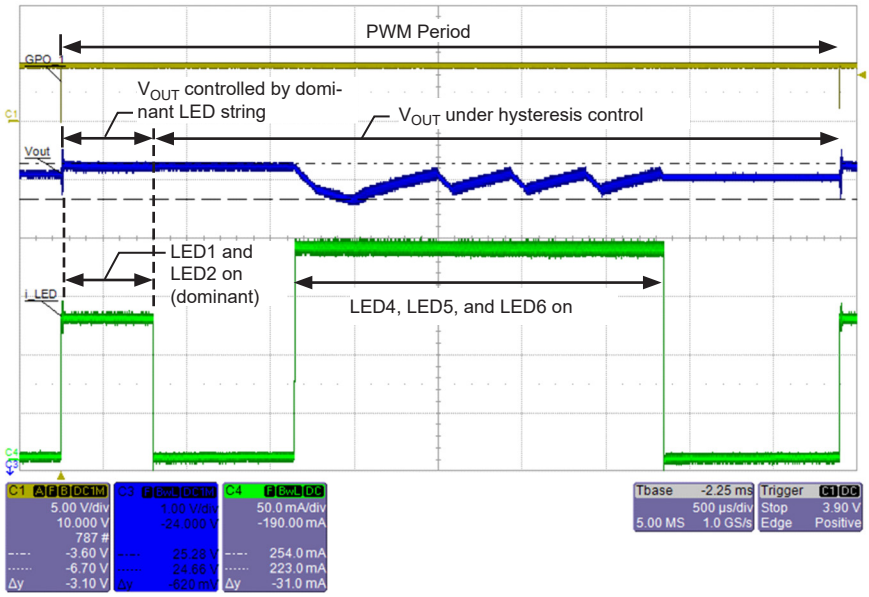
How quickly the external PMOS turns on depends on the gate capacitance, C_{GS}, of the PMOS. If the gate capacitance is very low, the inrush current may still exceed 5 A momentarily and trip the input disconnect protection. In this case, an external C_{GS} may be added to slow down the PMOS turn-on. A typical value of 10 nF should be sufficient in most cases.

When selecting the external PMOS, check for the following parameters:

- Drain-source breakdown voltage: $B_{VDSS} > -50$ V
- Gate threshold voltage: ensure it is fully enhanced at $V_{GS} = -4$ V, and cut-off at –1 V
- $R_{DS(on)}$: ensure the on-resistance is rated at $V_{GS} = -4.5$ V or similar, not at –10 V; derate it for higher temperatures

The PMOS gate voltage is clamped by the A8522 such that $V_{GS} = V_{IN} - V_{GATE} \leq 8$ V. This is to prevent the gate-source of external PMOS from breaking down due to higher input voltage. In case of very low input voltage, however, V_{GS} is limited by V_{IN}. Therefore it is important to select a PMOS with a lower gate threshold voltage.



Test conditions:

LED1 and LED2 = 8 series (dominant LED string),
LED4, LED5, LED6 = 7 series
All other channels disabled
60 mA each enabled channel
LED V_{REG} = 0.85 V
V_{IN} = 12 V
V_{OUT} hysteresis = 0.25 V

Scope traces:

C1 (Yellow) = V_{GPO1} PWM period (5 V/div)
C3 (Blue) = V_{OUT} (1 V/div, offset = 24 V)
C4 (Green) = Total I_{LEDx} (50 mA/div)
Time scale = 500 µs/div

A8522 evaluation PCB:

L_1 = 10 µH, C_{OUT5} = 68 µF / 50 V polymer electrolytic, C_{OUT4} = 2.2 µF / 50 V 1206 ceramic, R_Z = 10 kΩ, C_Z = 5.6 nF, C_P = 120 pF

Figure 7: Output Hysteresis Waveform, LED1 and LED2 are the Dominant Sring

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System Failure Detection and Protection

The A8522 is designed to detect and protect against a multitude of system-level failures. Some of those possible faults are illustrated in Figure 8 and the A8522 is described in Table 1.

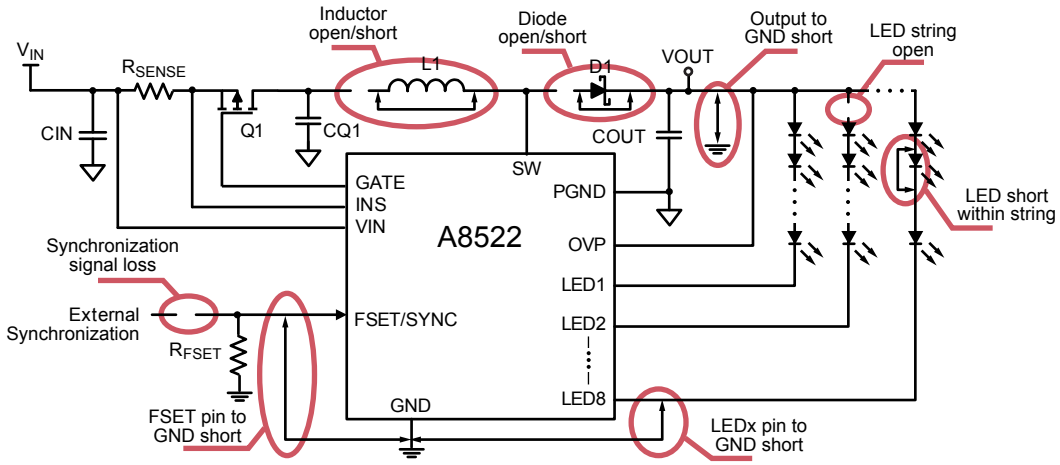

Figure 8: Examples of System Fault Modes

Table 1: System Failure Mode

Failure Mode	Symptom	Protected?	A8522 Response
Inductor open	Output undervoltage fault detected at startup	Yes	Will not proceed with startup
Inductor shorted	Excessive current through SW pin during switching, secondary OCP tripped	Yes	Shuts down and will not retry
Diode open	Excessive voltage detected at SW pin, secondary OVP tripped	Yes	Shuts down and will not retry
Diode shorted	Excessive current through SW pin during switching	Yes	Shuts down and will not retry
Output shorted to GND	Input overcurrent protection tripped at startup	Yes	Shuts off input power via input disconnect switch
LED string open or LEDx pin open	IC unable to detect LED current, output ramps up and trips OVP	Yes	Disable offending LED string, other strings continue to operate
LEDs shorted within one string	Excessive voltage drop at LEDx pin	Yes	Disable offending LED string, other strings continue to operate
LEDx pin to GND short at startup	Detected LED pin to GND short during startup error check	Yes	Will not proceed until fault is removed
LEDx pin to GND short during operation	IC unable to detect LED current, output ramps up and trips OVP	Yes	Shuts down and rechecks for pin to GND short before restart
FSET pin to GND short or FSET pin open	IC unable to start switching	Yes	Will not restart until fault is removed
External synchronization signal disconnected	Unable to detect logic signal at FSET pin	Yes	Falls back to switching frequency determined by R_{FSET}

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Fault Handling

The A8522 can detect and monitor 12 different fault modes internally. Some can be programmed for latching (flag set, system controller action required) or for auto restart after flag set and condition cleared. Faults are listed in Table 2.

In the event of a fault, registers 0x38 and 0x39 hold the fault status to allow the master to read what type of fault (such as OCP, OVP, open LED, and so forth) has been detected.

Internal State Monitoring

There are two general-purpose output pins, GPO1 and GPO2, that can be programmed to monitor selected internal status bits directly. This allows those pins to be used as special IRQ (interrupt request) lines for the system. The system can also monitor non-critical fault occurrences (such as temperature warning or SW current limit) while the IC continues to run. GPO1 and GPO2 are open-drain outputs, and an external pull-up resistor is required at each pin to set the logic-high level required.

LED Thermal Shutdown and Derating

The A8522 TSD (Thermal Shutdown) threshold is set to 170°C (typ). If the die temperature reaches the TSD threshold, boost and LED drivers are disabled. The IC will restart after the die temperature has fallen to 20° C below the TSD threshold.

The A8522 also has an optional thermal derating function controlled by a register bit. The LED derating bit enables or disables the Thermal Derating feature, which cuts-back on LED current when the die temperature gets too close to the thermal shutdown threshold. When enabled, the LED current starts decreasing as die temperature rises above 20°C from TSD. The Thermal Derating feature is disabled by default, which means the IC will continue to operate at full LED current until the TSD threshold is reached. Current derating is illustrated by Figure 9.

LED Pin Short to GND Check Before Startup

When the IC is enabled for the first time, it checks to determine if any LED pins are shorted to GND and/or are not used (LED string not populated). An internal 60 µA current source pulls all LED pin voltages high. Any LED pin with voltage below 120 mV is considered shorted to GND. Any LED pin with voltage above 270 mV is considered in use (see Figure 9). If any LED channel is unused, that LED pin must be connected to GND through a 4.7 kΩ resistor (note: there is an internal gated parallel resistor of 8 kΩ, so the combined sense resistance is 3 kΩ). The user can further disable any LED channel through I²C programming. All unused LED channels are taken out of regulation at this point and will not contribute to the boost regulation loop. If any LED pin is shorted to ground, the IC will not proceed with soft start until the short is removed for the LED pin. This prevents the A8522 from powering up and putting an uncontrolled amount of current through the LEDs.

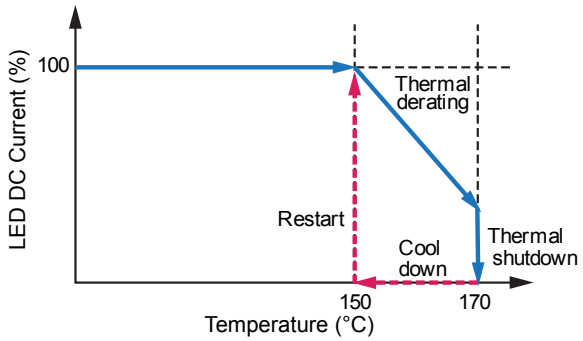

Figure 9: Thermal Derating and Shutdown Protection Features

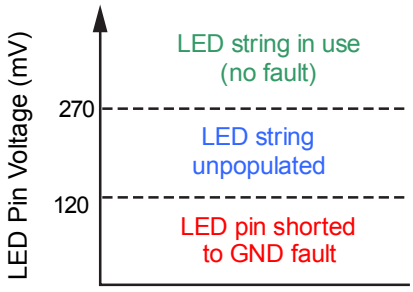

Figure 10: A8522 LED Short-to-GND Check Before Startup

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LED Pin Open/Short Fault During Normal Operation

During startup and normal operation, all enabled LED channels are supposed to ramp up in current until each channel regulation target is reached. If any channel is below regulation, it will request the boost output voltage to rise, so the higher voltage can help more current to flow through its LED string. But in the event that an LED pin is either open or shorted to ground, there can be no current flowing through its LED driver. The boost voltage will continue to rise until the OVP fault is tripped.

This function is used in conjunction with general fault 8 (overvoltage protection), so it can be monitored by the I²C master. When this bit is set to 0, the corresponding LED channel is within regulation and operating correctly (or the LED channel has been previously disabled). When the OVP fault is tripped the bit is set to 1.

When the OVP fault is tripped, any enabled LED channel that is not in regulation is tested for ground-short again:

- If an unregulated channel is shorted to ground, the boost stage is shutdown completely and will not attempt auto-restart. This is to prevent uncontrolled current from flowing through the LED string. Fault flag is set to signal an LED to GND short fault (#11). The corresponding bit in the LED Pin Shorted to GND status register is set. The user can then read this register to determine which LED channel is shorted.
- If an unregulated channel is not shorted to ground, the IC will remove the offending channel from regulation, and resume normal operation for other channels. The $\overline{\text{FLAG}}$ pin (which was previously set to signal an OVP fault) is then cleared. The corresponding bit in the Latched Status LEDs in Regulation registers (0x3A and 0x3B) is set. The user can then read this register to determine which LED channel is open.

Note:

If the OVP level is programmed too low in the OVP Threshold register for the LED string with highest forward voltage, the LED driver may not be able to reach regulation during startup. In this case, the IC will treat the LED pin as open. The offending LED pin is removed from regulation and the rest of the LED channels will resume normal operation.

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Table 2: Internal Fault Modes

Number and Name	Default Action	Programmable?	Input Disconnect Switch	Boost Switch	LED Current	$\overline{\text{FLAG}}$ Set on Fault?
Fault 1 Input Overcurrent	Latched	No	Off	Off	Off	Yes
	This fault is set when an input overcurrent has been detected ($V_{IN} – V_{INS}$ > 100 mV). The input disconnect switch is disabled, as well as the boost stage and LED drivers. The fault flag is latched at low. To reenable the part, the EN pin must be cycled.					
Fault 2 Output Undervoltage	Auto Restart	Yes	On	Off	Off	Yes
	The IC monitors the output voltage on the OVP pin. If the voltage level drops below output undervoltage threshold, V_{UVP} (such as in case of output shorted to GND), the fault will be registered. The boost SW and LED drivers are shut down.					
Fault 3 Temperature Warning	Auto Restart	Yes	On	On	Reduced	No
	This is a warning that the IC is approaching thermal shutdown. Typically this fault is asserted at 20°C below TSD, and LED current is reduced. As soon as the IC cools down, the fault bit will reset.					
Fault 4 Overtemperature Protection	Auto Restart	No	On	Off	Off	Yes
	Fault occurs when the die temperature exceeds the TSD (thermal shutdown) threshold, typically 170°C.					
Fault 5 FSET Short Protection	Auto Restart	Yes	On	Off	Off	Yes
	Fault occurs when the FSET/SYNC current exceeds approximately 180 µA (≈150% of maximum current). The boost will stop switching, and the IC will disable the LED sinks until the fault is removed.					
Fault 6 SW Primary Current Limit	Auto Restart	No	On	Truncated	On	No
	The device monitors its switch current on a cycle-by-cycle basis, and shuts the switch off for the existing cycle if the current exceeds $I_{SW(LIM)}$. Normal switching continues in the next cycle. This fault does not shut down the IC.					
Fault 7 SW Secondary Current Limit	Latched	No	Off	Off	Off	Yes
	When the current through the boost SW pin exceeds secondary current limit ($I_{SWLIM(sec)}$), the part will immediately shut down the input disconnect switch, LED drivers, and boost. To restart the part, either cycle the power or toggle the EN pin.					
Fault 8 Overvoltage Protection	Auto Restart	Yes	On	Off	On	Yes
	Fault occurs when the OVP pin exceeds the $V_{OVP(th)}$ threshold. Case 1. All enabled LED strings are in regulation. The IC will immediately stop boost switching. LED current sinks remain active to drain the output voltage. After the output voltage falls below approximately 94% of the OVP threshold, the IC will resume switching to regulate the output voltage. Case 2. One (or more) enabled LED string is not in regulation. See Fault 11.					
Fault 9 Open Diode Protection	Latched	No	Off	Off	Off	Yes
	Secondary overvoltage protection at the SW pin is used for open diode detection. When diode D1 opens up, the SW pin voltage will increase until $V_{OVP(sec)}$ is reached. The input disconnect switch is disabled, as well as the boost stage and LED drivers. The $\overline{\text{FLAG}}$ pin is pulled low only while the overvoltage condition exists. To restart the part, either cycle the power or toggle the EN pin.					
Fault 10 LED Pin Shorted to GND During Startup	Auto Restart	Yes	On	Off	Off	Yes
	The system at power-up checks if an LED pin is shorted to GND (see the LED Pin Short to GND Check before Startup section for details). If any pin is shorted, the system will not power up and the fault flag will be set.					
Fault 11 LED Pin Shorted to GND During Normal Operation	Latched	Yes	On	Off	Off	Yes
	This fault occurs when the LED pin is not in regulation and the output reaches OVP. At this time, the system removes LED from the regulation loop, allowing the high output voltage to fall. After this LED is disabled, the IC will determine whether the LED pin is shorted to GND or open (see the LED Pin Open/Short Fault during Normal Operation section for details). If the LED pin is open, the IC will continue to operate with the offending LED turned off. If LED pin is shorted to GND, the IC will shut down and latch off. To restart the part, either cycle the power or toggle the EN pin.					
Fault 12 LED String Short Detect	Auto Restart	Yes	On	On	On*	Yes
	This fault is set if any LED pin voltage goes above its LED Short-Detect Threshold (set by corresponding programmable register bits). The offending LED driver is disabled immediately. Other LED strings will continue to work as normal. At the next PWM cycle, the offending LED driver is checked again and may resume operation if the fault has been removed (unless the Auto-restart bit is turned off).					

*Only the offending LED driver is turned off. All other enabled LED drivers continue to work as normal.

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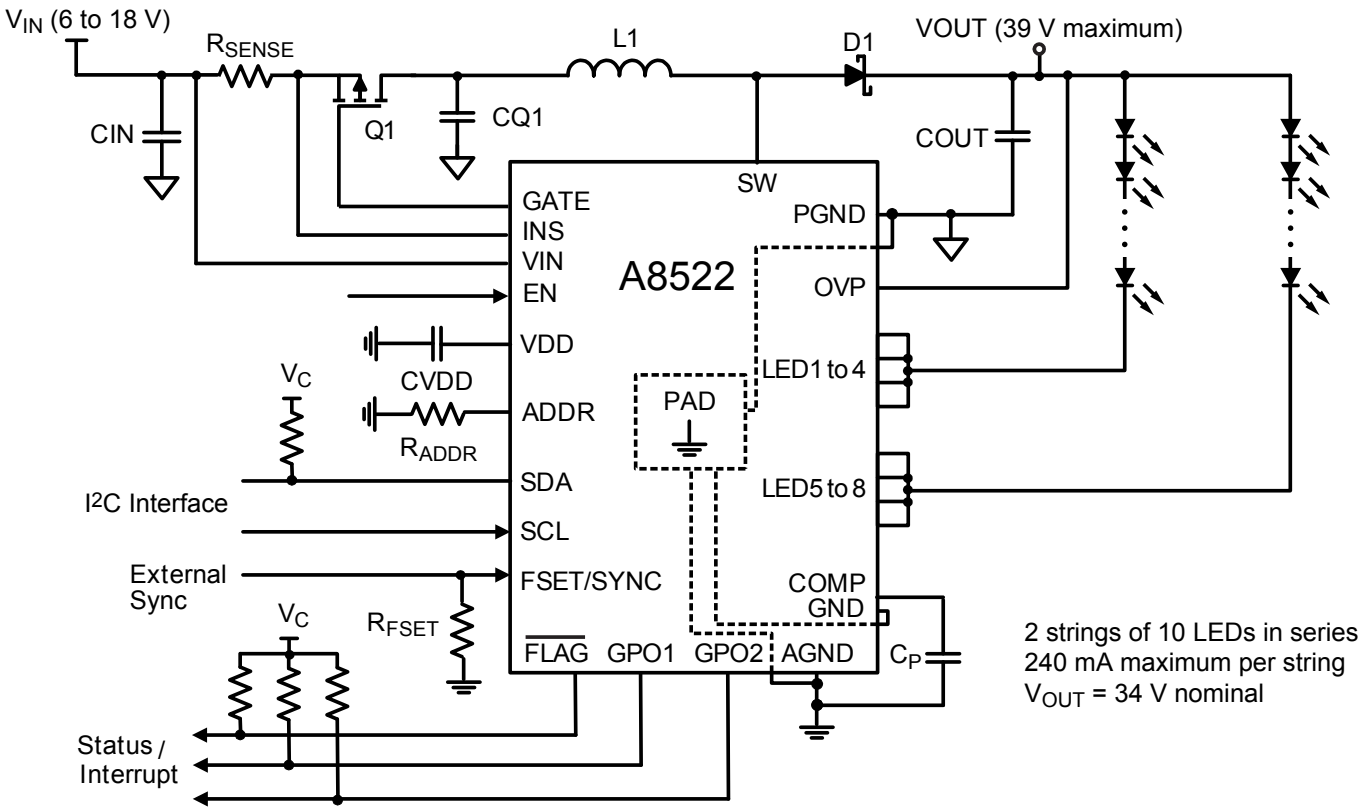
APPLICATION INFORMATION

Typical Applications

The A8522 is highly flexible and supports a wide range of application system configurations. Three example application configurations are described in this section:

- Application A. Driving two high-current, balanced LED strings
- Application B. Driving unbalanced LED strings
- Application C. SEPIC converter



Application A: Circuit Diagram Showing the A8522 with Optional Input Disconnect Switch.

LED current sinks are combined to drive two high-current LED strings. Unused LED pins are connected to GND through 4.7 kΩ resistors. As long as the two LED strings are well-balanced, the heat dissipation from the LED current sources (LED1 through LED4 and LED5 through LED8) can be minimized.

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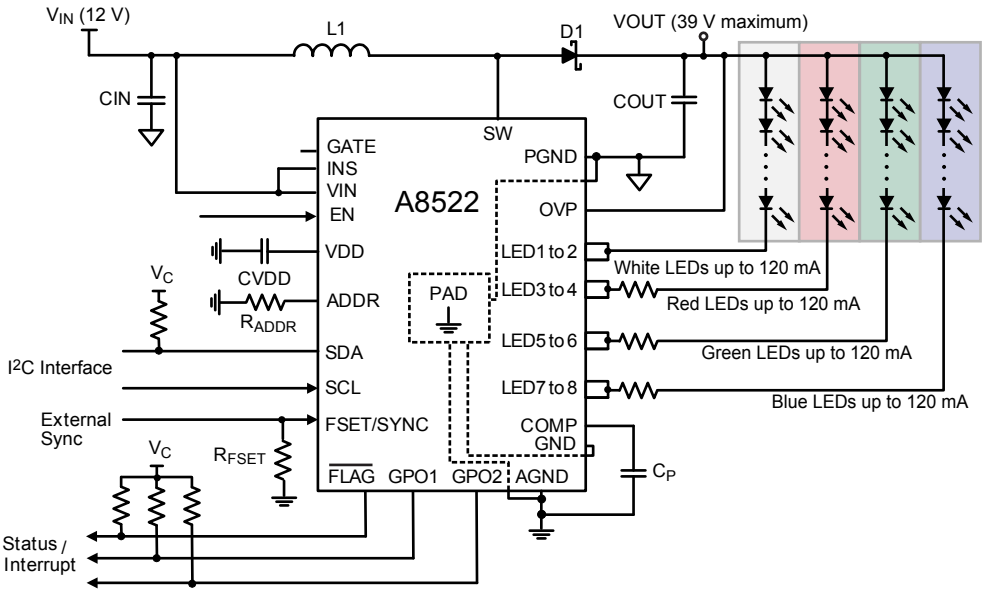
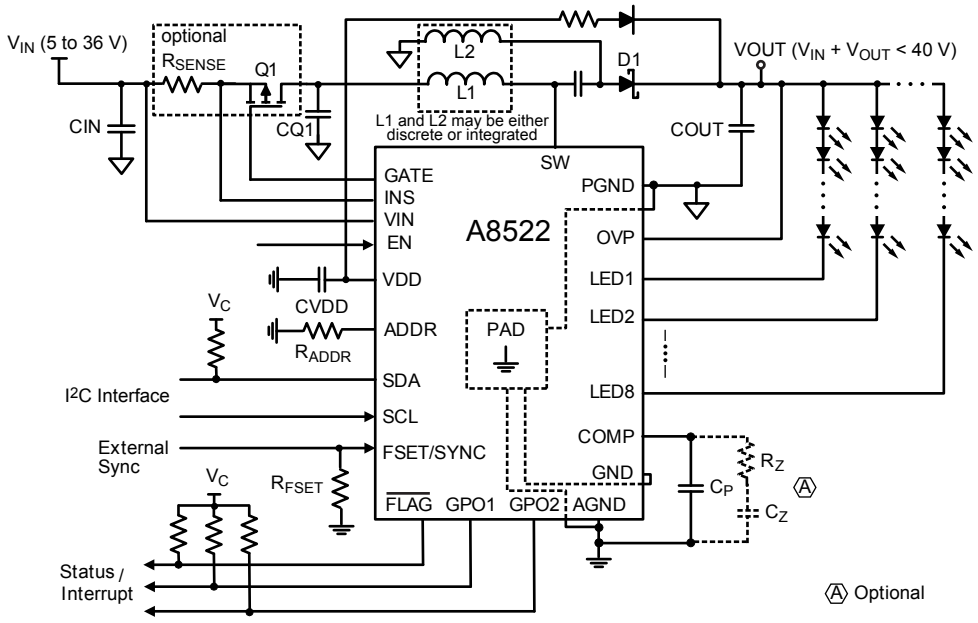


Application B: Circuit Diagram Showing the A8522 Used to Drive Four Unbalanced LED Strings: Separate Strings for White, Red, Green, and Blue LEDs.

The white LED string is assumed to have the greatest current and voltage drops across the LEDs. To reduce the power dissipation at other LED current sinks (LED3 through LED8), ballast resistors may be inserted into the LED strings to dissipate part of the heat externally. LED channels for each string should be grouped by programming the Polyphase register.



Application C: The A8522 can be used in a SEPIC (Single-Ended Primary Inductor Converter) Configuration.

The main advantage of SEPIC is that output voltage can be either higher or lower than the input voltage. In contrast, the output voltage of a boost converter must be higher than the input. One limitation of SEPIC configurations is that the voltage stress across SW is higher than for boost converters:

- For boost: $V_{SW} = V_{OUT}$
- For SEPIC: $V_{SW} = V_{IN} + V_{OUT}$

Therefore care must be taken to ensure that $V_{IN} + V_{OUT} < 40$ V for a SEPIC configuration.

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Design Example

This section provides a method for selecting component values when designing an application using the A8522. The results are diagrammed in the schematic shown in figure 10 at the end of this design example.

The following requirements are considered for this design example:

- V_{IN}: 10 to 14 V
- Quantity of LED channels (strings), n: 8
- Quantity of series LEDs per channel, nsl: 7
- LED current per channel, I_{LED}: 60 mA
- LED voltage drop, V_f: 3 V at 60 mA
- Boost diode forward voltage,V_d: 0.4 V
- f_{SW}: 2 MHz
- PWM dimming frequency: 200 Hz at 100% duty cycle
- Polyphase feature is turned on
- At 12 V and 60 mA/channel, the IC case temperature rise is measured to be 30°C. At lower V_{IN}, the IC case and junction temperature rise will increase. Therefore, if proper cooling is not applied, output current derating would be required.

STEP 1: Determining the output voltage. The output voltage is determined by the following equation:

$$V_{OUT} = nsl \times V_f + V_{LED} + 0.45\ (V)\ . \qquad (5)$$

The regulated V_{LED} is 0.85 V. The fixed 0.45 V is related to the output-implemented voltage hysteresis control. During PWM dimming on-time, V_{LED} is regulated to 0.85 V. During PWM dimming off-time, the output voltage hysteresis control is 0.45 V. Substituting into equation 5:

$$V_{OUT} = 7 \times 3\ (V) + 0.85\ (V) + 0.45\ (V) = 22.3\ V\ .$$

STEP 2: Determining the OVP threshold limit. This is the maximum voltage based on the LED requirements. The regulation voltage, V_{LED}, of the A8522 is 0.85 V. A constant term, 5 V, is added to give some margin to the design:

$$V_{OUT(OVP)} = nsl \times V_f + V_{LED} + 0.45\ (V) + 5\ (V). \qquad (6)$$

Substituting into equation 6:

$$V_{OUT(OVP)} = 7 \times 3\ (V) + 0.85\ (V) + 0.45\ (V) + 5\ (V) = 27.3\ V\ .$$

In the OVP Threshold register (0x04), set the OVP threshold to 28 V.

STEP 3: At this point, a quick check should be done to determine if the conversion ratio is acceptable for the selected frequency. First, determine the maximum duty cycle:

$$D_{MAX} = 1 - t_{SWOFFTIME}(max) \times f_{SW}\ , \qquad (7)$$

where $t_{SWOFFTIME}$(max), 85 ns, is found in the datasheet. Substituting into equation 7:

$$D_{MAX} = 1 - (0.085\ (\mu s) \times 2\ (MHz)) = 0.83\ .$$

Then the theoretical maximum voltage, V_{OUTMAX}, is calculated as:

$$V_{OUTMAX} = [V_{INMIN} / (1 - D_{MAX})] - V_d\ , \qquad (8)$$

where V_d is the boost diode forward voltage. Substituting into equation 8:

$$V_{OUTMAX} = [10\ (V) / (1 - 0.83)] - 0.4\ (V) = 58.42\ V\ .$$

The theoretical maximum voltage value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, the switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirements.

STEP 3: Selecting the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applications due to stringent EMI requirements the system must operate in continuous conduction mode (CCM) at least throughout the normal selected input voltage range and nominal output current.

STEP 3a: Determining the maximum operating duty cycle in CCM. The duty cycle is calculated as follows:

$$D_{CCM(MAX)} = 1 - V_{INMIN} / (V_{OUT(OVP)} + V_d)\ , \qquad (9)$$

and substituting into equation 9:

$$D_{CCM(MAX)} = 1 - 10(V) / (28\ (V) + 0.4\ (V)) = 0.65\ .$$

STEP 3b: Determining the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum input current will dictate the current rating of the inductor.

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First, calculate the maximum input current. The input current is output-determined, so:

$$I_{OUT} = n \times I_{LED} , \quad (10)$$

given I_{LED} = 60 mA, substituting into equation 10:

$$I_{OUT} = 8 \times 0.060\ (A) = 0.48\ (A) .$$

I_{OUT} can be used to calculate the maximum input current:

$$I_{INMAX} = (V_{OUT(OVP)} \times I_{OUT}) / (V_{INMIN} \times \eta) , \quad (11)$$

where η is the efficiency value, which can be obtained from efficiency curves in this datasheet (at f_{SW} = 2 MHz). It is approximately 80% under these conditions. Substituting into equation 11:

$$I_{INMAX} = (28\ (V) \times 0.48\ (A)) / (10\ (V) \times 0.8) = 1.68\ A .$$

Similarly, calculate the minimum input current:

$$I_{INMIN} = (V_{OUT} \times I_{OUT}) / (V_{INMAX} \times \eta) , \quad (12)$$

where V_{OUT} is determined by equation 5, and η is the efficiency value, which can be obtained from efficiency curves in this datasheet (at f_{SW} = 2 MHz). It is approximately 85% under these conditions. Substituting into equation 12:

$$I_{INMIN} = (22.3\ (V) \times 0.48\ (A)) / (14\ (V) \times 0.85) = 0.90\ A .$$

STEP 3c: Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor must be set such that the $^1/_2$ inductor ripple current is not greater than the average minimum input current:

$$\Delta I_L = I_{INMAX} \times k_{ripple} . \quad (13)$$

A practical starting point is to consider k_{ripple} to be 40% of the maximum inductor current. Substituting into equation 13:

$$\Delta I_L = 1.68\ (A) \times 0.4 = 0.67\ A$$

The inductor value can then be calculated as:

$$L_1 = V_{INMIN} / (\Delta I_L \times f_{SW}) \times D_{CCM(MAX)} . \quad (14)$$

where $D_{CCM(MAX)}$ is calculated as in equation 9. Substituting into equation 14:

$$L_1 = 10\ (V) / (0.67\ (A) \times 2\ (MHz)) \times 0.65 = 4.85\ \mu H$$

Double-check to make sure that the $^1/_2$ inductor ripple current is less than I_{INMIN}, by applying equations 12 and 13:

$$I_{INMIN} > (1/2) \times \Delta I_L$$

$$0.90 > 0.34\ A .$$

For lower ripple current, smaller output capacitor, and higher efficiency, we selected the inductor value to be 10 µH.

STEP 3d: This step is used to verify that there is sufficient slope compensation for the chosen inductor.

The ripple current when L = 10 µH is given by:

$$\Delta I_{Lused} = (V_{INMIN} \times D_{CCM(MAX)}) / (L_{used} \times f_{SW}) . \quad (15)$$

Substituting into equation 15:

$$\Delta I_{Lused} = (10\ (V) \times 0.65) / (10\ (\mu H) \times 2.0\ (MHz)) = 0.325\ A .$$

The minimum required slope compensation is proportional to the switching frequency and it is given by:

$$S_{E(MINREQ)} = \frac{\Delta I_{Lused} \times (\Delta s \times 10^{-6})}{\left(\frac{1}{f_{SW}}\right) \times (1 - D_{CCM(MAX)})} \quad (16)$$

where Δs is taken from Riddley's formula:

$$\Delta s = 1 - 0.18 / D_{CCM(MAX)} \quad (17)$$

$$= 1 - 0.18 / 0.65 = 0.723 .$$

Substituting into equation 16:

$$S_{E(MINREQ)} = \frac{0.325\ (A) \times (0.723 \times 10^{-6})}{\left(\frac{1}{2.0\ (MHz)}\right) \times (1 - 0.65)}$$

$$= 1.34\ A/\mu s$$

At 2 MHz switching frequency, 2.3A/µs slope compensation is implemented in the A8522 (programmable through the I²C interface). If the implemented value is less than the figure calculated using equation 16, then the inductor value must be increased.

STEP 3e: Determining the inductor current rating. The minimum inductor current rating can be calculated as follows:

$$I_{LMIN} = I_{INMAX} + {}^1/_2 \times \Delta I_L \quad (18)$$

$$= 1.68\ (A) + 0.325\ (A) / 2$$

$$= 1.84\ A$$

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The inductor current rating should be higher than 2.26 A. Because the converter must operate properly until OCP is triggered, it is recommended to select the inductor current rating to be same as the OCP limit, which is 3.8 A. An inductor current rating of 4 A is good.

STEP 4: Selecting the switching frequency. The switching frequency is set by the resistor connected from the FSET/SYNC pin to GND. Using the component values from figure 2, to operate at a 2 MHz switching frequency R_{FSET} should be 10 kΩ.

STEP 5: Choosing the output boost Schottky diode. The Schottky diode must be chosen taking the following four characteristics into account when it is used in LED lighting circuitry:

- Current rating
- Reverse voltage
- Leakage current
- Reverse recovery charge

Current Rating – The diode should be able to handle the same peak current as the inductor:

$$I_{dp} = I_{INMAX} + \Delta I_{Lused} / 2 \quad (19)$$
$$= 1.68\ (A) + 0.325\ (A) / 2$$
$$= 1.84\ A$$

Reverse Voltage – The reverse voltage rating should be larger than the maximum output voltage. In this case, it is $V_{OUT(OVP)}$.

Leakage Current – The third major component in deciding the boost Schottky diode is the reverse leakage current characteristic. This characteristic is especially important when PWM dimming is implemented. During PWM off-time, the boost converter is not switching. This results in a slow bleeding off of the output voltage due to leakage currents. Leakage current can be a large contributor especially at high temperatures. For the diode that was selected in this design, the leakage current varies between 1 and 100 µA.

Reverse Recovery Charge – For higher efficiency, the reverse recovery charge should be as small as possible. This charge and the boost switch output capacitor charge are the contributors for the boost turn-on loss. This turn-on loss at high output voltage and high switching frequency becomes significant. A Vishay Schottky diode SS2PH10 2A 100V is selected for this design.

STEP 6: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. In addition, the output capacitors should be big enough to hold and maintain the output voltage within acceptable voltage ripple range during PWM dimming off-time. The major contributor is the leakage current, I_{LK}. This current is the combination of the OVP sense, as well as the leakage current of the Schottky diode. In this design, the PWM dimming frequency is 200 Hz and the minimum PWM dimming duty cycle is 0.02%. Typically, the voltage variation on the output during PWM dimming should be less than 0.5 V so that no audible hum can be heard.

The selected diode leakage current at a 150°C junction temperature and 30 V output is 100 µA, and the leakage current through OVP pin is 30 µA. The total leakage current can be calculated as follows:

$$I_{lk} = I_{LKG(diode)} + I_{LKGOVP} \quad (20)$$
$$= 100\ \mu A + 30\ \mu A$$
$$= 130\ \mu A$$

To accommodate this, the output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{lk} \times (1 - D_{MIN})}{f_{SW(PWM)} \times V_{COUT}}$$
$$= \frac{130\ (\mu A) \times (1 - 0.02)}{200\ (Hz) \times 0.450\ (V)} \quad (21)$$
$$= 1.42\ \mu F$$

where D_{MIN} is the minimum dimming duty cycle and $f_{SW(PWM)}$ is the PWM dimming frequency.

A capacitor larger than 1.42 µF should be selected. It should be noted that the ceramic capacitor value is reduced with DC voltage bias. The capacitance value at 30 V output may drop by 40%. 4.7 µF and 2.2 µF, 50 V ceramic capacitors are good choice for

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this design:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

It is also necessary to note that, if a high dimming ratio of 5000:1 must be maintained at lower input voltages, then larger output capacitors will be needed.

The rms current through the capacitor is given by:

$$C_{OUTrms} = I_{OUT} \times \sqrt{\frac{D_{CCM(MAX)} + \frac{\Delta I_{Lused}}{I_{INMAX} \times 12}}{1 - D_{CCM(MAX)}}} \quad (22)$$

$$= 0.6\ (A) \times \sqrt{\frac{0.65 + \frac{0.325\ (A)}{2.1\ (A) \times 12}}{1 - 0.65}}$$

$$= 0.826\ A$$

The output capacitor must have a current rating of at least 0.826 A. The capacitors selected in this design have a combined current rating of 3 A.

STEP 7: Selecting the input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple, ΔV_{IN}, to be 1% of the minimum input voltage. To accommodate this, the input capacitance can be calculated as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}}$$

$$= \frac{0.325\ (A)}{8 \times 2\ (MHz) \times 0.1\ (V)} \quad (23)$$

$$= 0.203\ \mu F$$

The rms current through the capacitor is given by:

$$C_{INrms} = I_{OUT} \times \frac{\frac{\Delta I_{Lused}}{I_{INMAX}}}{(1 - D_{CCM(MAX)}) \times \sqrt{12}} \quad (24)$$

$$= 0.6\ (A) \times \frac{\frac{0.325\ (A)}{2.1\ (A)}}{(1 - 0.65) \times \sqrt{12}}$$

$$= 0.076\ A$$

4.7 µF and 2.2 µF, 50 V ceramic capacitors are good choice for this design:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

If long wires are used for the input, it is necessary to use a much larger input capacitor. A larger input capacitor is also required to have stable input voltage during line transients.

STEP 8: Choosing the input disconnect switch components. Choose a P-channel MOSFET disconnect switch with current rating the same or higher than the IC trip threshold current limit, Set the limit to be 5 A.

The IC trip current limit, I_{LIM}, can be set by the input current sense resistor. When the IC detects $V_{INSTRIP}$, 150 mV (typ), across the input current sense resistor, it turns off the disconnect switch. The sense resistor value can be calculated as follows:

$$R_{SENSE} = V_{INSTRIP} / I_{LIM} \quad (25)$$

$$= 0.105\ (V) / 5\ (A)$$

$$= 0.021\ \Omega$$

A 18 mΩ / 0.5 W, 1206 resistor is selected. Therefore, the actual current limit is calculated by rearranging equation 25:

$$I_{LIM} = 0.105\ V / 0.018\ \Omega = 5.8\ A$$

The AO4421 6.2 A / 60 V P-channel MOSFET is selected.

STEP 9: Selecting the ADDR pin resistor value. Use a 0 Ω resistor to address 100 0000.

STEP 10: Selecting the VDD pin capacitor value. To get proper high frequency noise attenuation, use a 1 µF / 10 V X7R ceramic capacitor.

STEP 11: Selecting the $\overline{\text{FLAG}}$, GPO1, and GPO2 pull-up resistors. For each of these output pins, use a 10 kΩ resistor to V_{CC}.

STEP 12: Selecting the output LEDs. High power white 3000 K 85 CRI Duris E5 (LCW JDSHEC-EUFQ-5R8T-1) LEDs were selected.

STEP 13: Selecting CQ1 , placed from the drain of Q1 to GND. The purpose of this capacitor is to absorb the negative spike generated by L1 when the input disconnect switch is turned off. Use a small value such as 1 µF / 50 V ceramic. A large value may trip OCP during startup or a fast VIN transient.

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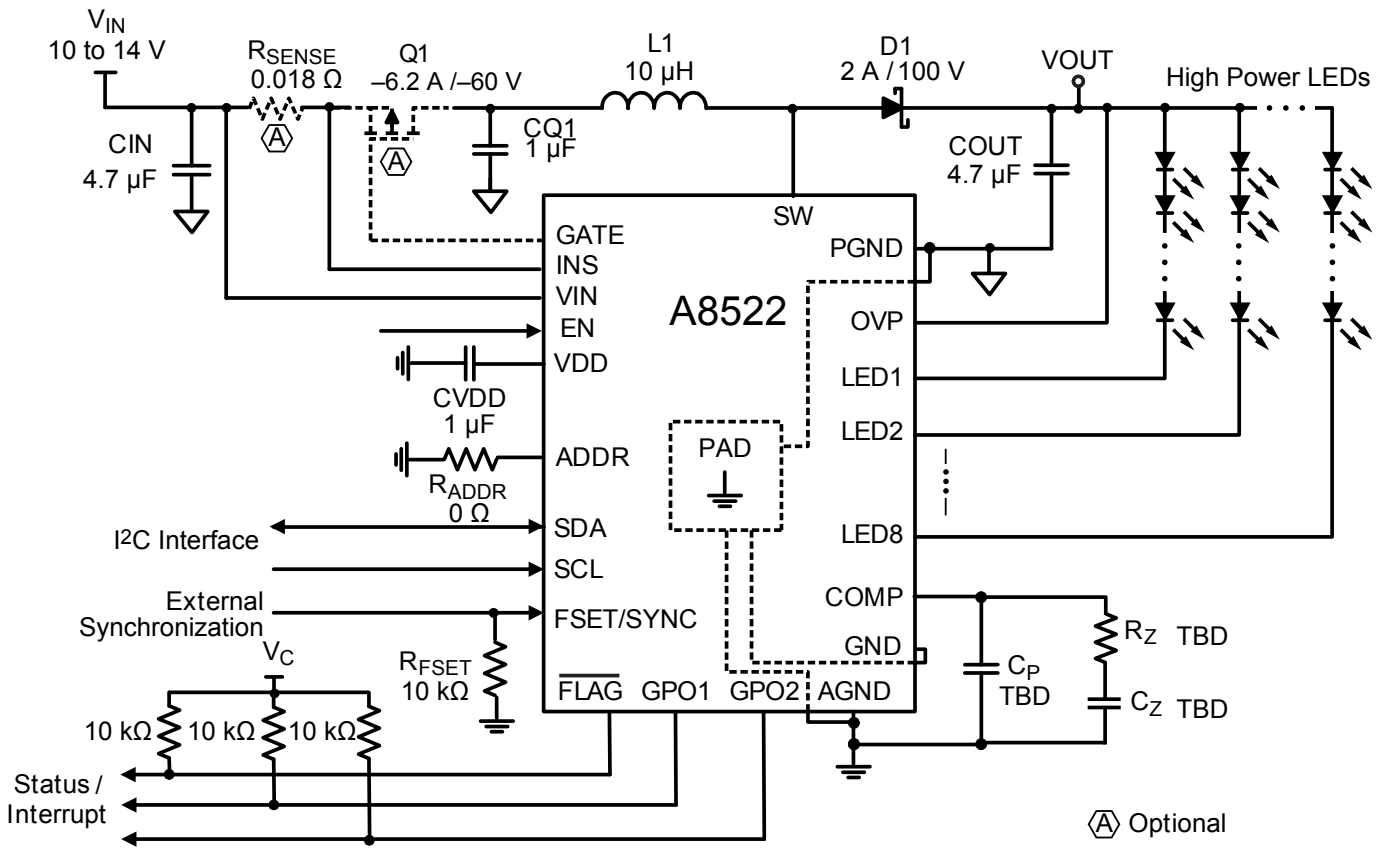

Figure 11: Schematic Diagram Showing Calculated Components from the Above Design Example

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PACKAGE OUTLINE DESIGN

For Reference Only – Not for Tooling Use

(Reference MO-153 AET)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

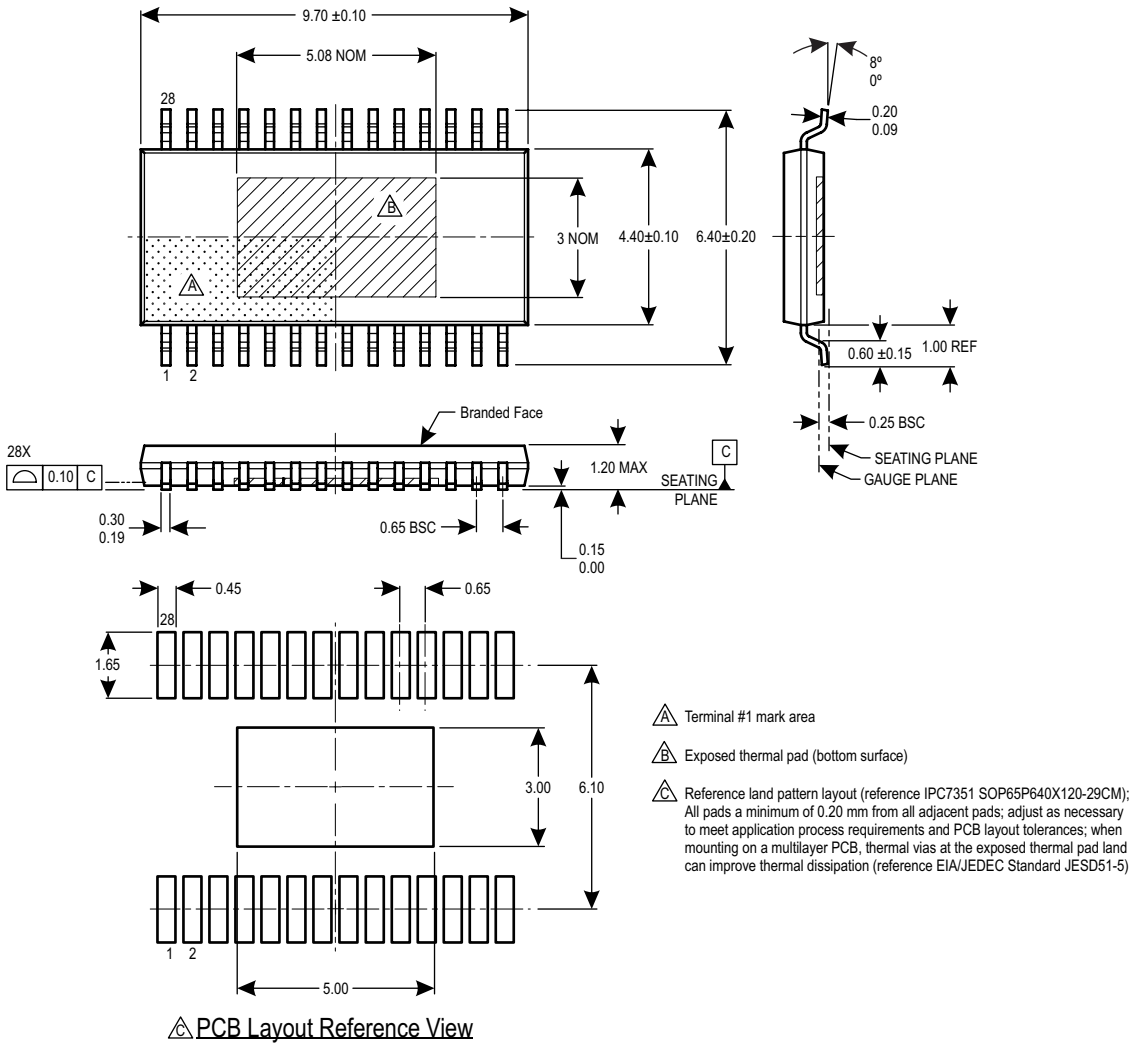

Figure 12: Package LP, 28-Pin TSSOP with Exposed Thermal Pad

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APPENDIX A: PROGRAMMING INFORMATION

The I²C registers are setup in clusters. Each cluster has an 8-bit register in a group which is called register bank (RB).

The I²C interface communicates with the system via separate read and write registers, as shown in Figure A-1.

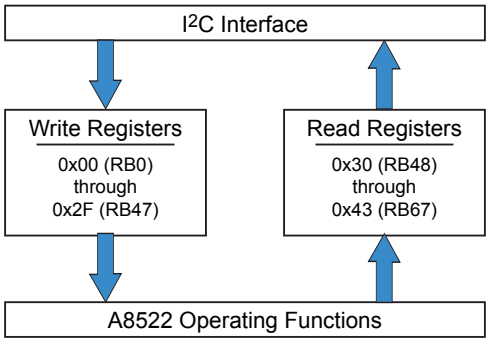

Figure A-1: I²C Interface Communication Structure

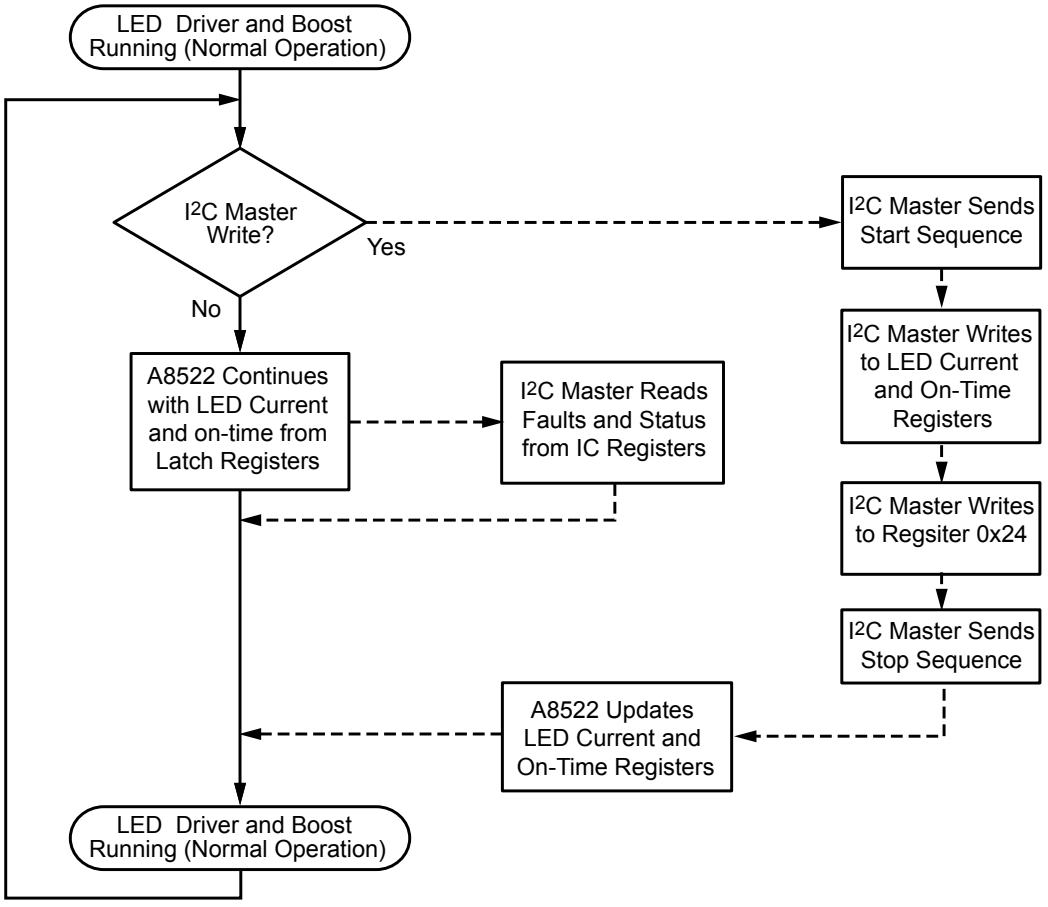

Figure A-2: I²C Interface During Normal Operation

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I²C Interface Description

The A8522 provides an I²C-compliant serial interface that exchanges commands and data between a system microcontroller (master) and the A8522 (slave). Two bus lines, SCL and SDA, provide access to the internal control registers. The clock input on the SCL pin is generated by the master, while the SDA line functions as either an input or an open drain output for the A8522, depending on the direction of the data flow.

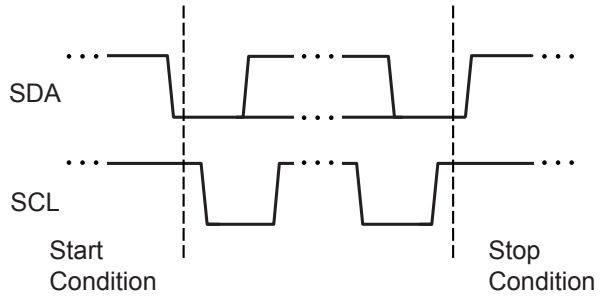
The I²C input thresholds depend on the V_{DD} voltage of the A8522. The threshold levels across the operating V_{DD} range are compatible with 3 V logic.

TIMING CONSIDERATIONS

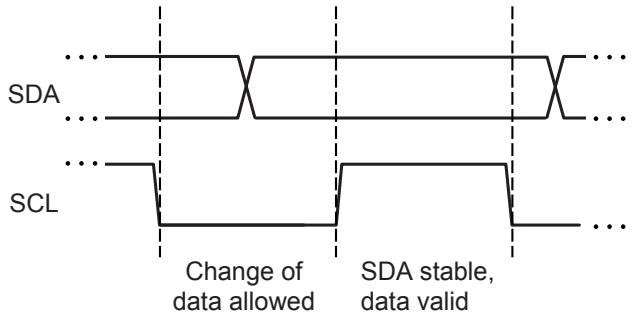
I²C communication is composed of several steps, in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high (see Figure A-3).
2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit (see Figure A-4).
3. Data Cycles. Reading or writing 8 bits of data followed by an acknowledge bit (see Figure A-4).
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high (see Figure A-3).

It is possible for the Start or Stop condition to occur at any time during a data transfer. The A8522 always responds by resetting the data transfer sequence. Except to indicate a Start or Stop condition, SDA must be stable while the clock is high (Figure A-3). SDA can only be changed while SCL is low.



(A) Start and Stop Conditions



(B) Clock and Data Bit Synchronization

Figure A-3: Bit Transfer on the I²C Bus

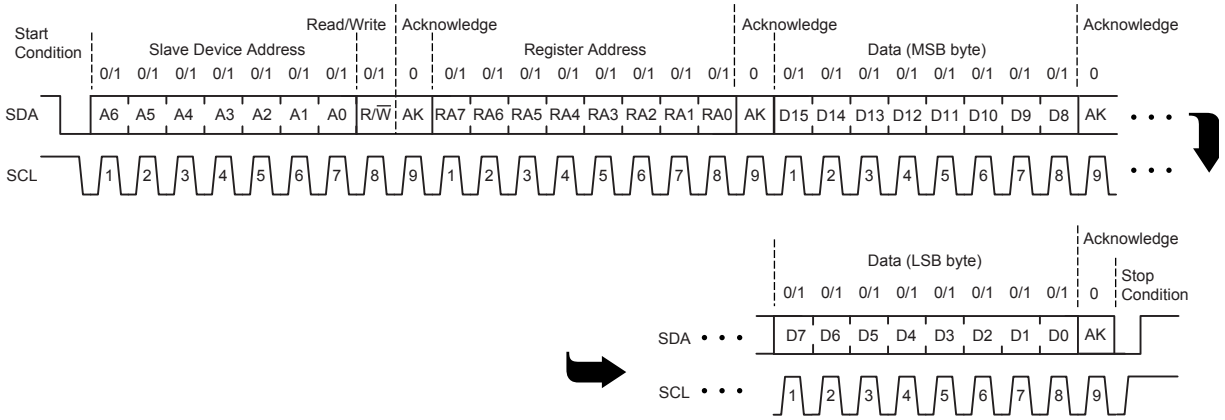


Figure A-4: Complete Data Transfer Pulse Train

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The state of the Read/Write bit (R/$\overline{W}$) is set low to indicate a Write cycle and set high to indicate a Read cycle.

The master monitors for an acknowledge bit to determine if the slave device is responding to the address byte sent to the A8522. When the A8522 decodes the 7-bit address field as a valid address, it acknowledges by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A8522 pulls SDA low during the clock cycle that follows each data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow the handshaking to occur.

I²C COMMAND WRITE TO THE A8522

The master controls the A8522 by programming it as a slave. To do so, the master transmits data bits to the SDA input of the A8522, synchronized with the clocking signal the master transmits simultaneously on the SCL input (Figure A-5).

A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). Between these points, the master transmits a pattern of address bits with a Write command bit (R/$\overline{W}$), then the register

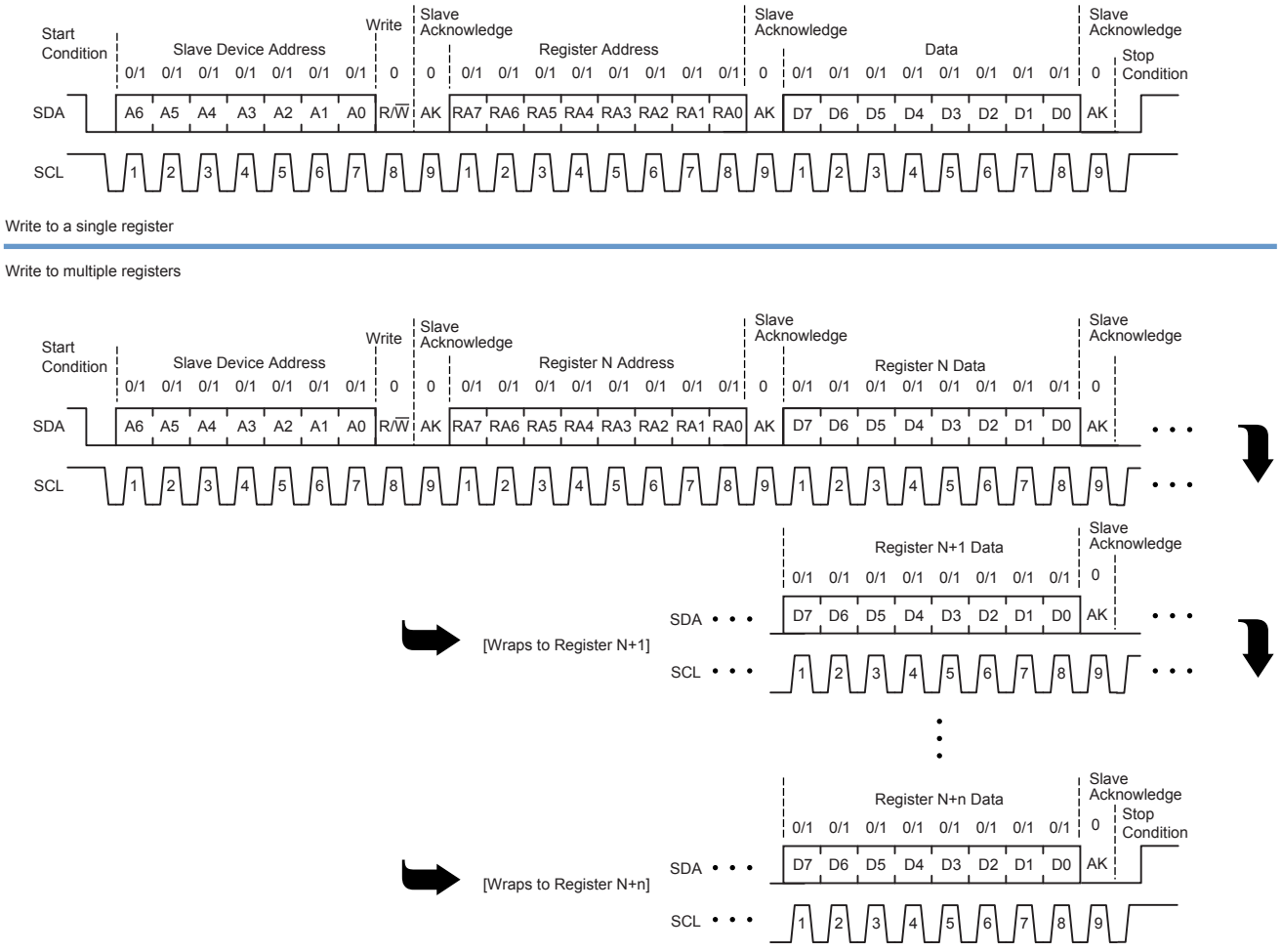

Figure A-5: Writing to Single and to Multiple Registers

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address, and finally the data. The address therefore consists of two bytes, comprised of the A8522 chip address, with the write enable bit, followed by the address of the individual register.

After each byte, the slave A8522 acknowledges by transmitting a low to the master on the SDA line. After writing data to a register the master must provide a Stop bit if writing is completed. Otherwise, the master can continue sending data to the device and it will automatically increase the register value by one for additional data byte. This allows faster data entry but restricts the data entry to sequential registers.

I²C COMMAND READ FROM THE A8522

The master can read back the register values of the A8522. The Read command is given in the R/$\overline{W}$ bit of the address byte. To do so, the master transmits data bits to the SDA input of the A8522, synchronized with the clocking signal the master transmits simultaneously on the SCL input. The pulse train is shown in figure A-6. A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA pin (Stop bit). Between these points, the Master transmits a pattern of chip address with the Read command (R/$\overline{W}$ = 1) and then the address of the register to be read. Again, the address consists of two bytes, comprising the address of the A8522 (chip address) with the read enable bit, followed by the address of the individual register. The bus master then executes a Master Restart, reissues the slave address, then the A8522 exports the data byte for that register, synchronized with the clock pulse supplied by the master. The master must provide the clock pulses, as the A8522 slave does not have the capability to generate them.

If the master does not send an non-acknowledge bit (AK = 1) after receiving the data, the A8522 will continue sending data from the sequential registers after the addressed one, as shown in figure A-5. After the master provides an non-acknowledge bit, the A8522 will stop sending the data. After that, if additional register reads are required, the process must start over again.

Order of Reading and Writing Registers

All I²C registers can be read back in any order, either one byte at a time or multiple bytes sequentially.

As for writing, however, the following register pairs must be written sequentially as a 16-bit word (MSB/LSB):

- Reg0x00-01 = LED channel enable
- Reg0x02-03 = LED PWM period
- Reg0x10-11 = LED1 PWM on-time
- Reg0x12-13 = LED2 PWM on-time
  ...
- Reg0x1E-1F = LED8 PWM on-time

Dealing with Incomplete Transmission

There is no restriction on how slow the I²C clock can be. Suppose the Master sent out part of a data byte and then paused, the Slave will wait for the rest of the byte indefinitely. The proper way for the Master to terminate an incomplete transmission is to send out either a STOP command or a new START command. The Slave will then discard the previously received incomplete data.

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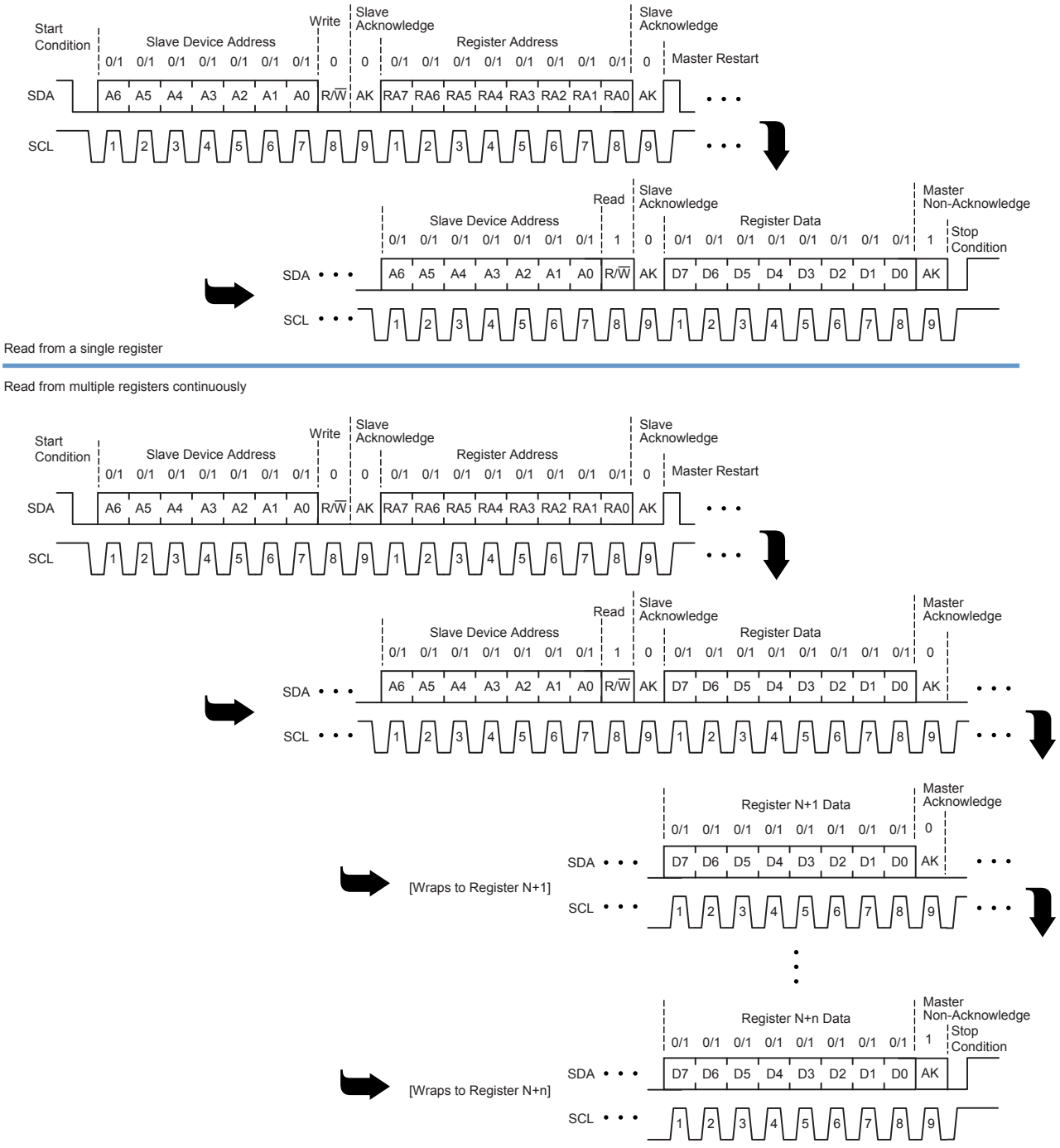

Figure A-6: Reading from Single and to Multiple Registers

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Register Map

Table A-1: Register Banks and Bit Names

RB#	Address	Register Name	Definition	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Default Value	Type*
				Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
0	0x00	LED Enable	Enable / disable each populated LED string	–	–	–	–	–	–	Not Available	Not Available	0000 0011	R/W
1	0x01			LED8EN	LED7EN	LED6EN	LED5EN	LED4EN	LED3EN	LED2EN	LED1EN	1111 1111	R/W
2	0x02	LED PWM Period	Program the PWM period for all LED strings	–	–	–	PWM12	PWM11	PWM10	PWM9	PWM8	0000 1111	R/W
3	0x03			PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	1111 1111	R/W
4	0x04	OVP Threshold	Program the OVP threshold	–	–	–	OVP4	OVP3	OVP2	OVP1	OVP0	0001 1100	R/W
5	0x05	Boost Dithering and Thermal Derating	Program the boost dither and LED derating	–	–	–	–	–	TD	BD1	BD2	0000 0000	R/W
6	0x06	Fault Mode	Program the fault action type for general 12 faults	–	–	–	–	FAULT12	FAULT11	FAULT10	FAULT9	0000 1010	R/W
7	0x07			FAULT8	FAULT7	FAULT6	FAULT5	FAULT4	FAULT3	FAULT2	FAULT1	1011 1110	R/W
8	0x08	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
9	0x09	Polyphase Grouping	Program the polyphase for LEDs 2 through 10	–	LED8PPH	LED7PPH	LED6PPH	LED5PPH	LED4PPH	LED3PPH	LED2PPH	0000 0000	R/W
10	0x0A	LED Short-Detect Threshold	Program LED short detect threshold for LEDs 1-2	–	SDT2_2	SDT2_1	SDT2_0	–	SDT1_2	SDT1_1	SDT1_0	0000 0000	R/W
11	0x0B		Program LED short detect threshold for LEDs 3-4	–	SDT4_2	SDT4_1	SDT4_0	–	SDT3_2	SDT3_1	SDT3_0	0000 0000	R/W
12	0x0C		Program LED short detect threshold for LEDs 5-6	–	SDT6_2	SDT6_1	SDT6_0	–	SDT5_2	SDT5_1	SDT5_0	0000 0000	R/W
13	0x0D		Program LED short detect threshold for LEDs 7-8	–	SDT8_2	SDT8_1	SDT8_0	–	SDT7_2	SDT7_1	SDT7_0	0000 0000	R/W
14	0x0E	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
15	0x0F	GPO Control	General-purpose output selection	–	–	–	GPO1S1	GPO1S0	–	GPO2S1	GPO2S0	0000 0000	R/W
16	0x10	PWM Dimming On-Time	Program PWM on-time for LED1	T1_15	T1_14	T1_13	T1_13	T1_12	T1_11	T1_10	T1_9	0000 0000	R/W
17	0x11			T1_8	T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	0000 0000	R/W
18	0x12		Program PWM on-time for LED2	T2_15	T2_14	T2_13	T2_13	T2_12	T2_11	T2_10	T2_9	0000 0000	R/W
19	0x13			T2_8	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	0000 0000	R/W
20	0x14		Program PWM on-time for LED3	T3_15	T3_14	T3_13	T3_13	T3_12	T3_11	T3_10	T3_9	0000 0000	R/W
21	0x15			T3_8	T3_7	T3_6	T3_5	T3_4	T3_3	T3_2	T3_1	0000 0000	R/W
22	0x16		Program PWM on-time for LED4	T4_15	T4_14	T4_13	T4_13	T4_12	T4_11	T4_10	T4_9	0000 0000	R/W
23	0x17			T4_8	T4_7	T4_6	T4_5	T4_4	T4_3	T4_2	T4_1	0000 0000	R/W
24	0x18		Program PWM on-time for LED5	T5_15	T5_14	T5_13	T5_13	T5_12	T5_11	T5_10	T5_9	0000 0000	R/W
25	0x19			T5_8	T5_7	T5_6	T5_5	T5_4	T5_3	T5_2	T5_1	0000 0000	R/W
26	0x1A		Program PWM on-time for LED6	T6_15	T6_14	T6_13	T6_13	T6_12	T6_11	T6_10	T6_9	0000 0000	R/W
27	0x1B			T6_8	T6_7	T6_6	T6_5	T6_4	T6_3	T6_2	T6_1	0000 0000	R/W
28	0x1C		Program PWM on-time for LED7	T7_15	T7_14	T7_13	T7_13	T7_12	T7_11	T7_10	T7_9	0000 0000	R/W
29	0x1D			T7_8	T7_7	T7_6	T7_5	T7_4	T7_3	T7_2	T7_1	0000 0000	R/W
30	0x1E		Program PWM on-time for LED8	T8_15	T8_14	T8_13	T8_13	T8_12	T8_11	T8_10	T8_9	0000 0000	R/W
31	0x1F			T8_8	T8_7	T8_6	T8_5	T8_4	T8_3	T8_2	T8_1	0000 0000	R/W
32	0x20	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
33	0x21	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
34	0x22	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
35	0x23	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
36	0x24	PWM On-Time Update	Command loading all LED on-times	–	–	–	–	–	–	–	LOAD	0000 0000	W

Continued on the next page…

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Table A-1: Register Banks and Bit Names (continued)

RB#	Address	Register Name	Definition	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Default Value	Type*
				Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
37	0x25	LED Regulation Voltage and Output Hysteresis	Program boost slope compensation, hysteresis, LED regulation voltage and Dummy Load	DUMMYLOAD	–	–	–	LEDREG	–	OUTHYS	SLOPE	0000 0000	R/W
38	0x26	LEDx DC current	Program the DC current of LED1	–	–	DC1_5	DC1_4	DC1_3	DC1_2	DC1_1	DC1_0	0001 1111	R/W
39	0x27		Program the DC current of LED2	–	–	DC2_5	DC2_4	DC2_3	DC2_2	DC2_1	DC2_0	0001 1111	R/W
40	0x28		Program the DC current of LED3	–	–	DC3_5	DC3_4	DC3_3	DC3_2	DC3_1	DC3_0	0001 1111	R/W
41	0x29		Program the DC current of LED4	–	–	DC4_5	DC4_4	DC4_3	DC4_2	DC4_1	DC4_0	0001 1111	R/W
42	0x2A		Program the DC current of LED5	–	–	DC5_5	DC5_4	DC5_3	DC5_2	DC5_1	DC5_0	0001 1111	R/W
43	0x2B		Program the DC current of LED6	–	–	DC6_5	DC6_4	DC6_3	DC6_2	DC6_1	DC6_0	0001 1111	R/W
44	0x2C		Program the DC current of LED7	–	–	DC7_5	DC7_4	DC7_3	DC7_2	DC7_1	DC7_0	0001 1111	R/W
45	0x2D		Program the DC current of LED8	–	–	DC8_5	DC8_4	DC8_3	DC8_2	DC8_1	DC8_0	0001 1111	R/W
46	0x2E	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
47	0x2F	Reserved	–	–	–	–	–	–	–	–	–	0000 0000	R/W
48	0x30	Fault Status	Check the general 12 faults active fault status	–	–	–	–	FS12	FS11	FS10	FS9	XXXX XXXX	R
49	0x31			FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	XXXX XXXX	R
50	0x32	Reserved	–	–	–	–	–	–	–	–	–	XXXX XXXX	R
51	0x33	Active LED In-regulation Status	Read the status of LEDs in regulation	REG8	REG7	REG6	REG5	REG4	REG3	REG2	REG1	XXXX XXXX	R
52	0x34	Reserved	–	–	–	–	–	–	–	–	–	XXXX XXXX	R
53	0x35	LED Pin Shorted to GND Status	Read the status of LED pin-to-GND shorts	LGS8	LGS7	LGS6	LGS5	LGS4	LGS3	LGS2	LGS1	XXXX XXXX	R
54	0x36	Reserved	–	–	–	–	–	–	–	–	–	XXXX XXXX	R
55	0x37	LED String Short-Detect Status	Read the status of LED string short detect	LSD8	LSD7	LSD6	LSD5	LSD4	LSD3	LSD2	LSD1	XXXX XXXX	R
56	0x38	Latched Fault Status	Check the general 12 faults hold fault status	–	–	–	–	FAULTHST12	FAULTHST11	FAULTHST10	FAULTHST9	XXXX XXXX	R/COW
57	0x39			FAULTHST8	FAULTHST7	FAULTHST6	FAULTHST5	FAULTHST4	FAULTHST3	FAULTHST2	FAULTHST1	XXXX XXXX	R/COW
58	0x3A		Reserved	–	–	–	–	–	–	–	–	XXXX XXXX	R/COW
59	0x3B		Check the hold fault status of LEDs in regulation	LED8HREG	LED7HREG	LED6HREG	LED5HREG	LED4HREG	LED3HREG	LED2HREG	LED1HREG	XXXX XXXX	R/COW
60	0x3C		Reserved	–	–	–	–	–	–	–	–	XXXX XXXX	R/COW
61	0x3D		Read the hold fault status of LED GND shorts	LED8HGND	LED7HGND	LED6HGND	LED5HGND	LED4HGND	LED3HGND	LED2HGND	LED1HGND	XXXX XXXX	R/COW
62	0x3E		Reserved	–	–	–	–	–	–	–	–	XXXX XXXX	R/COW
63	0x3F		Read the hold fault status of LED string short detect	LED8HOVP	LED7HOVP	LED6HOVP	LED5HOVP	LED4HOVP	LED3HOVP	LED2HOVP	LED1HOVP	XXXX XXXX	R/COW
64	0x40		Reserved	–	–	–	–	–	–	–	–	XXXX XXXX	R
65	0x41		Read the status of LED Drive OK	LED8VCC	LED7VCC	LED6VCC	LED5VCC	LED4VCC	LED3VCC	LED2VCC	LED1VCC	XXXX XXXX	R
66	0x42		Reserved	–	–	–	–	–	–	–	–	XXXX XXXX	R/COW
67	0x43		Read the fault hold status of LED Drive OK	LED8HVCC	LED7HVCC	LED6HVCC	LED5HVCC	LED4HVCC	LED3HVCC	LED2HVCC	LED1HVCC	XXXX XXXX	R/COW

* R/W = Read and Write, W = Write only, R = Read only, R/COW = Read and Clear-On-Write (by writing a '1' to the bit field).

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Register Field Reference

LED Enable

Address: 0x00:0x01

RB	RB0 (0x00)								RB1 (0x01)							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–	LED Enable_L							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
MSB = Bit 9																

LED Enable_L [7:0]

LED Enable Settings (LSB Byte)

Enables or disables LED strings 1 to 8.

Bit	Value	Description
7	0	Disable LED8
	1	Enable LED8 (default)
6	0	Disable LED7
	1	Enable LED7 (default)
5	0	Disable LED6
	1	Enable LED6 (default)
4	0	Disable LED5
	1	Enable LED5 (default)
3	0	Disable LED4
	1	Enable LED4 (default)
2	0	Disable LED3
	1	Enable LED3 (default)
1	0	Disable LED2
	1	Enable LED2 (default)
0	0	Disable LED1
	1	Enable LED1 (default)

Note 1: It is important that the user clear register 0x00, by writing 0s to every bit in that register, in order for strings LED1 through LED8 to operate correctly.

Note 2: If any LED is unpopulated (signalled by having a 4.7 kΩ resistor from the LEDx pin to GND) , but during startup it is incorrectly set to Enable in this register, the IC considers this an error and will not proceed with startup. This is summarized in the following table:

LED String Hardware Status	Register (RB0+1 Enable Status	LED LIght	Fault Flag
Populated	Disabled	Off	High (no fault)
	Enabled	On	High (no fault)
Unpopulated (4.7 kΩ resistor to GND)	Disabled	Off	High (no fault)
	Enabled	Off	Low (fault)

Note 3: In case the Fault 11 flag is erroneously set in the Fault Status Hold register, clear it by writing 0x0400 to register bank 0x38-0x39. Do this only after the enable registers 0x00-0x01 have been correctly set.

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LED PWM Period

Address: 0x02:0x03

RB	RB2 (0x02)								RB3 (0x03)							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	PWM_Period_H					PWM_Period_L							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	X	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
MSB = Bit 12																

PWM_Period_H [12:8]

PWM Dimming Period (MSB Byte)

PWM_Period_L [7:0]

PWM Dimming Period (LSB Byte)

Bit	Value	Description
12:0	0/1	Absolute PWM period multiplier

This register allows the user to set a wide variety of PWM dimming periods. Bit resolution is 1.5 µs. The actual PWM period is defined as (N+1) × 1.5 µs, where N is the combined value stored in these two register banks. A 13-bit total programming capability allows the user program up to approximately a 10 ms PWM period (a 100 Hz PWM frequency).

The smallest recommended PWM period is 45 µs (22 kHz PWM frequency). The maximum recommended PWM period is 9.830 ms, which corresponds to a setting of XXX1 1001 1001 1000 (calculated as: (6552+1) × 1.5 µs = 9.8295 ms).

It is possible for the user to program a longer PWM period, but doing so will not allow 100% PWM dimming because the LED on-time counter can be programmed only up to a maximum of 9.830 ms. So for example, if the user programs the maximum period (XXX1 1111 1111 1111), this gives a PWM period of (8191+1) × 1.5 µs = 12.288 ms, so all LEDs would be limited to an 80% PWM duty cycle.

The reset setting is 0x0fff = 4095. This corresponds to a PWM period of (4095+1) × 1.5 µs = 6.144 ms (162.8 Hz PWM frequency).

Example: To set the PWM frequency to 400 Hz:

1. PWM period = 1/400 = 2.5 ms
2. Number of steps = 2.5 ms / 1.5 µs = 1667
3. The required LED PWM_Period register value is then 1666 (XXX0 0110 1000 0010):

   RB2 = 0000 0110 (MSB)

   RB3 = 1000 0010 (LSB)

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OVP Threshold

Address: 0x04

RB	RB4 (0x04)							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	OVP				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	X	X	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	1	1	1	0	0
MSB = Bit 4								

OVP [4:0]

OVP Trip Point

Sets the OVP trip point multiplier. Bit resolution is 1.0 V. The OVP trip point can be set anywhere from 8 V (00000) to 39 V (11111). Example: The reset value of 0x1C, 28 decimal, gives an OVP trip point of: 8 V + (1.0 V × 28) = 36 V.

Bit	Value	Description
4:0	0/1	Sets the OVP threshold multiplier

Boost Dithering and Thermal Derating

Address: 0x05

RB	RB5 (0x05)							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	TD	BD1	BD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	X	X	X	X	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 2								

TD [2]

LED Derating Enable

Enables the Thermal Derating function.

Bit	Value	Description
2	0	Disable Thermal Derating feature (default)
	1	Enable Thermal Derating

BDx [1:0]

Boost Dither Enable and Magnitude

Enable and set the multiplier for the main switching frequency dithering feature. Not available when external synchronization signal is used (through FSET/SYNC pin). Example: Value of 11 sets ±15% (step size x number of steps = 5% × 3). If f_{SW} = 600 kHz, ±90 kHz: lower frequency = 510 kHz, upper frequency = 690 kHz.

Bit		Description
BD1	BD0	
0	0	Disable dithering (default)
0	1	Frequency variation ±5% of nominal f_{SW}
1	0	Frequency variation ±10% of nominal f_{SW}
1	1	Frequency variation ±15% of nominal f_{SW}

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Fault Mode

Address: 0x06:0x07

RB	RB6 (0x06)								RB7 (0x07)							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	FAULT CNTRL_M				FAULT CNTRL_L							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R/W	R	R/W	R/W	R
Value	X	X	X	X	0/1	0/1	0/1	0	0/1	0	1	0/1	1	0/1	0/1	0
Reset	0	0	0	0	1	0	1	0	1	0	1	1	1	1	1	0
MSB = Bit 11																

FAULT CNTRL_M [11:8]

Fault Control Mode Settings (MSB Byte)

Sets the fault handling behavior for faults 9 through 12. Certain bits are non-programmable (default value only) for safety reasons.

Bit	Value	Description
11	0	Fault 12 Latched (no auto restart)
	1	Fault 12 Auto restart (default)
10	0	Fault 11 Latched (no auto restart) (default)
	1	Fault 11 Auto restart
9	0	Fault 10 Latched (no auto restart)
	1	Fault 10 Auto restart (default)
8	0	Fault 9 Latched (no auto restart) (default)

FAULT CNTRL_L [7:0]

Fault Control Mode Settings (LSB Byte)

Sets the fault handling behavior for faults 8 through 1. Certain bits are non-programmable (default value only) for safety reasons.

Bit	Value	Description
7	0	Fault 8 Latched (no auto restart)
	1	Fault 8 Auto restart (default)
6	0	Fault 7 Latched (no auto restart) (default)
5	1	Fault 6 Auto restart (default)
4	0	Fault 5 Latched (no auto restart)
	1	Fault 5 Auto restart (default)
3	1	Fault 4 Auto restart (default)
2	0	Fault 3 Latched (no auto restart)
	1	Fault 3 Auto restart (default)
1	0	Fault 2 Latched (no auto restart)
	1	Fault 2 Auto restart (default)
0	0	Fault 1 Latched (no auto restart) (default)

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Polyphase Grouping

Address: 0x08:0x09

RB	RB9 (0x09)							
Bit	7	6	5	4	3	2	1	0
Name	–	POLYPHASE_L						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 6								

POLYPHASE_L [6:0]

LED String Grouping (LSB Byte)

Enables grouping with LED8 through LED2. Note: LED1 is not included, because there is no lower-number LED channel, but it can be grouped by setting LED2.

Bit	Value	Description
6	0	LED8 not grouped (default)
	1	LED8 grouped
5	0	LED7 not grouped (default)
	1	LED7 grouped
4	0	LED6 not grouped (default)
	1	LED6 grouped
3	0	LED5 not grouped (default)
	1	LED5 grouped
2	0	LED4 not grouped (default)
	1	LED4 grouped
1	0	LED3 not grouped (default)
	1	LED3 grouped
0	0	LED2 not grouped (default)
	1	LED2 grouped

An ungrouped LED channel starts PWM operation in a separate time slot, with duty cycle specified by the corresponding PWM Dimming On-Time register.

A grouped LED channel starts in the same time slot as the next lower-numbered channel, and inherits the PWM Dimming On-Time of that lower-numbered channel (the original time slot of the grouped channel is not used). If more than one adjacent channels are grouped, the entire group starts at the time slot of the lowest-numbered channel in the group, and inherits that on-time setting. Example: Set bit 6 to group LED8 with LED7 (start and duty cycle according to LED7), also set bit 5 to group LED8 and LED7 with LED6 (start and duty cycle according to LED6).

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LED Short-Detect Threshold

Address: 0x0A: 0x0E

RB	RB10 (0x0A) to RB14 (0x0E)							
Bit	7	6	5	4	3	2	1	0
RB10	–	SDT2_x			–	SDT1_x		
RB11	–	SDT4_x			–	SDT3_x		
RB12	–	SDT6_x			–	SDT5_x		
RB13	–	SDT8_x			–	SDT7_x		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 6 and bit 2								

SDTx_x [6:4], [2:0]

LED String Short Detect Threshold

Allows adjustment of the LED string short-detect threshold for each LED channel to prevent false tripping if the voltage drop across all LED strings varies by more than one LED V_f during normal operation.

Bit			Description
6	**5**	**4**	
2	**1**	**0**	
0	0	0	Threshold = 12 V (default)
0	0	1	Threshold = 11 V
0	1	0	Threshold = 10 V
0	1	1	Threshold = 9 V
1	0	0	Threshold = 8 V
1	0	1	Threshold = 7 V
1	1	0	Threshold = 6 V
1	1	1	Threshold = 5 V

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General Purpose Output Selection

Address: 0x0F

RB	RB15 (0x0F)							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	GPO1		–	GPO2	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	X	X	0/1	0/1	X	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 4, bit 1								

GPO1 [4:3]

General Purpose Output 1 Data

Select data type to be output on the GPO1 pin.

Bit		Description
4	3	
0	0	Data: Boost soft start status (default) High = soft start in progress Low = soft start finished
0	1	Data: Master system clock / 4 Normal operation = approximately 1.65 MHz
1	0	Data: LED PWM frequency Normal operation = low approximately 300 ns each PWM period)
1	1	Data: Thermal Warning High = normal operation Low = Thermal Derating active

GPO2 [1:0]

General Purpose Output 2 Data

Select data type to be output on the GPO2 pin.

Bit		Description
1	0	
0	0	Data: IC and LED status (default) High = startup test not passed Low = LED startup test passed
0	1	Data: SW 1x Current Limit High = normal operation Low = current limit exceeded
1	0	Data: Boost status High = Boost switching Low = No switching
1	1	Reserved

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PWM Dimming On-Time

Address: 0x10:0x1F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RB	RB16 (0x10)								RB17 (0x11)							
Name	LED1_TON_M								LED1_TON_L							
RB	RB18 (0x12)								RB19 (0x13)							
Name	LED2_TON_M								LED2_TON_L							
RB	RB20 (0x14)								RB21 (0x15)							
Name	LED3_TON_M								LED3_TON_L							
RB	RB22 (0x16)								RB23 (0x17)							
Name	LED4_TON_M								LED4_TON_L							
RB	RB24 (0x18)								RB25 (0x19)							
Name	LED5_TON_M								LED5_TON_L							
RB	RB26 (0x1A)								RB27 (0x1B)							
Name	LED6_TON_M								LED6_TON_L							
RB	RB28 (0x1C)								RB29 (0x1D)							
Name	LED7_TON_M								LED7_TON_L							
RB	RB30 (0x1E)								RB31 (0x1F)							
Name	LED8_TON_M								LED8_TON_L							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	X	X	X	X	X	X	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB = Bit 15																

LEDx_TON_M [15:8]
LED PWM On-Time (MSB Byte)

LEDx_TON_L [7:0]
LED PWM On-Time (LSB Byte)

Bit	Value	Description
15:0	0/1	Absolute PWM on-time multiplier

Set PWM dimming on-time multiplier for each LED channel. 16 bits are required for each channel. Bit resolution is 150 ns.

Let T = LED PWM Period, and t_{ON} = PWM Dimming On-Time, then the PWM dimming percentage = t_{ON} / T.

Although the minimum on-time that can be set by the register is 150 ns, in practice it is strongly advised to keep the on-time at 1 µs or above. This implies a maximum dimming ratio of 5000:1 at 200 Hz PWM frequency. Therefore, the minimum t_{ON} multiplier is 7 (0000 0000 0000 0111 in binary), which gives 150 ns × 7 = 1.05 µs.

The maximum t_{ON} multiplier is 65,535 (1111 1111 1111 1111 in binary), which gives 150 ns × 65,535 = 9.83 ms. When all 16 bits are 1, or when t_{ON} > T , the LEDs are on all the time.

The default register value = 0x0000, which means all LED channels are off, even if they are enabled by RB0 and RB1. Therefore it is necessary to update the LED on-time registers first, in order to turn on LED strings.

The registers must be written as MSB followed by LSB. Update is allowed only after LSB write is complete. All eight registers are buffered initially, until a Write operation is performed on register 0x24, at which time all 8 channels are updated together.

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PWM On-Time Update

Address: 0x24

RB	RB36 (0x24)							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	LOAD
R/W	W	W	W	W	W	W	W	R/W
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 0								

LOAD [0]

Enable Load PWM On-Time Update

All PWM on-time registers are buffered and do not take effect until a Write operation is performed on register 0x24 (the actual data written does not matter). When the write operation is complete, all eight channel data are updated together. This feature is vital for applications that require synchronized update for all LED brightness, such as for localized dimming.

Bit	Value	Description
0	0	(default)
	1	Upload current contents of PWM dimming on-time registers

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LED Regulation Voltage and Output Hysteresis

Address: 0x25

RB	RB37 (0x25)							
Bit	7	6	5	4	3	2	1	0
Name	DUMMYLOAD	–	–	–	LEDREG	–	OUTHYS	SLOPE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0
MSB = Bit 7								

DUMMYLOAD [7]

Enable Startup Output Load Resistance

Enables a resistive load of approximately 4.3 kΩ connected to VOUT during startup process. The load is removed after startup is completed.

Bit	Value	Description
7	0	(default)
	1	Enable connection of resistive load

LEDREG [3]

Enable Augmented LED Regulation Voltage

The A8522 has a minimum LED Regulation voltage of 0.85 V (typ). Lower regulation voltage is generally preferred, because it means less power loss across the LEDx current sinks. In certain situations (such as during input voltage transients at extremely low PWM duty cycles) it may be advantageous to set the regulation voltage higher in order to maintain current regulation.

Bit	Value	Description
3	0	Normal V_{REG}, 0.85 V (typ) (default)
	1	Augmented V_{REG}, 1.05 V

OUTHYS [1]

Enable Augmented Output Hysteresis

The A8522 has a minimum output voltage hysteresis of 0.25 V. Lower hysteresis is generally preferred, because excessive ripple voltage may lead to audible noises from output ceramic capacitors. But larger ripple may be required to reduce the frequency of the hysteresis control loop. The correct value should be determined through experimentation.

Bit	Value	Description
1	0	Normal V_{OUThys}, 0.25 V (typ) recommended (default)
	1	Augmented V_{OUThys}, 0.45 V

SLOPE [0]

Enable Reduced Slope Compensation

Slope compensation is necessary in current-mode control circuits in order to avoid instability at > 50% SW duty cycle. The A8522 allows selection between two slope compensation values for best results.

Bit	Value	Description
0	0	10.8 A/µs at 2 MHz
	1	2.3 A/µs at 2 Mz

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LEDx DC Current

Address: 0x26: 0x2D

Bit	7	6	5	4	3	2	1	0
RB	RB38 (0x26)							
Name	–	–	LED1_CURRENT					
RB	RB39 (0x27)							
Name	–	–	LED2_CURRENT					
RB	RB40 (0x28)							
Name	–	–	LED3_CURRENT					
RB	RB41 (0x29)							
Name	–	–	LED4_CURRENT					
RB	RB42 (0x2A)							
Name	–	–	LED5_CURRENT					
RB	RB43 (0x2B)							
Name	–	–	LED6_CURRENT					
RB	RB44 (0x2C)							
Name	–	–	LED7_CURRENT					
RB	RB45 (0x2D)							
Name	–	–	LED8_CURRENT					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	1	1	1	1	1
MSB = Bit 5								

LEDx_CURRENT [5:0]

LED Current Sink Capacity

Sets DC sink current capability multiplier for each LED channel. Bit resolution is 1 mA. Each LED channel has a base current of 1 mA. Default is 0x1F = 32 mA.

Bit	Value	Description
5:0	0/1	Absolute LED current multiplier

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Fault Status

Address: 0x30:0x31

RB	RB48 (0x30)								RB49 (0x31)							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Value	X	X	X	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FSx [11:0]

General Fault Status

Reports status of the 12 general faults. In the event of a fault condition ($\overline{\text{FLAG}}$ pin is pulled low), the system controller can read these registers to determine which fault condition has occurred. For certain faults, such as LED pin open/short, other status registers are available to be read to determine which LED circuit caused the fault.
Note: Some fault types are followed by auto-restart. For such faults, if the fault is subsequently resolved, the corresponding bit is cleared in the General Fault Status register. Despite that, to allow the system controller the option of diagnosing the problem, the incident remains recorded in the Latched Status registers (0x38 through 0x43) until a reset occurs.

Bit	Value	Description
11:0	0	No fault present (default)
	1	Specific fault detected

Active LED In-Regulation Status

Address: 0x33

RB	RB51 (0x33)							
Bit	7	6	5	4	3	2	1	0
Name	REG8	REG7	REG6	REG5	REG4	REG3	REG2	REG1
R/W	R	R	R	R	R	R	R	R
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0

REGx [7:0]

LED Voltage Fault Status

Sets a bit for each LED channel, when an LED driver is not in regulation and the output exceeds the OVP threshold. Used with FAULT 8.

Bit	Value	Description
7:0	0	LED in regulation or not enabled (default)
	1	LED out of regulation and V_{OUT} exceeds OVP

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LED Pin Shorted to GND Status

Address: 0x35

RB	RB53 (0x35)							
Bit	7	6	5	4	3	2	1	0
Name	LGS8	LGS7	LGS6	LGS5	LGS4	LGS3	LGS2	LGS1
R/W	R	R	R	R	R	R	R	R
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0

LGSx [7:0]

LED Short to GND Fault Status

This bit is set if an LED pin voltage is found to remain at GND level during startup (prevents further initialization). Used with FAULT 10.

Bit	Value	Description
7:0	0	LED voltage normal (default)
	1	LED remaining at GND during startup

LED String Short-Detect Status

Address: 0x37

RB	RB54 (0x37)							
Bit	7	6	5	4	3	2	1	0
Name	LSD8	LSD7	LSD6	LSD5	LSD4	LSD3	LSD2	LSD1
R/W	R	R	R	R	R	R	R	R
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0

LSDx [7:0]

LED String Short Detect Status

This bit is set if an LED pin voltage goes above its preset voltage limit, as set by its corresponding LED pin Short-Detect Threshold register. Used with FAULT 12.

Bit	Value	Description
7:0	0	LED voltage normal (default)
	1	LED exceeds short-detect threshold

Latched Status Registers

Address: 0x38:0x43

(RB56 to RB67)

Retain the status of faults that have been detected, allowing the system controller to poll them by an I²C Read to diagnose problems. All bits are cleared after a Read for the register.

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Appendix B. Feedback Loop Components Calculation for Peak Current Control Boost Converter Used in LED Drivers Applications

This appendix provides an examination of the factors involved in calculating the transfer function of a peak current controlled boost converter, an output to control transfer function, and recommendations for stabilizing the feedback loop closed system. An example of a complete small signal model of a peak-current-mode boost converter is shown in figure B-2. The A8522 is an example of a boost converter that drives 8 LED strings with 10 LEDs in each string.

Power Stage Transfer Function

Using a frequency-based model, the transfer function (control to output) of boost power stage peak-current control is given by the following equation:

$$T_P(f) = A_P \times \frac{\left(1+\frac{2\times\pi\times f\times j}{\omega_Z}\right)\times\left(1-\frac{2\times\pi\times f\times j}{\omega_{RHP}}\right)}{\left(1+\frac{2\times\pi\times f\times j}{\omega_P}\right)\times\left(1+\frac{2\times\pi\times f\times j}{Q_D\times\omega_S}-\frac{(2\times\pi\times f\times j)^2}{\omega_S^2}\right)} \quad \text{(B-1)}$$

A_P is the DC gain,
ω_Z is the angular frequency of the output capacitor ESR zero, f_Z,
ω_{RHP} is the angular frequency of the right-half plane zero, f_{RHP},
ω_P is the angular frequency of the output load pole, f_P,
Q_D is the inductor peak current sampling double pole quality or damping factor, and
ω_S is the double-pole angular frequency oscillation.

Figure B-1 shows the plot of the power stage logarithmic transfer function as gain, $G_{P(f)}$, versus frequency. with $G_{P(f)}$ given by:

$$G_P(f) = 20 \times \log(|T_P(f)|) \quad \text{(B-2)}$$

The next sections define the components of $T_P(f)$.

A_P, DC gain

The DC gain is defined as follows:

$$A_P = \frac{1-D(\text{nom})}{R_I} \times \frac{R_S \times R_{EQ}}{R_S + R_D + R_{EQ}} \quad \text{(B-3)}$$

where

- D is the PWM duty cycle, calculated as:

$$D(\text{nom}) = (V_{OUT} - V_{IN}(\text{nom})) / V_{OUT} \quad \text{(B-4)}$$

where

$$V_{OUT} = N_L \times V_f + V_{REG} + V_D + V_H \quad \text{(B-5)}$$

and
N_L is the quantity of LEDs per string,
V_f is the nominal forward voltage drop for each LED diode,
V_{REG} is the current sink regulated voltage for each LED string,
V_D is the Schottky diode forward voltage drop and
V_H is the output hysteresis-control voltage.
- R_I is the current sense resistor, which is connected in series with the boost power switch,
- R_S is the LED sink pin sense resistor, which is usually located inside the IC and can be calculated from the following equation:

$$R_S = V_{REG} / I_{LED} \quad \text{(B-6)}$$

where I_{LED} is the current through one LED string,

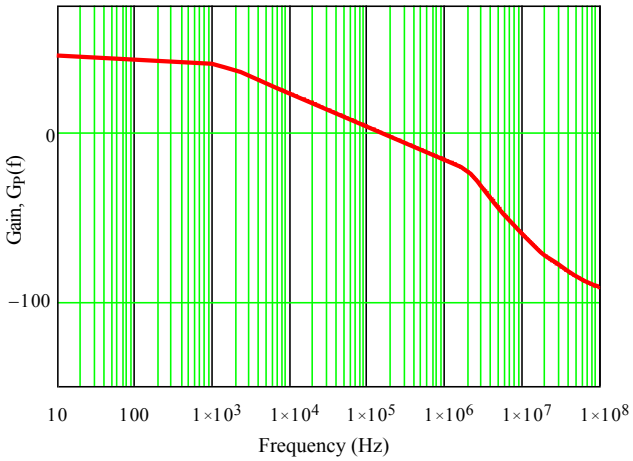

Figure B-1. Plot of power stage transfer function versus frequency

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- R_{EQ} is the output nominal operating resistance, which is given by the following equation:

$$R_{EQ} = V_{OUT} / I_{LEDT} \quad \text{(B-7)}$$

where I_{LEDT} is the total output current through all LED strings:

$$I_{LEDT} = N_S \times I_{LED} \quad \text{(B-8)}$$

and N_S is the total quantity of LED strings, and

- R_D is the total dynamic resistance of one LED string, which can be measured in the lab, as follows:

1. Get a load board with one string of LEDs.
2. Apply an external DC voltage across all LEDs in one string through a current limit resistor, R = 10 Ω.
3. Change the DC voltage to get 90% of one string current. Then measure the voltage across all LEDs in one string.
4. Repeat step 3 until reaching 100% of one string current.
5. Calculate $R_D = (V_2 - V_1) / (I_2 - I_2)$. V_2 is the voltage across all LEDs in one string at I_2 = 100% of one string LED current. V_1 is the voltage across all LEDs in one string at I_1 = 90% of one string LED current.

Q_D, inductor peak current sampling double pole quality

$$Q_D = \frac{1}{\pi \times [0.5 - D(\text{nom}) + (1 - D(\text{nom})) \times \text{IFSC}]} \quad \text{(B-9)}$$

where

IFSC is the implemented factor of inductor slope compensation, and is given by:

$$\text{IFSC} = (\text{ISC} / \text{CSC}) \times \text{FSC} \quad \text{(B-10)}$$

and

ISC is the IC implemented slope compensation in A/µs. At 2 MHz switching frequency, ISC = 2.3 A/µs. However, it changes as the switching frequency changes. It is normalized to a 2 MHz swtiching frequency. At a switching frequency different from 2 MHz the implemented slope compensation can be calculated from:

$$\text{ISC} = 2.3\ (\text{A}/\mu\text{s}) \times (f_{SW} / 2\ (\text{MHz})) \quad \text{(B-11)}$$

CSC is the calculated slope compensation also in A/µs, given by:

$$CSC = \frac{\Delta I \times \text{FSC} \times 10^{-6}}{(1/f_{SW}) \times (1 - D(\text{max}))} \quad \text{(B-12)}$$

and

$$\Delta I = (V_{IN}(\text{min}) \times D(\text{max})) / L_1 \times f_{SW}, \text{ and} \quad \text{(B-13)}$$

FSC is the Ridley's factor slope compensation, given by:

$$\text{FSC} = 1 - 0.18 / D(\text{max}) \quad \text{(B-14)}$$

ω_Z, angular frequency of the output capacitor ESR zero, f_Z

$$\omega_Z = 1 / (\text{ESR} \times C_{OUT}) \quad \text{(B-15)}$$

ω_{RHP}, angular frequency of the right-half plane zero, f_{RHP}

$$\omega_{RHP} = R_{EQ} / (1 - \text{D(max)})^2 \times L_1) \quad \text{(B-16)}$$

where

$$D(\text{max}) = (V_{OUT} - V_{IN}(\text{min})) / V_{OUT} \quad \text{(B-17)}$$

ω_P, angular frequency of the output load pole, f_P

$$\omega_P = \frac{R_S + R_D + R_{EQ}}{(R_S + R_D + \text{ESR}) \times R_{EQ} \times C_{OUT}} \quad \text{(B-18)}$$

ω_S, angular frequency oscillation of the double pole that occurs at half of the switching frequency, f_{SW}

$$\omega_S = \pi \times f_{SW} \quad \text{(B-19)}$$

Output to Control Transfer Function

When using peak current mode control for a DC-to-DC converter, a type II PI error amplifier compensation circuit is sufficient to stabilize the converter. For controlling the current sink voltage and as a result controlling the output, the A8522 IC uses a high bandwidth transconductance amplifier, shown as A1 in figure B-2.

A transconductance amplifier is actually a voltage-controlled current source. It converts any error voltage at its input pins to a current flowing out of its output pin at V_C. The transconductance gain of the error amplifier, g, is defined as:

$$g = I_{AMP} / V_{error} \quad \text{(B-20)}$$

In figure B-2, R_{AMP} represents the output impedance of the transconductance amplifier (A1). R_{AMP} usually has a high value and it is neglected in the calculation of the error amplifier transfer function.

R_Z, C_Z, and C_P represent the external Type II compensation network. From an AC point of view, the non-inverting pin of A1 is connected to a DC reference voltage, V_{REG}, which is a virtual

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AC ground. Therefore, the transfer function of the compensation circuit is derived as follows:

$$T_{EA}(f) = \frac{V_C(f)}{V_{OUT}(f)} \quad \text{(B-21)}$$

$$= \frac{-1 \times I_{AMP} \times Z_C(f)}{V_{ERROR} \times \left(\frac{R_S + R_D}{R_S}\right)} \quad \text{(B-22)}$$

applying equation B-20:

$$T_{EA}(f) = -1 \times \left(\frac{R_S \times g}{R_S + R_D}\right) \times Z_C(f) \quad \text{(B-23)}$$

where

$$Z_C(f) = \frac{\left(R_Z + \frac{1}{2 \times \pi \times f \times j \times C_Z}\right) \times \left(\frac{1}{2 \times \pi \times f \times j \times C_P}\right)}{\left(R_Z + \frac{1}{2 \times \pi \times f \times j \times C_Z}\right) + \left(\frac{1}{2 \times \pi \times f \times j \times C_P}\right)} \quad \text{(B-24)}$$

Figure B-3 shows the logarithmic transfer function for the output to control compensation circuit, with gain, $G_{EA}(f)$. given by:

$$G_{EA}(f) = 20 \times \log(|T_{EA}(f)|) \quad \text{(B-25)}$$

The transfer function has a single pair of pole and zero in addition to the pole at the origin. The pole at the origin is defined by C_P and R_{AMP}. The zero is defined by R_Z and C_Z. The zero frequency location is selected to compensate or cancel the power train load pole. It is defined by:

$$f_{ZEA} = 1/(2 \times \pi \times R_Z \times C_Z) \quad \text{(B-26)}$$

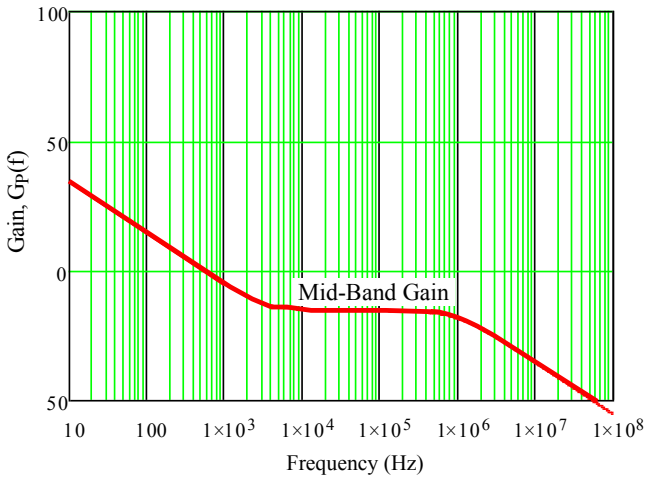

Figure B-3. Plot of error amplifier stage transfer function versus frequency

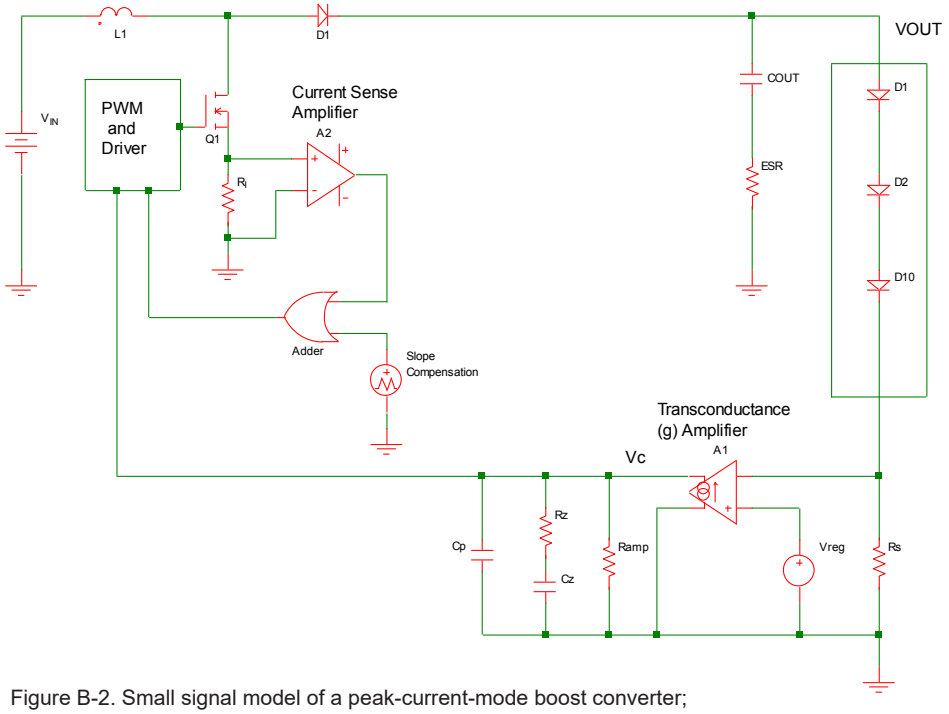

Figure B-2. Small signal model of a peak-current-mode boost converter; the ten strings of the A8522 are represented by one string in this example

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The error amplifier pole frequency is selected to compensate for or cancel the power train ESR zero. This is the case if the frequency of the ESR zero is small or below the switching frequency. Otherwise, it is selected to be at half switching frequency. This pole frequency determines the end of mid-band gain of the error amplifier transfer function, so it ensures that the closed loop system cross-over frequency is below half switching frequency, which is important for stability issues. The pole frequency is defined by:

$$f_{PEA} = \frac{1}{2 \times \pi \times R_Z \times \left(\frac{C_Z \times C_P}{C_Z + C_P} \right)} \quad \text{(B-27)}$$

Stabilizing the Closed Loop System

In this section, calculations are provided for selecting optimal R_Z, C_Z, and C_P. The closed loop system will be stable if the total system transfer function rolls off while crossing over at a phase margin of approximately 90° or –20 dB per decade. It is recommended that the phase margin does not fall below 45°. For higher stability, the cross over frequency should be much less than the right half plane zero and smaller than half of the switching frequency.

To achieve that, first fix the mid-band gain of the error amplifier transfer function. Make it equal in value to the power train gain at the cross over frequency, but negative so the total closed loop gain will be 0 dB. Then position the compensation pole and zero. Here are step-by-step procedures on how to calculate the compensation network components:

1. Calculate R_Z such that the negative mid-band gain of the error amplifier will be equal to the power train gain at the required system bandwidth or cross over frequency.

1a. Calculate the cross over frequency to be much less than the RHP zero and lower than the half-switching frequency. A 20 to 30 kHz cross over frequency is appropriate for LED applications, calculated as follows:

$$f_C = 0.015 \times f_{SW} \quad \text{(B-28)}$$

1b. Calculate, or preferably measure, the power train gain at f_C, which is $G_P(f_C)$, then multiply it by –1.

1c. To compensate for the difference from the error amplifier gain at f_{ZEA} and the actual mid-band gain, subtract an additional 3 dB:

$$-G_P(f_C) - 3 \text{ dB} \quad \text{(B-29)}$$

1d. Convert the calculated gain to a linear gain:

$$10^{\left(\frac{-G_P(f_C)-3}{20}\right)} \quad \text{(B-30)}$$

1e. Calculate R_Z:

$$R_Z = \frac{10^{\left(\frac{-G_P(f_C)-3}{20}\right)}}{g \times \left(\frac{R_S}{R_S + R_D} \right)} \quad \text{(B-31)}$$

2. Select a value for C_Z.

2a. Calculate the frequency for the error-amplifier compensation zero, f_{ZEA}. This zero should cancel the dominant low frequency pole of power train. Therefore, f_{ZEA} should be close to f_P. Usually it is selected to be $^1/_5$ to $^1/_{10}$ of f_C:

$$f_{ZEA} = f_C / 10 \quad \text{(B-32)}$$

2b. Cz can be calculated by applying equation B-26:

$$C_Z = 1 / (2 \times \pi \times R_Z \times f_{ZEA}) \quad \text{(B-33)}$$

3. Select a value for C_P.

3a. Select a frequency for the error-amplifier compensation pole, f_{PEA}. This pole determines the error-amplifier end of the mid-band region. It is selected to cancel the power train ESR zero. However, if ceramic capacitors are used at the output, the ESR zero will be at very high frequency. In this case, the f_{PEA} is selected to be at half of the switching frequency to ensure that f_C is at lower than half the switching frequency and as a result a higher phase margin can be achieved. f_{PEA} is given by:

$$f_{PEA} = 0.5 \times f_{SW} \quad \text{(B-34)}$$

3b. C_P can be calculated by applying equation B-27:

$$C_P = \frac{C_Z}{2 \times \pi \times R_Z \times C_Z \times f_{PEA} - 1} \quad \text{(B-35)}$$

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The closed-loop system transfer function is given by:

$$T_S(f) = T_P(f) \times T_{EA}(f) \quad \text{(B-36)}$$

The closed-loop system logarithmic transfer function gain is given by:

$$G_S(f) = 20 \times \log(|T_S(f)|) \quad \text{(B-37)}$$

Figure B-4 shows the closed loop logarithmic transfer function as gain versus frequency. As shown in figure B-4, if the above methods are implemented the transfer function rolls off while crossing over with around a –20 dB per decade, which results in around a 90° phase margin.

Finally, it is recommended to measure the gain and phase margin of the whole system closed loop. If necessary, the compensation components values could be tweaked to obtain the required cross over frequency and phase margin.

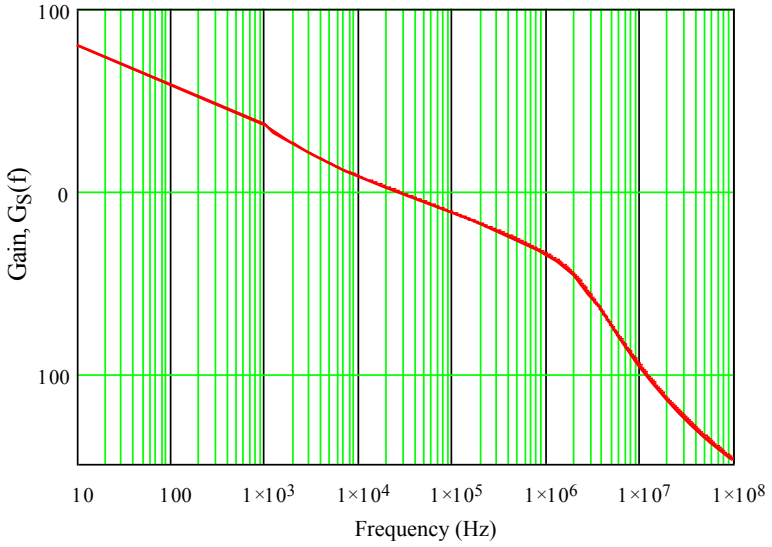

Figure B-4. Plot of the whole system closed loop transfer function gain versus frequency, with a cross over frequency, f_C, of 30 kHz

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Measuring the Feedback Loop Gain and Phase Margin

It is always necessary to measure the feedback loop gain and phase margin of a power converter to make sure the converter runs stably and responds quickly to line or load transients. In addition, to calculate the feedback-loop component values, it is necessary first to calculate or preferably to measure only the power-stage transfer function at the required cross over frequency. Below, one method for measuring the power-stage and the closed-loop whole system transfer functions is presented.

Power Stage Transfer Function Measurement

The power stage or control to output transfer function can be measured using any gain/phase analyzer. Figure B-5 shows a block diagram for the whole closed-loop system. To measure the power-stage transfer function, implement the following steps:

1. First, temporarily, use a large value capacitor for C_Z, say 4.7 µF, and a small value resistor for R_Z, say 100 Ω, to roll-off the control loop at very low frequency.

2. On the PCB cut the trace between VOUT and the LED strings.

3. Connect a 10 Ω resistor from VOUT to the LED strings.

4. Connect the sweeping signal, V_S, leads from the spectrum analyzer line (red) to VOUT and the neutral (black) to the LED string, across the 10 Ω resistor.

5. Hook the voltage probe V2 (red) to VOUT (B1) and the ground lead to PCB GND.

6. Hook the voltage probe V1 (blue) to V_C, so the gain would be $G_P(f) = B1 / A2$.

7. Run the sweep.

8. When the sweep is completed, to read the power stage gain $G_P(f_C)$ at the selected frequency, f_C, place the analyzer screen cursor at that frequency.

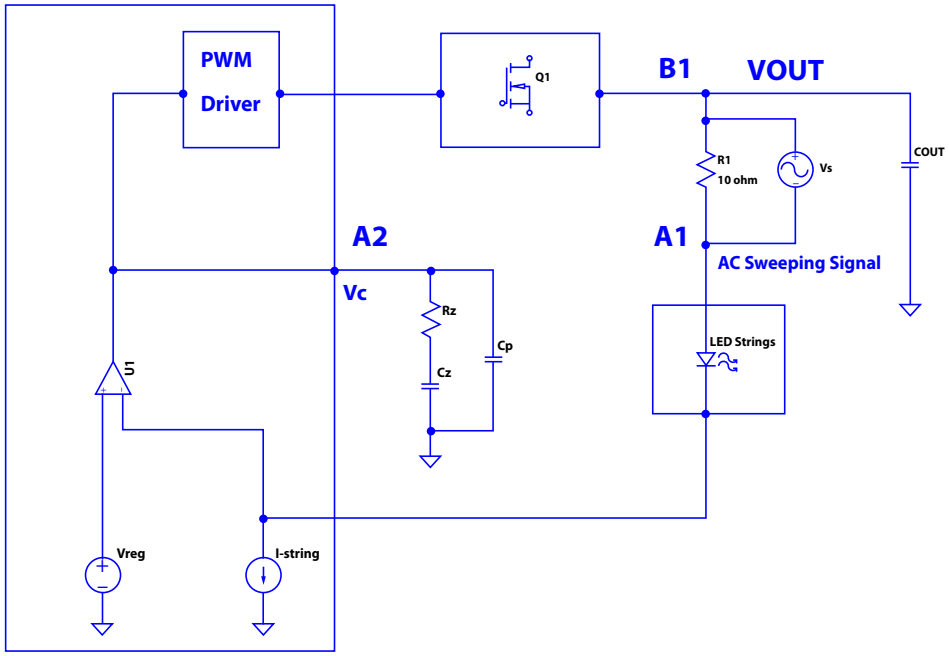

Figure B-5. Simplified block diagram for the closed-loop whole system to show how to measure the gain of the power stage or closed-loop system gain and phase margin

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Whole Closed-Loop System Transfer Function Gain and Phase Margin Measurement

The closed-loop whole system transfer function gain and phase margin can be measured using the following steps:

1. Change R_Z, C_Z, and C_P to be the same as the calculated values.

2. Follow same steps 2 through 5, shown above.

3. Hook the voltage probe V1 (blue) to A1, so the gain would be $G_S(f) = B1/A1$.

4. Run the sweep.

5. When the sweep is completed, to read the phase margin at the cross over frequency, f_C, place the analyzer screen cursor at f_C.

6. To read the gain margin, place the analyzer screen cursor where the phase margin is zero.

The whole system closed loop is considered stable if the phase margin is larger than 45°. It is also recommended to have the gain margin as large as possible. A gain margin around –7 dB is sufficient.

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REVISION HISTORY

Number	Date	Description
4	September 29, 2015	Updated Output Current and Voltage (p. 18), Boost Frequency Dithering (p. 22), LED Regulation Voltage and Output Hysteresis (p. A-17), and LED Voltage Fault Status (p. A-19).
5	June 3, 2016	Updated Application C diagram (p. 31).
6	June 10, 2016	Updated NC terminal function description in Terminal List table (p. 5).
7	November 15, 2016	Updated Figures 4a and 4b (p. 19-20).
8	January 19, 2017	Updated Switch Leakage Current maximum value for first condition row (p. 6).
9	February 10, 2017	Corrected figure numbers in Functional Description (p. 17). Added Note 3 to LED Enable_L section (page A-8).
10	July 7, 2017	Updated Table A-1 footnote (p. A-7).
11	October 24, 2017	Updated Soft-Start Timing section (p. 24); added Order of Reading and Writing Registers and Dealing with Incomplete Transmission sections (p. A-4); corrected typo in Register Map (p. A-6).
12	July 2, 2018	Updated ADDR Pull-Up Current values (p. 8).
13	July 12, 2019	Minor editorial updates.

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