

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

60 V, 2.6 A, 116 mΩ

## FDN86501LZ

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 116 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2.6\text{ A}$
- Max  $r_{DS(on)}$  = 173 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 2.1\text{ A}$
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- Primary DC-DC Switch
- Load Switch

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

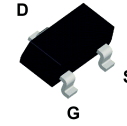
Symbol	Parameter	Ratings	Unit	
$V_{DS}$	Drain to Source Voltage	60	V	
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V	
$I_D$	Continuous (Note 1a)	2.6	A	
	Pulsed (Note 4)	24		
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ	
$P_D$	Power Dissipation	(Note 1a)	1.5	W
		(Note 1b)	0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

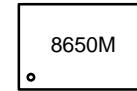
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ\text{C/W}$

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
60 V	116 mΩ @ 10 V	2.6 A
	173 mΩ @ 4.5 V	



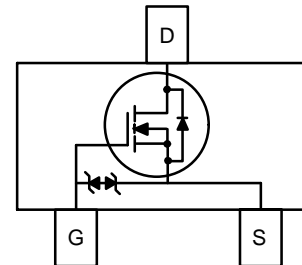
SOT-23/SUPERSOT™-23, 3 LEAD, 1.4x2.9  
CASE 527AG

### MARKING DIAGRAM



8650 = Specific Device Code  
M = Date Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDN86501LZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	68	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±10	μA

## ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	1.9	2.4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–5	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A	–	89	116	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.1 A	–	121	173	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A, T <sub>J</sub> = 125°C	–	152	198	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.6 A	–	8	–	S

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	236	335	pF
C <sub>oss</sub>	Output Capacitance		–	77	110	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	4.9	10	pF
R <sub>g</sub>	Gate Resistance		0.1	0.8	2.0	Ω

## SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.6 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	4.4	10	ns
t <sub>r</sub>	Rise Time		–	1.2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	9.6	20	ns
t <sub>f</sub>	Fall Time		–	1.2	10	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.6 A	–	3.8	5.4	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.6 A	–	1.9	2.7	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2.6 A	–	0.7	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	0.6	–	nC

## DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.6 A (Note 2)	–	0.9	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 2.6 A, di/dt = 100 A/μs	–	31	50	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	19	31	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 80°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 180°C/W when mounted on a minimum pad.

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
- E<sub>AS</sub> of 6 mJ is based on starting T<sub>J</sub> = 25°C, L = 3 mH, I<sub>AS</sub> = 2 A, V<sub>DD</sub> = 60 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 9 A.
- Pulsed I<sub>d</sub> please refer to Figure 11 SOA graph for more details.

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## TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

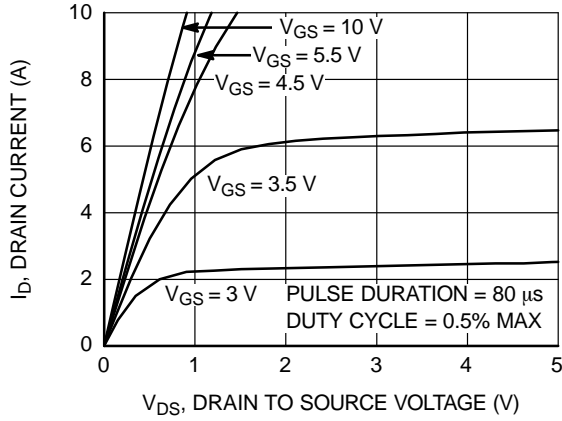


Figure 1. On-Region Characteristics

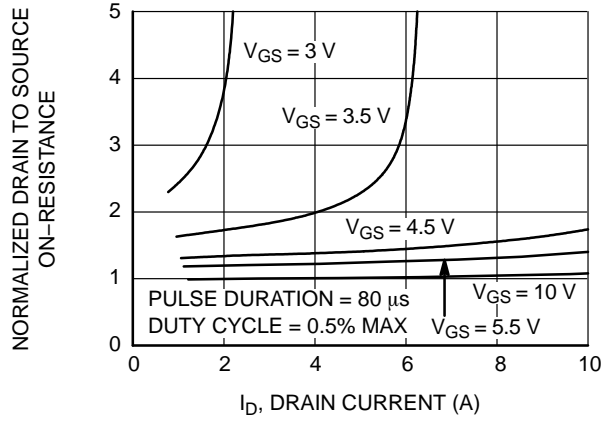


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

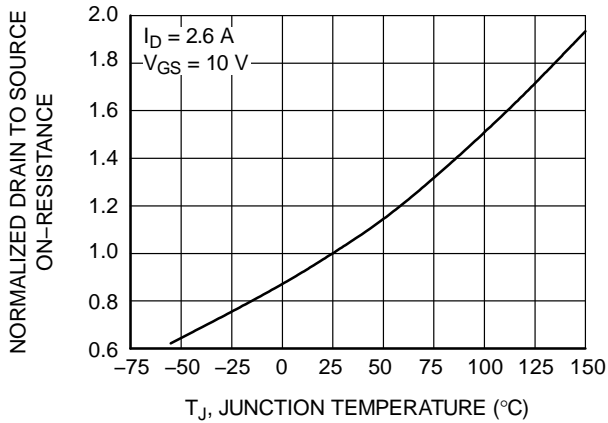


Figure 3. Normalized On-Resistance vs. Junction Temperature

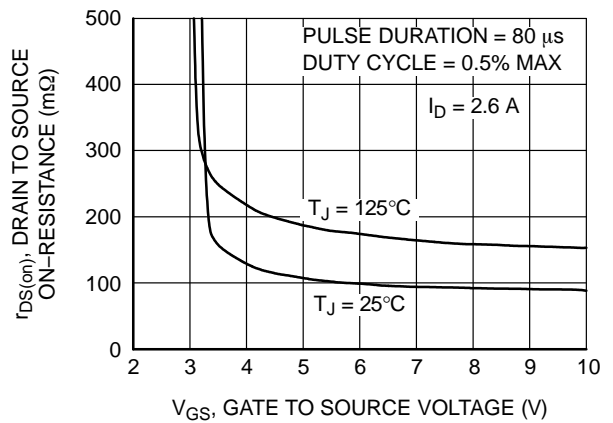


Figure 4. On-Resistance vs. Gate to Source Voltage

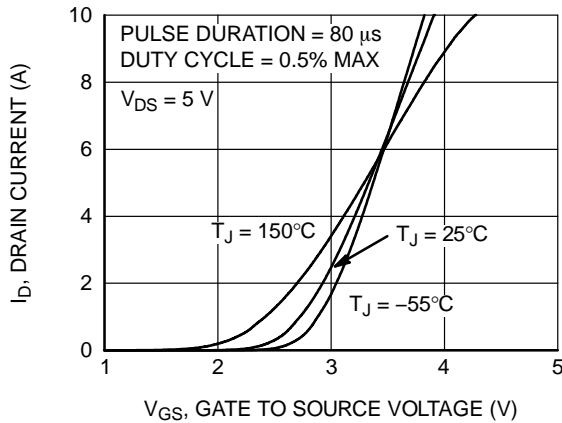


Figure 5. Transfer Characteristics

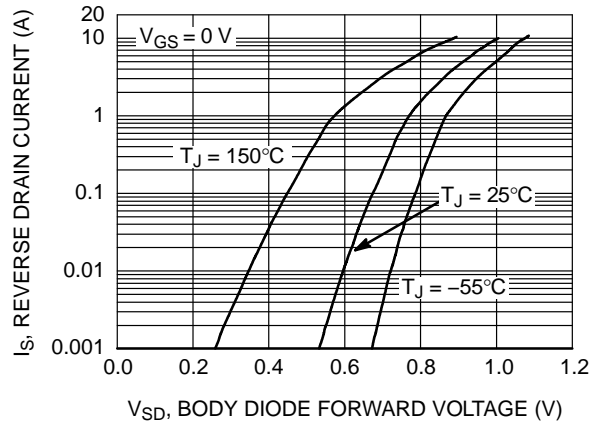


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDN86501LZ

## TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

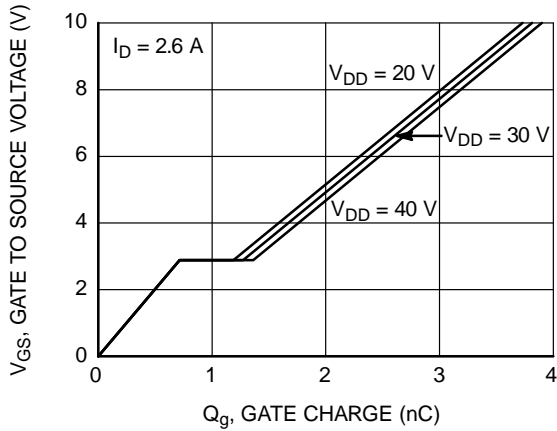


Figure 7. Gate Charge Characteristics

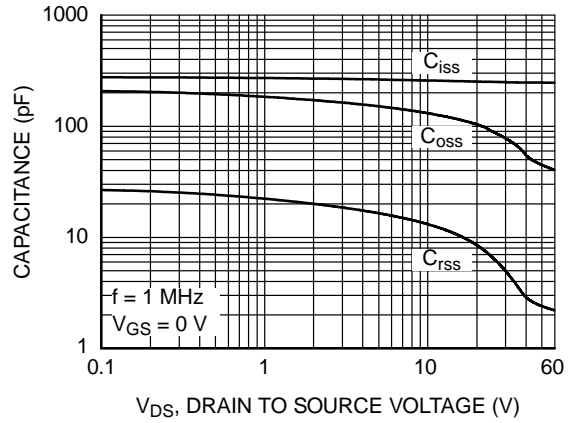


Figure 8. Capacitance vs. Drain to Source Voltage

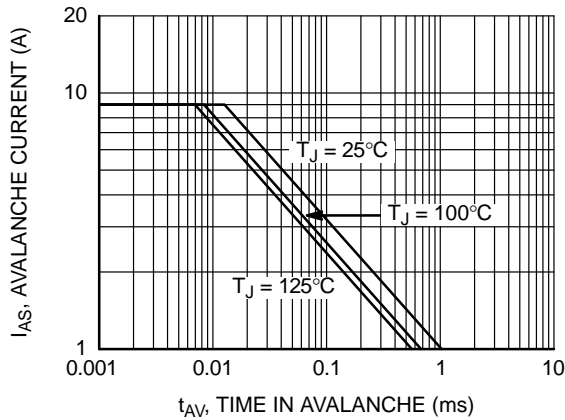


Figure 9. Unclamped Inductive Switching Capability

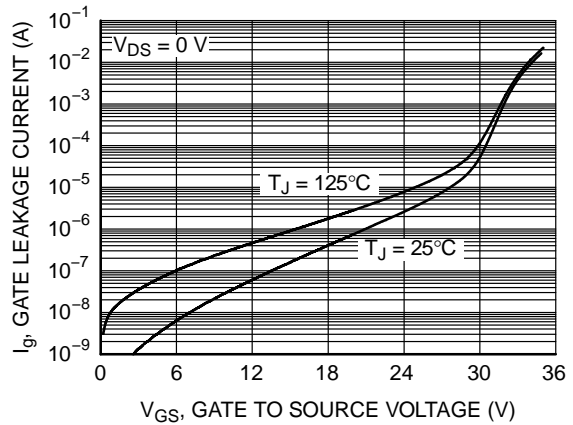


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

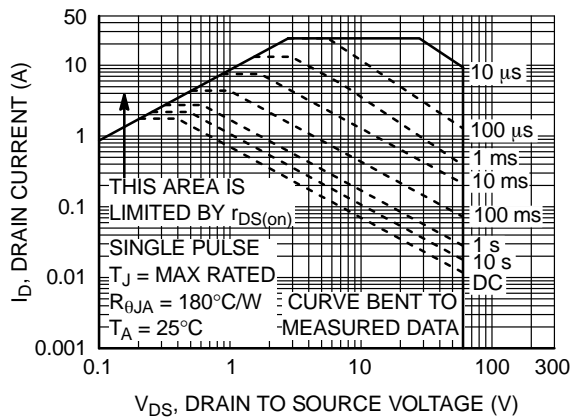


Figure 11. Forward Bias Safe Operating Area

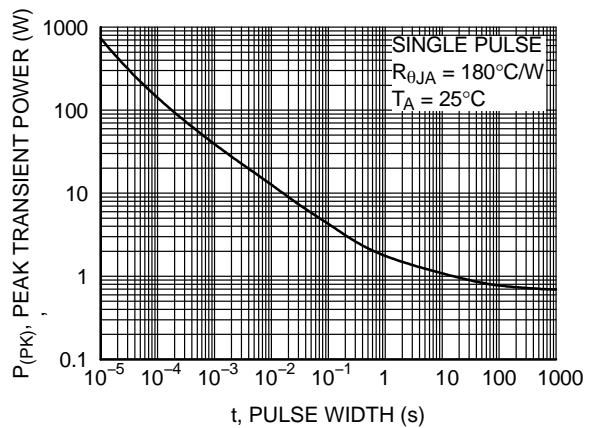


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS

(T<sub>J</sub> = 25°C unless otherwise noted) (continued)

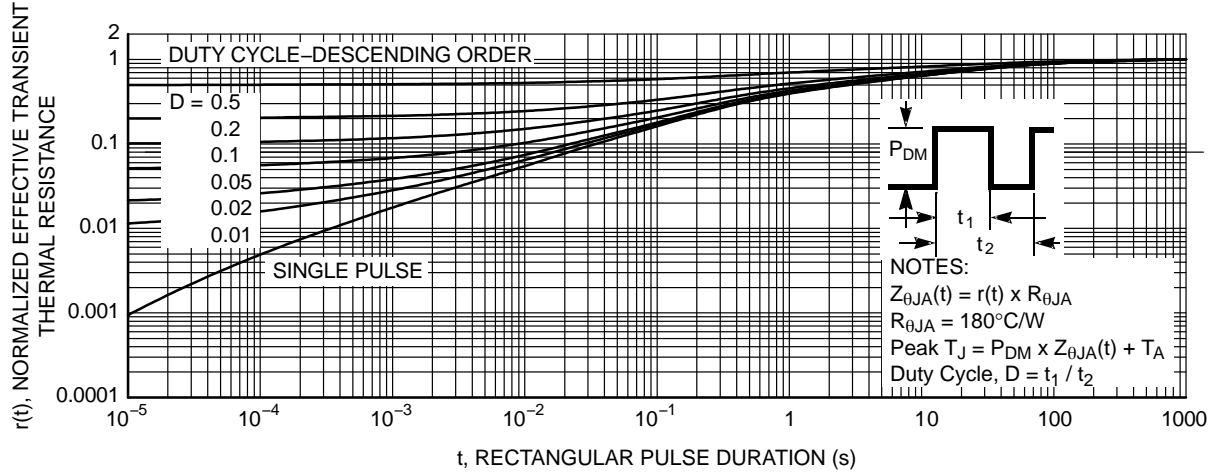


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDN86501LZ	8650	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

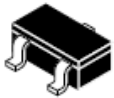
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

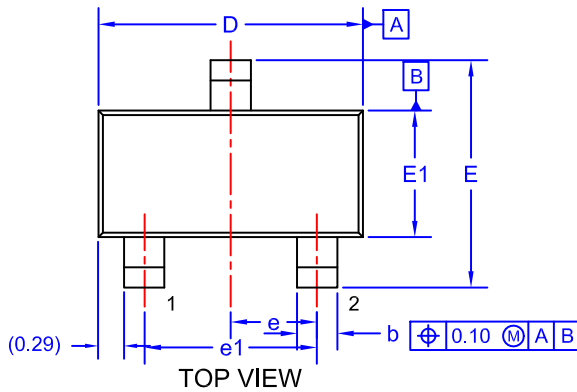
ON Semiconductor®



### SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9

CASE 527AG  
ISSUE A

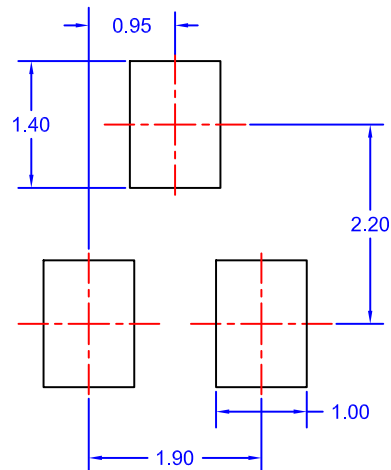
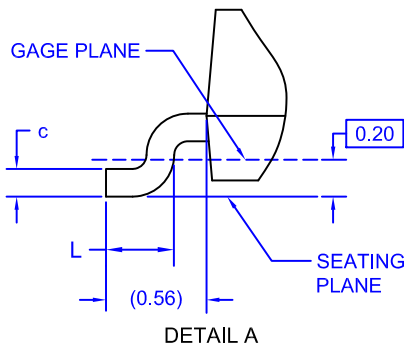
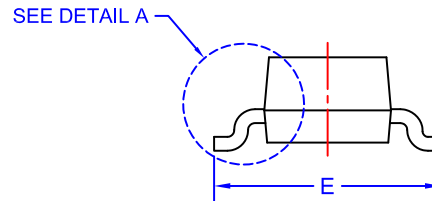
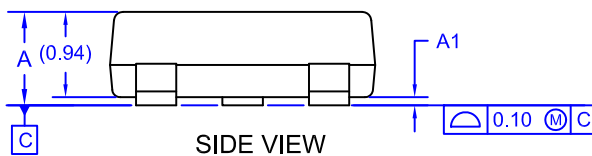
DATE 09 DEC 2019



NOTES: UNLESS OTHERWISE SPECIFIED

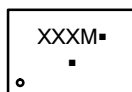
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43



\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Month Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9</b>	<b>PAGE 1 OF 1</b>

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