TPS81256 3-W, High Efficiency Step-Up Converter In MicroSiP™ Packaging

1 Features

- 91% Efficiency at 4MHz Operation
- Wide V_{IN} Range From 2.5V to 5.5V
- I_{OUT} ≥550mA at V_{OUT} = 5.0V, V_{IN} ≥3.3V
- Fixed Output Voltage 5.0V
- ±2% Total DC Voltage Accuracy
- 43µA Supply Current
- *Best-in-Class* Line and Load Transient
- V_{IN} ≥ V_{OUT} Operation
- Low-Ripple Light-Load PFM Mode
- True Load Disconnect During Shutdown
- Thermal Shutdown and Overload Protection
- Sub 1-mm Profile Solution
- Total Solution Size <9mm^2
- 9-Pin MicroSiP Packaging

2 Applications

- Cell Phones, Smart-Phones, Tablet PCs
- Mono and Stereo APA Applications
- USB-OTG, HDMI Applications
- USB Charging Port (5V)

3 Description

The TPS81256 device is a complete MicroSiP DC/DC step-up power solution intended for battery-powered portable applications. Included in the package are the switching regulator, inductor and input/output capacitors. Only a tiny additional output capacitor is required to finish the design.

The TPS81256 is based on a high-frequency synchronous step-up DC/DC converter optimized for battery-powered portable applications.

The DC/DC converter operates at a regulated 4-MHz switching frequency and enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the supply current to 43µA (typical) during light load operation. Intended for low-power applications, the TPS81256 supports more than 3W output power over a full Li-Ion battery voltage range. Input current in shutdown mode is less than 1µA (typical), which maximizes battery life.

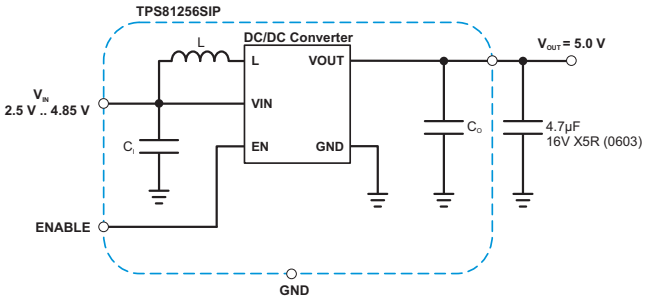
The TPS81256 offers a very small solution size of less than 9mm^2 due to minimum amount of external components. The solution is packaged in a compact (2.6mm x 2.9mm) and low profile (1.0mm) BGA package suitable for automated assembly by standard surface mount equipment.

Device Information(1)

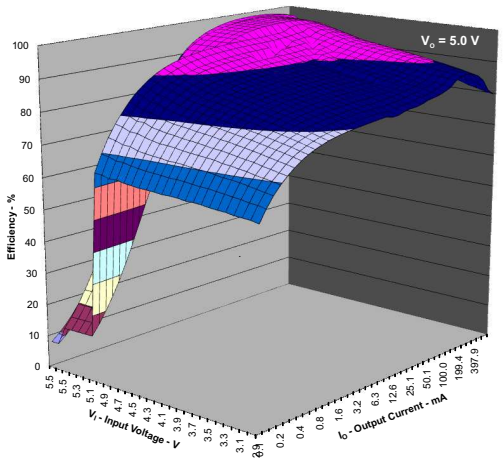
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS81256	µSIP (9)	2.925 mm × 2.575 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2016) to Revision D — **Page**

- Updated package drawing ... 22

Changes from Revision B (February 2015) to Revision C — **Page**

- Reversed D & E dimensions in to match MECHANICAL DATA drawing; and, changed "8-bump" to "9-bump" in the description. ... 21
- Added Community Resources section ... 21

Changes from Revision A (August 2013) to Revision B — **Page**

- Added *Device Information and ESD Ratings tables, Feature Description section, Device Functional Modes, Application and Implementation section, System Examples, Power Supply Recommendations section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.* ... 1
- Changed the pinout drawing to match the device orientation shown on the MECHANICAL DATA drawing. ... 3
- Changed SIP Package "Top View" image orientation to correctly match "YML LSB" symbolization with pin A1. ... 21

Changes from Original (June 2012) to Revision A — **Page**

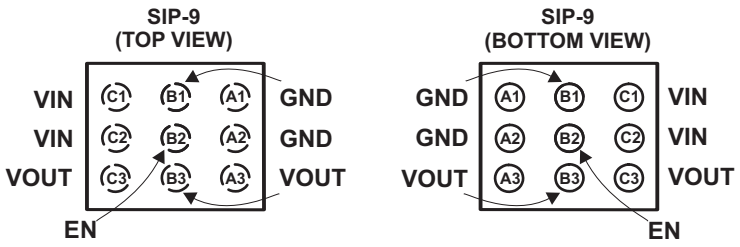
- Added animated performance characteristics table ... 6
- Deleted MLCC capacitor B1 life documentation ... 19

5 Device Options

PART NUMBER	OUTPUT VOLTAGE	PACKAGE MARKING CHIP CODE
TPS81256	5.0V	TT

6 Pin Configuration and Functions

SIP Package
9-Pin µSIP



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
GND	A1, A2, B1		Ground pin.
VIN	C1, C2	I	Power supply input.
VOUT	A3, B3, C3	O	Boost converter output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	Voltage at VIN(2), VOUT(2), EN(2)	–0.3	6	V
Input current	Continuous average current into VIN(3)		1.05	A
	Pulsed current into VIN(4)		1.3	A
Power dissipation		Internally limited		
Operating temperature, T_A(3)(4)(5)		–40	85	°C
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Limit the junction and the (top side) inductor case temperature to 110°C, limit the (top side) capacitor case temperature to 85°C for 2000h operation at maximum output power. Contact TI for more details on lifetime estimation.
(4) Limit the (top side) inductor case temperature to 140°C and the (top side) capacitor temperature to 115°C for 100h operation. Contact TI for more details on lifetime estimation.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 125°C, a maximum inductor case temperature of 125°C and a maximum capacitor case temperature of 85°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine Model - (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.5		5.5	V
R_L	Minimum resistive load for start-up ($V_I \le 4.8V$)	65			Ω
C_{EXT}	Output capacitance	2		30	µF
T_A	Ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
T_{CASE_IND}	Operating inductor case temperature			125	°C
T_{CASE_CAP}	Operating capacitor case temperature			85	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS81256 µSIP (SIP) – 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31	
ψ_{JT}	Junction-to-case (top) thermal resistance	–	

(1) Thermal data have been simulated with high-K board (per JEDEC standard).

7.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.5V to 5.5V, V_{OUT} = 5.0V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 5.0V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current into V_{IN} (1)	I_{OUT} = 0mA, V_{OUT} = 5.0V, V_{IN} = 3.6V EN = V_{IN} Device not switching		30	50	µA
	Operating quiescent current into V_{OUT} (1)			7	20	µA
I_{SD}	Shutdown current(1)	EN = GND		0.85	5.0	µA
V_{UVLO}	Under-voltage lockout threshold	Falling		2.0	2.1	V
		Hysteresis		0.1		V
ENABLE						
V_{IL}	Low-level input voltage				0.4	V
V_{IH}	High-level input voltage		1.0			V
I_{lkg}	Input leakage current	Input connected to GND or V_{IN}			0.5	µA
OUTPUT						
V_{OUT}	Regulated DC output voltage	2.5V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA PWM operation. Open Loop	4.92	5	5.08	V
		3.3V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 550mA PFM/PWM operation	4.85	5	5.2	V
		2.9V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 450mA PFM/PWM operation	4.85	5	5.2	V
ΔV_{OUT}	Power-save mode output ripple voltage	PFM operation, I_{OUT} = 1mA		35		mVpk
	PWM mode output ripple voltage	PWM operation, I_{OUT} = 200mA		8		mVpk
POWER SWITCH						
$r_{DS(on)}$	Input-to-output On-resistance	V_I = 5.25 V. Device not switching		320		mΩ
I_{lkg}	Reverse leakage current into VOUT(1)	EN = GND			5	µA
I_{LIM}	Average input current limit	EN = V_{IN}. V_{IN} = 3.3V		1180		mA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
OSCILLATOR						
f_{OSC}	Oscillator frequency	V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 500mA		4		MHz
TIMING						
	Start-up time	I_{OUT} = 0mA Time from active EN to start switching		70		µs
		I_{OUT} = 0mA Time from active EN to V_{OUT}		400		µs

(1) Maximum values can vary over lifetime due to intrinsic capacitor ageing effects. For more details, refer to *Thermal and Reliability Information* section.

7.6 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current	Figure 1, Figure 3
		vs Input voltage	Figure 2
V_O	DC output voltage	vs Output current	Figure 4, Figure 5, Figure 6
		vs Input voltage	Figure 7
I_O	Maximum output current	vs Input voltage	Figure 8
ΔV_O	Peak-to-peak output ripple voltage	vs Output current	Figure 8
I_{CC}	Supply current	vs Input voltage	Figure 10
I_{LIM}	Input current	vs Output current	Figure 11

Table 2. Table of Animated Performance Characteristics

		VIDEO
AC Load Response	vs. Input Voltage	Video 1
Load Transient Response (10mA to 400mA)	vs. Input Voltage	Video 2
Load Transient Response (to 400mA)	vs. Base Load Current ($2.9V_{IN}$)	Video 3
	vs. Base Load Current ($3.6V_{IN}$)	Video 4
	vs. Base Load Current (4.2_{VIN})	Video 5
Start-Up Response	vs. Delay to Load Current ($2.9V_{IN}$)	Video 6
	vs. Delay to Load Current ($3.6V_{IN}$)	Video 7
	vs. Delay to Load Current ($4.2V_{IN}$)	Video 8
Start-Up Response (200mA I_{OUT})	vs. Input Voltage	Video 9
Overload Response	vs. Input Voltage	Video 10

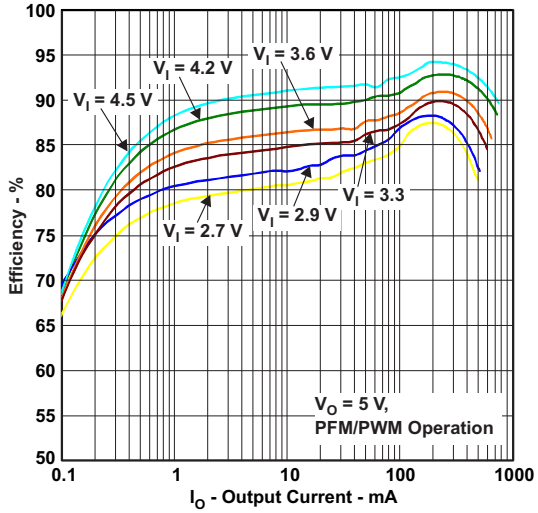


Figure 1. Efficiency vs Output Current

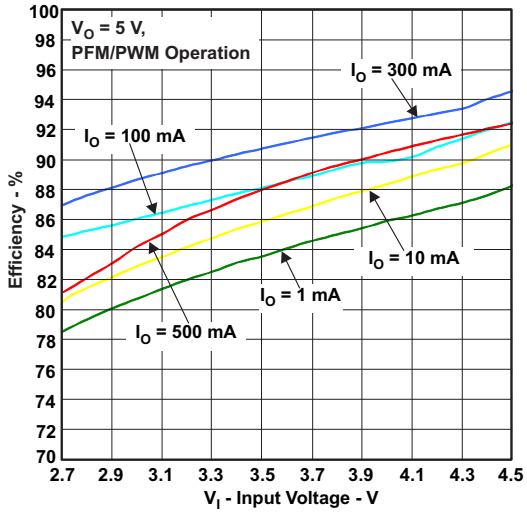


Figure 2. Efficiency vs Input Voltage

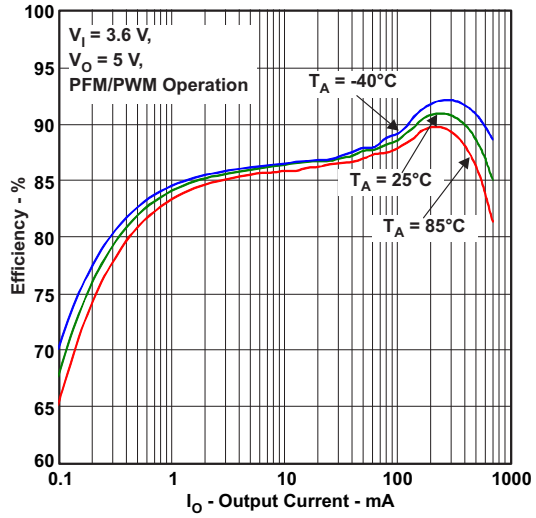


Figure 3. Efficiency vs Output Current

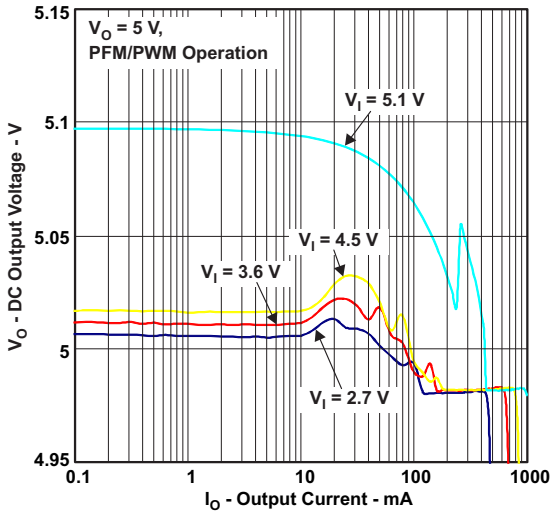


Figure 4. DC Output Voltage vs Output Current

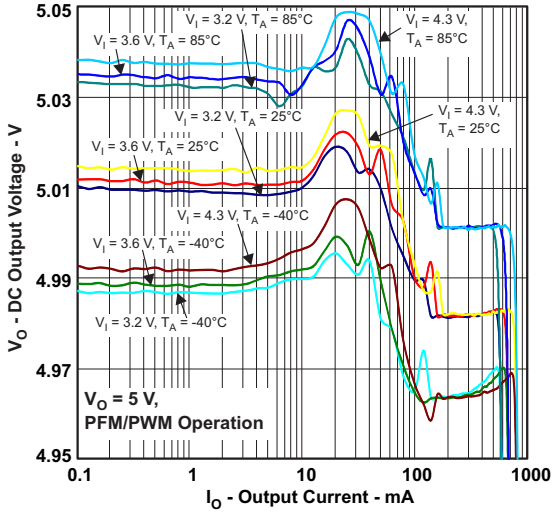


Figure 5. DC Output Voltage vs Output Current

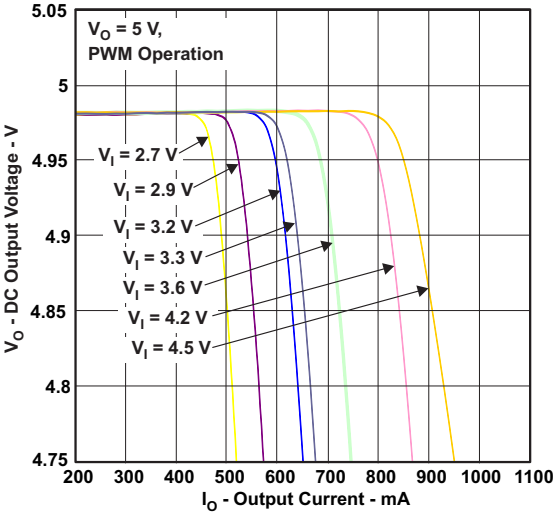


Figure 6. DC Output Voltage vs Output Current

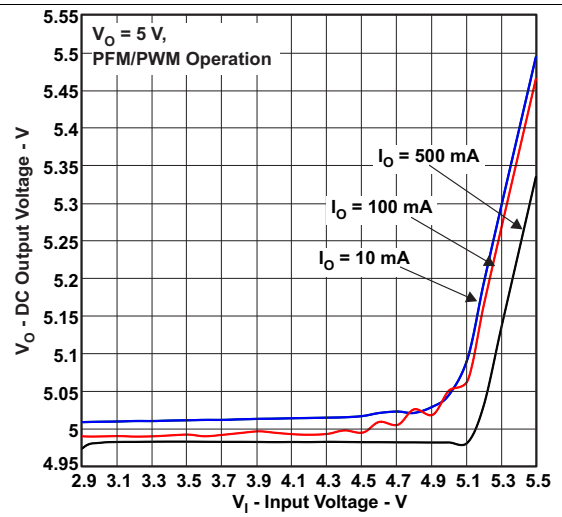


Figure 7. DC Output Voltage vs Input Voltage

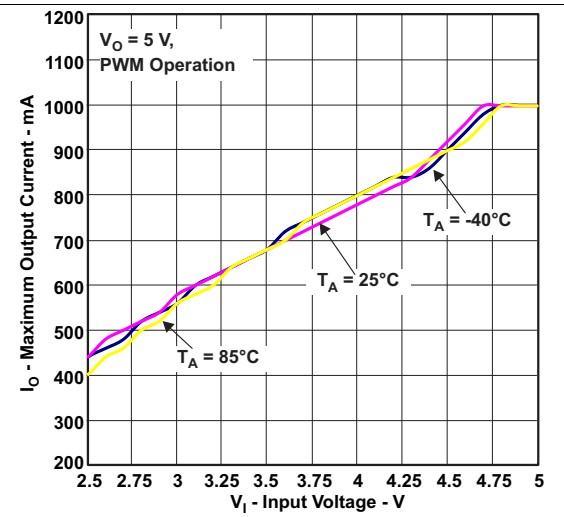


Figure 8. Maximum Output Current vs Input Voltage

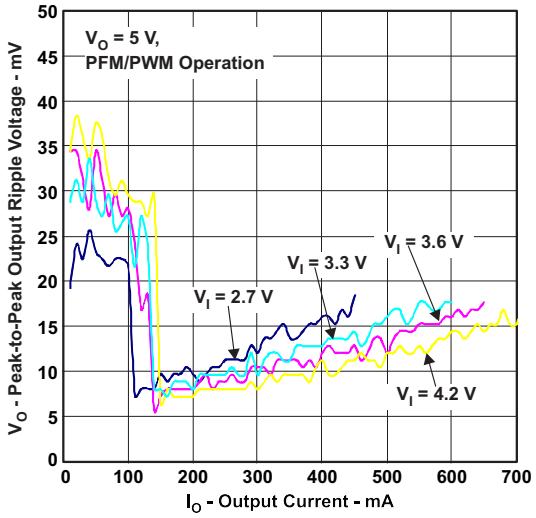


Figure 9. Peak-To-Peak Output Ripple Voltage vs Output Current

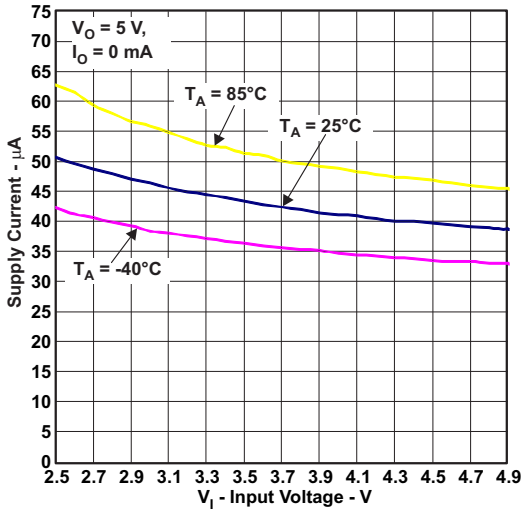


Figure 10. Supply Current vs Input Voltage

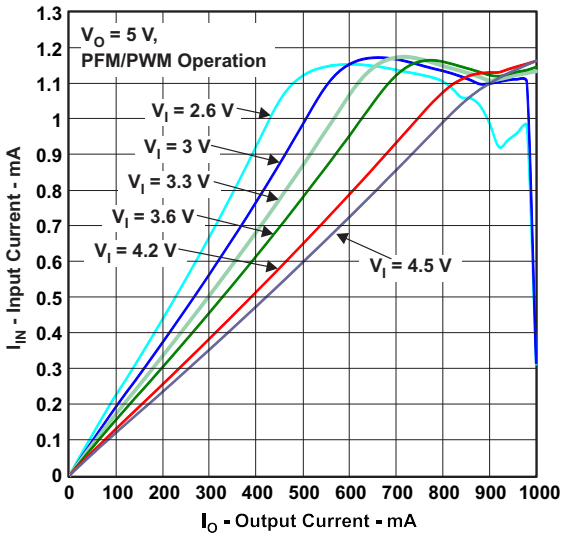


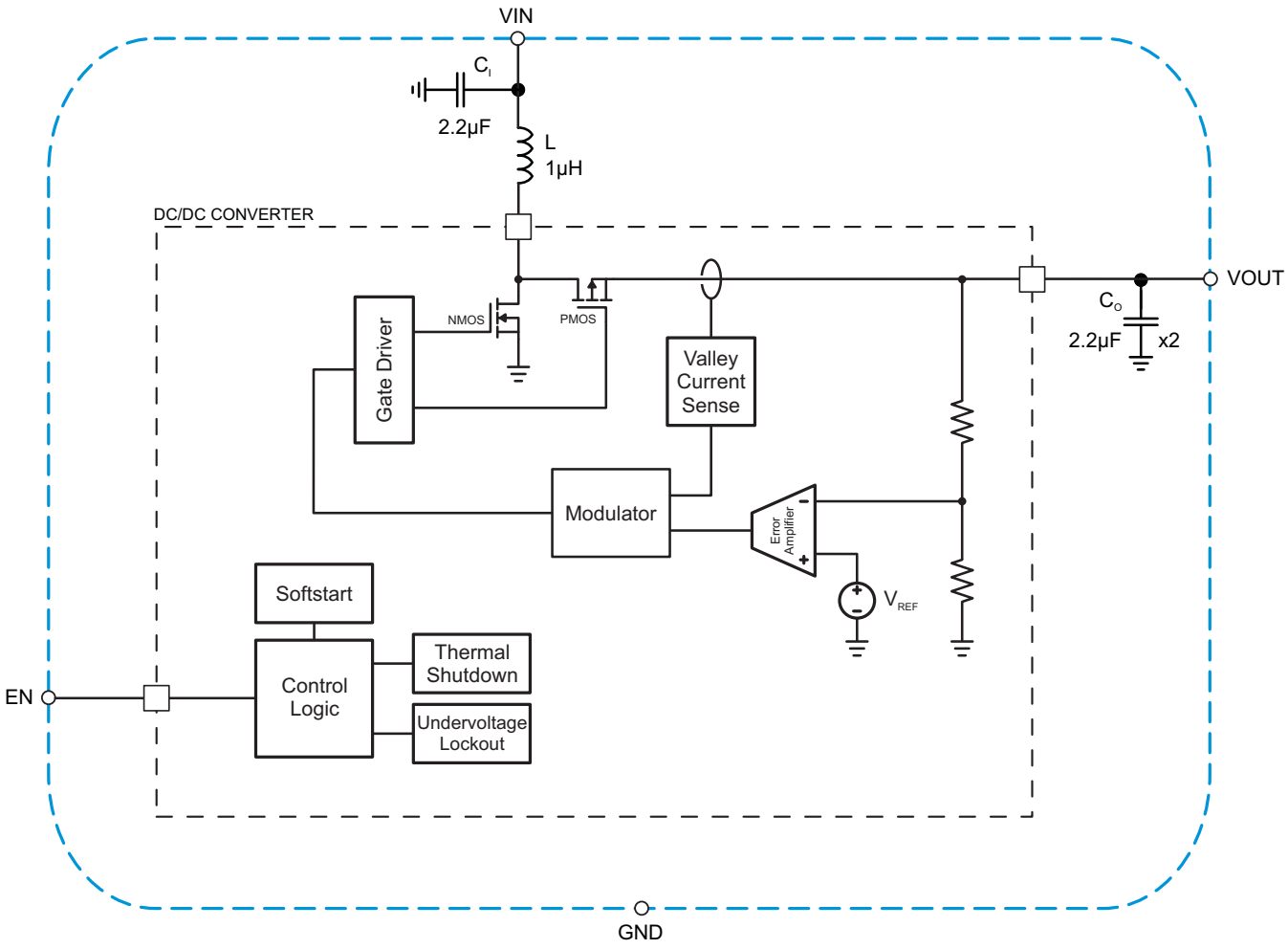
Figure 11. Input Current vs Output Current

8 Detailed Description

8.1 Overview

The TPS81256 is a stand-alone, synchronous, step-up converter module. The converter operates at a quasi-constant 4-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS81256 converter operates in power-save mode with pulse frequency modulation (PFM).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operation

During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time.

At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

Feature Description (continued)

In general, a dc/dc step-up converter can only operate in "true" boost mode, i.e. the output “boosted” by a certain amount above the input voltage. The TPS81256 device operates differently as it can smoothly transition in and out of zero duty cycle operation. Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive. In this operation mode, the output current capability of the regulator is limited to ca. 150mA. Refer to the typical characteristics section (DC Output Voltage vs. Input Voltage) for further details.

The current mode architecture with adaptive slope compensation provides excellent transient load response while requiring only one external tiny capacitor for output filtering and loop stability purposes. Internal soft-start and loop compensation simplifies the application design process.

8.3.2 Power-Save Mode

The TPS81256 integrates a power-save mode to improve efficiency at light load. In power-save mode the converter only operates when the output voltage trips below a set threshold voltage.

It ramps up the output voltage with several pulses and goes into power save mode when the output voltage exceeds the set threshold voltage.

PFM mode is exited and the PWM mode entered in case the output current can no longer be supported in PFM mode.

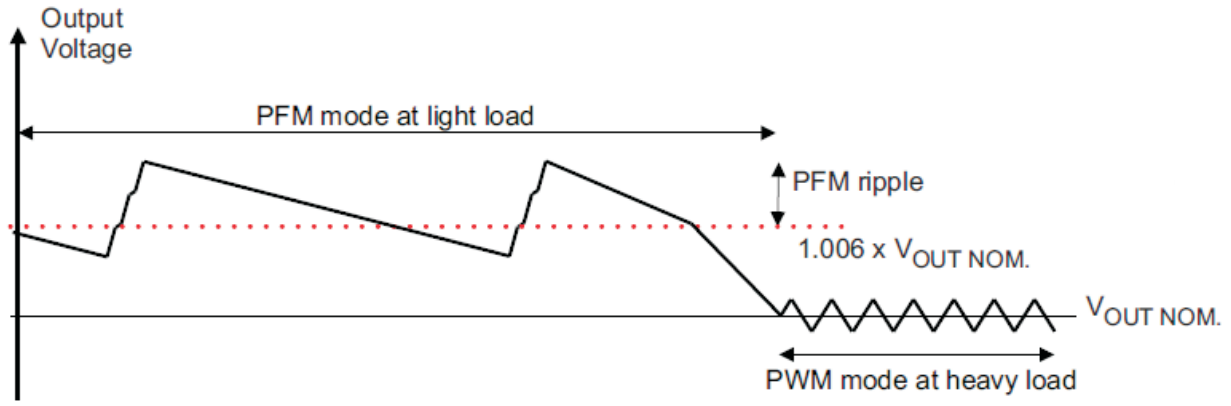


Figure 12. Power-Save Example

8.3.3 Current Limit Operation, Maximum Output Current

The TPS81256 directly and accurately controls the average input current through intelligent adjustment of the valley current limit. The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(DC)} = I_{IN(CL)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \eta \quad (1)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

8.4 Device Functional Modes

8.4.1 Softstart, Enable

The TPS81256 device starts operation when EN is set high and starts up with the soft-start sequence. For proper operation, the EN pin must be terminated and must not be left floating.

The TPS81256 device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (approx. 200mA) during this phase. This mechanism is used to limit the output current under short-circuit condition.

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

Pulling the EN pin low forces the device in shutdown, with a shutdown current of typically 1µA. In this mode, true load disconnect between the battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

8.4.2 Load Disconnect and Reverse Current Protection

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharge during shutdown. The advantage of TPS81256 is that this converter is disconnecting the output from the input of the power supply when it is disabled (so called true shutdown mode). In case of a connected battery it prevents it from being discharge during shutdown of the converter.

8.4.3 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typically 2.1V.

8.4.4 Thermal Regulation

The TPS81256 device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110°C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10°C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

8.4.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typically) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS81256 device is a complete MicroSiP™ DC/DC step-up power solution intended for battery-powered portable applications.

9.2 Typical Application

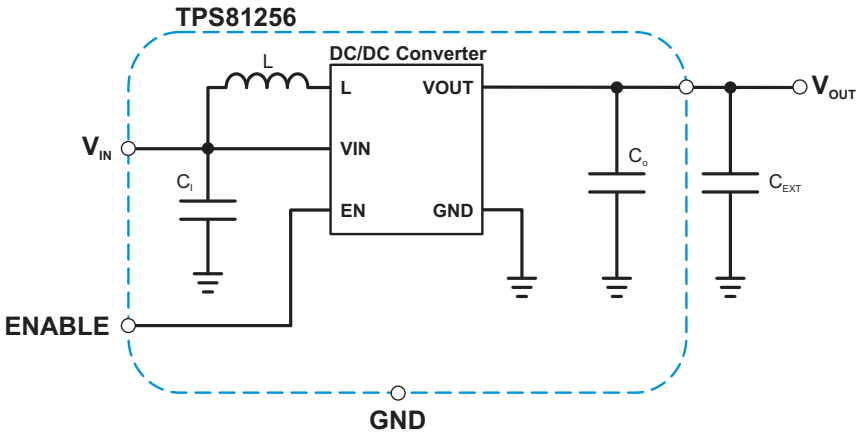


Figure 13. 5-V Power Supply

9.2.1 Design Requirements

The following design guidelines provide a component selection process for the typical application circuit shown to operate the device within the *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Capacitor Selection C_{EXT}

Because of the pulsating output current nature of the boost converter, a low ESR output capacitor is required to maintain control loop stability, to enhance the converter's transient response and to reduce the output voltage ripple. For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. The minimum capacitance is 2µF.

To get an estimate of the steady ripple due to charging and discharging the output capacitance, Equation 2 can be used.

$$\Delta V = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{C \cdot V_{OUT} \cdot f} \quad (2)$$

Where f is the switching frequency which is 4MHz (typically.) and C is the effective output capacitance. Notice the TPS81256 device already incorporates ca. 1.2µF effective output capacitance.

In practice, the total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 3:

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (3)$$

Typical Application (continued)

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed ca. 30µF.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 4.7µF X5R 16V 0603 MLCC capacitor would typically show an effective capacitance of less than 2.5µF (under 5V bias condition, high temperature and ageing effects).

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PWB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter small and large signal behavior must be checked over the input voltage range, load current range and temperature range.

The easiest sanity test is to evaluate, directly at the converter's output, the following aspects:

- PFM/PWM efficiency
- PFM/PWM and PWM load transient response

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Table 3. Recommended Capacitor C_{EXT}

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER(1)
C_{EXT}	4.7µF, 16V, 0603, X5R ceramic	GRM188R61C475KAAJ, muRata

(1) See *Third-Party Products Disclaimer*

9.2.2.2 Input Capacitor Selection

In a dc/dc boost converter, since the input current is continuous, only minimum input capacitance is required. The TPS81256 device integrates a low ESR decoupling capacitor to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.

For most applications, the input capacitor that is integrated into the TPS81256 should be sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input capacitance to find a remedy. Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Additional input capacitors should be located as close as possible to the device.

The TPS81256 uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

9.2.3 Application Curves

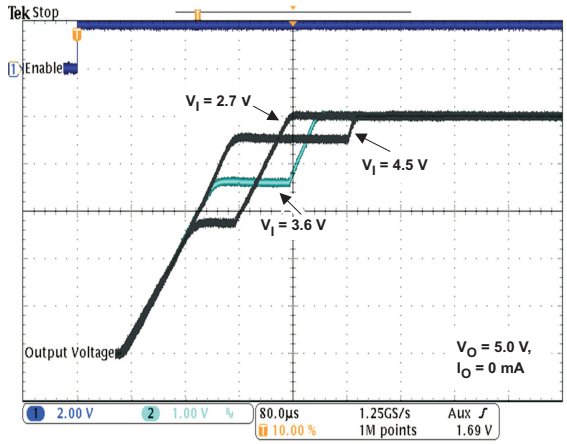


Figure 14. Start-Up

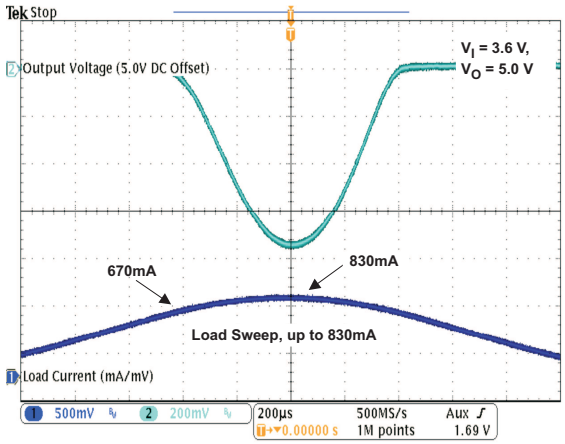


Figure 15. Overload Recovery Response

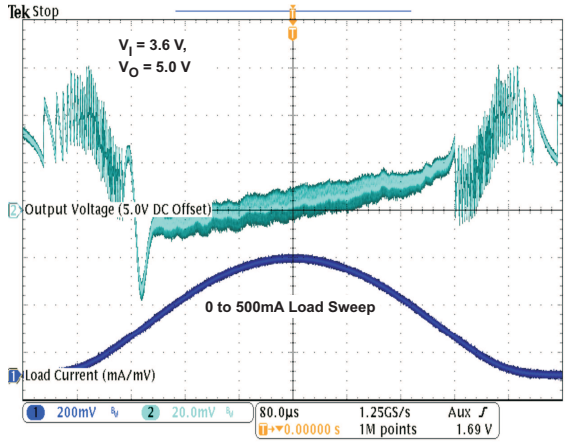


Figure 16. AC Load Transient

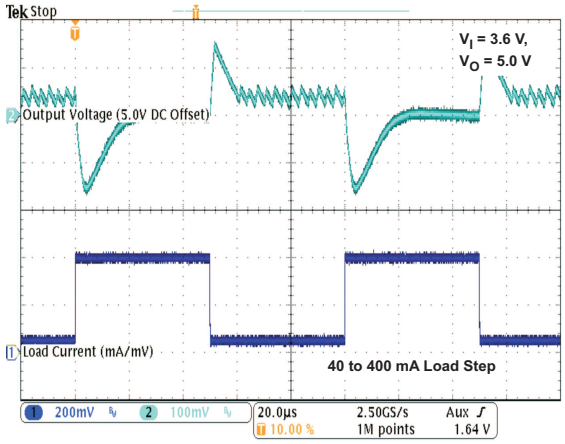


Figure 17. Load Transient Response In PFM/PWM Operation

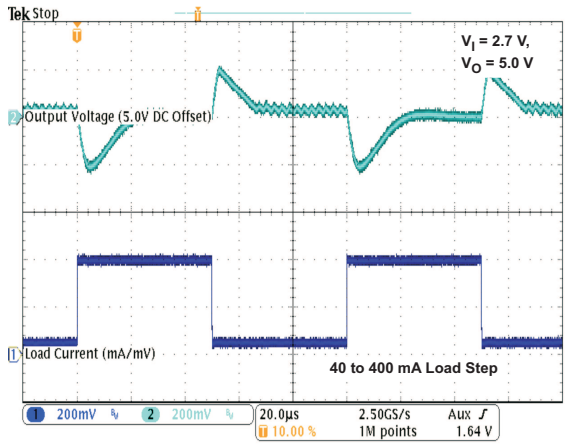


Figure 18. Load Transient Response In PFM/PWM Operation

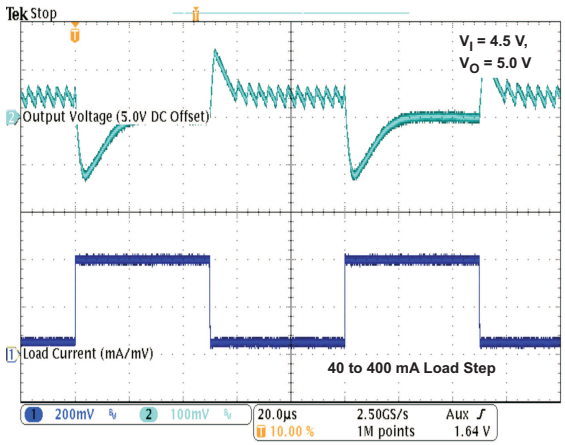


Figure 19. Load Transient Response In PFM/PWM Operation

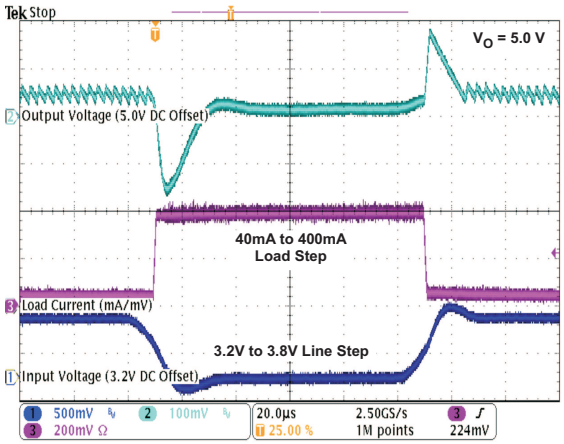
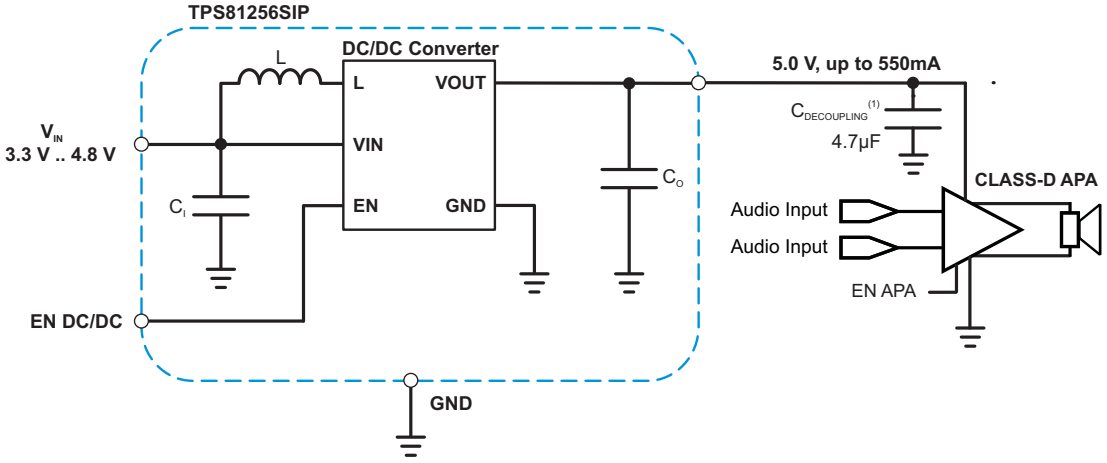


Figure 20. Combined Line/Load Transient Response

9.3 System Examples



(1) The capacitor is not only required to decouple the audio power amplifier, but is also required to stable operation of the SMPS converter. The SMPS converter should be located in the close vicinity of the audio power amplifier.

Figure 21. "Boosted" Audio Power Supply

System Examples (continued)

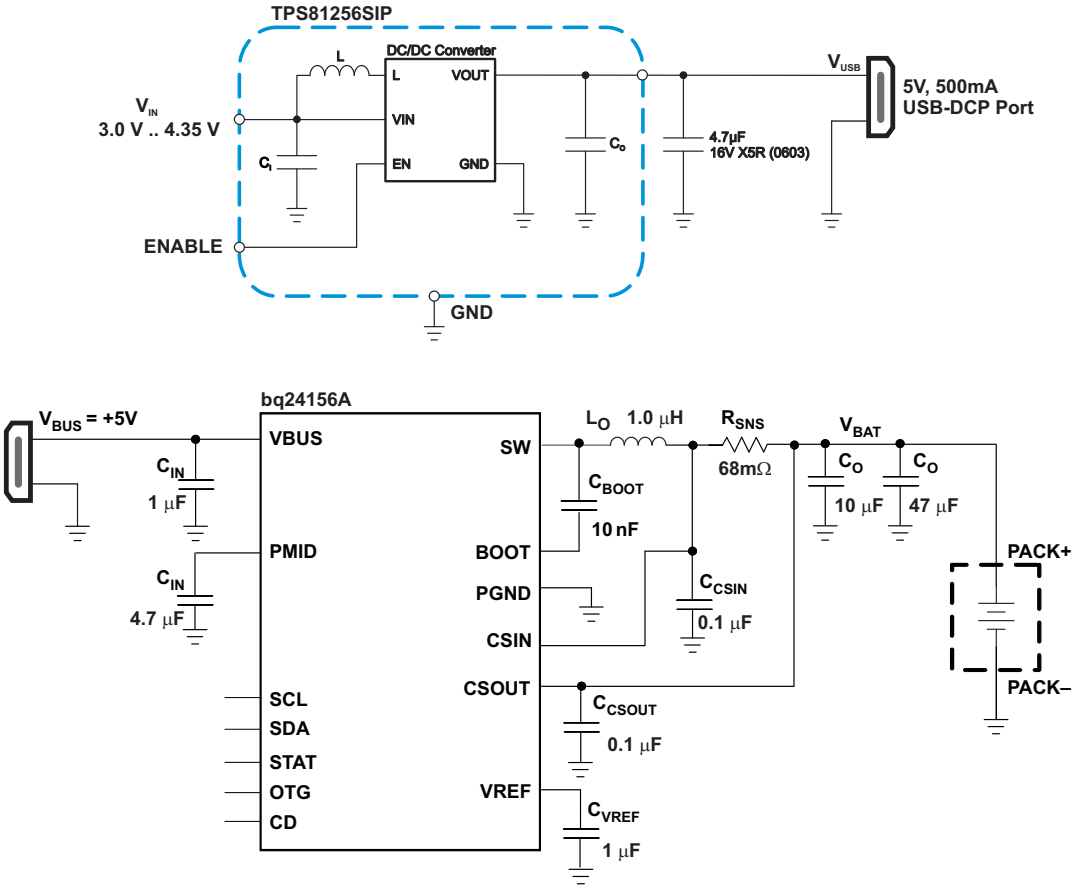


Figure 22. Battery Powered USB-DCP Power Supply

10 Power Supply Recommendations

The TPS81256 has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS81256

11 Layout

11.1 Layout Guidelines

In making the pad size for the µSiP LGA balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 23 shows the appropriate diameters for a MicroSiP layout.

11.2 Layout Example

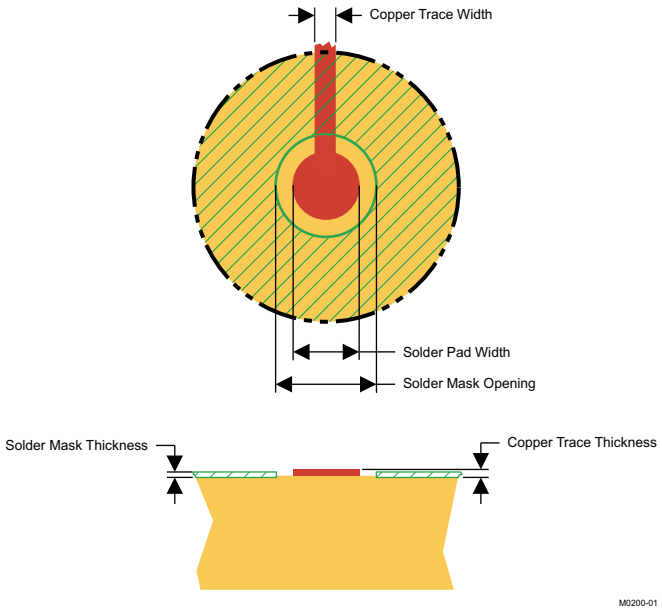


Figure 23. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

11.3 Surface Mount Information

The TPS81256 MicroSiP DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum thereby to allow the MicroSiP device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

11.4 Thermal and Reliability Information

The TPS81256 output current may need to be de-rated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current de-rating is dependent upon the input voltage, output power and environmental thermal conditions. Care should especially be taken in applications where the localized PWB temperature exceeds 65°C.

The TPS81256 die and inductor temperature should be kept lower than the maximum rating of 125°C, so care should be taken in the circuit layout to ensure good heat sinking. Sufficient cooling should be provided to ensure reliable operation.

To estimate the junction temperature, approximate the power dissipation within the TPS81256 by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking a power measurement if you have an actual TPS81256 device or a TPS81256EVM evaluation module. Then calculate the internal temperature rise of the TPS81256 above the surface of the printed circuit board by multiplying the TPS81256 power dissipation by the thermal resistance.

The thermal resistance numbers listed in the Thermal Information table are based on modeling the MicroSiP package mounted on a high-K test board specified per JEDEC standard. For increased accuracy and fidelity to the actual application, it is recommended to run a thermal image analysis of the actual system. Figure 24 and Figure 25 are thermal images of TI's evaluation board with readings of the temperatures at specific locations on the device.

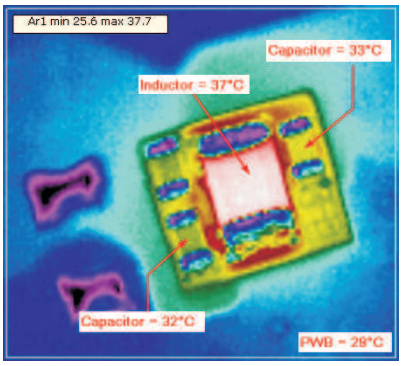


Figure 24. V_{IN}=3.6v, V_{OUT}=5v, I_{OUT}=300ma
150mw Power Dissipation At Room Temperature

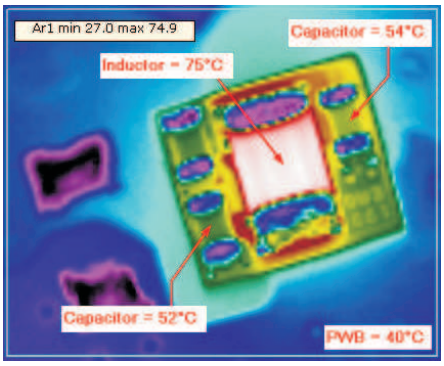


Figure 25. V_{IN}=3.6v, V_{OUT}=5v, I_{OUT}=600ma
600mw Power Dissipation At Room Temperature

The TPS81256 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, it follows that prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the components internal to the MicroSiP™ package are subjected to high temperatures for prolonged or repetitive intervals, which may damage or impair the reliability of the device.

MLCC capacitor reliability/lifetime is dependant on temperature and applied voltage conditions. At higher temperatures, MLCC capacitors are subject to stronger stress. On the basis of frequently evaluated failure rates determined at standardized test conditions, the reliability of all MLCC capacitors can be calculated for their actual operating temperature and voltage.

Thermal and Reliability Information (continued)

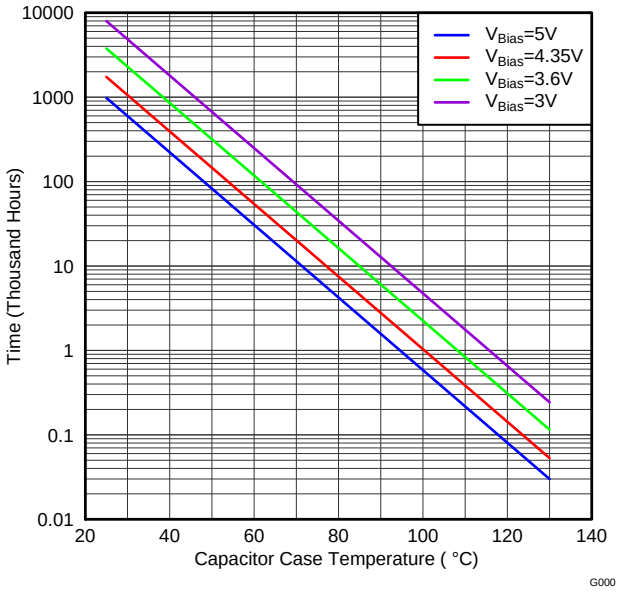


Figure 26. Capacitor Lifetime vs Capacitor Case Temperature

Failures caused by systematic degradation can be described by the Arrhenius model. The most critical parameter (IR) is the Insulation Resistance (i.e. leakage current). The drop of IR below a lower limit (e.g. 1 MΩ) is used as the failure criterion, see Figure 26. It should be noted that the wear-out mechanisms occurring in the MLCC capacitors are not reversible but cumulative over time.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

MicroSiP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

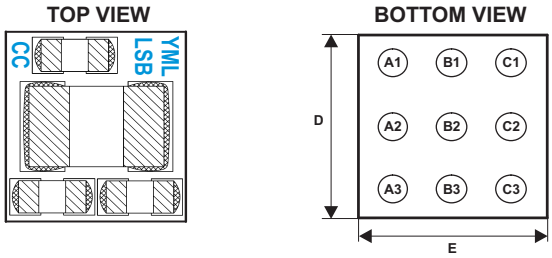
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MicroSiP DC/DC Module Package Dimensions

The TPS81256 device is available in a 9-bump ball grid array (BGA) package. The package dimensions are:

- D = 2.925 ±0.05 mm
- E = 2.575 ±0.05 mm



Code:

- CC — Package marking Chip Code (see Package Option Addendum for more details)
- YML — Y: Year, M: Month, L: Lot trace code
- LSB — L: Lot trace code, S: Site code, B: Board locator

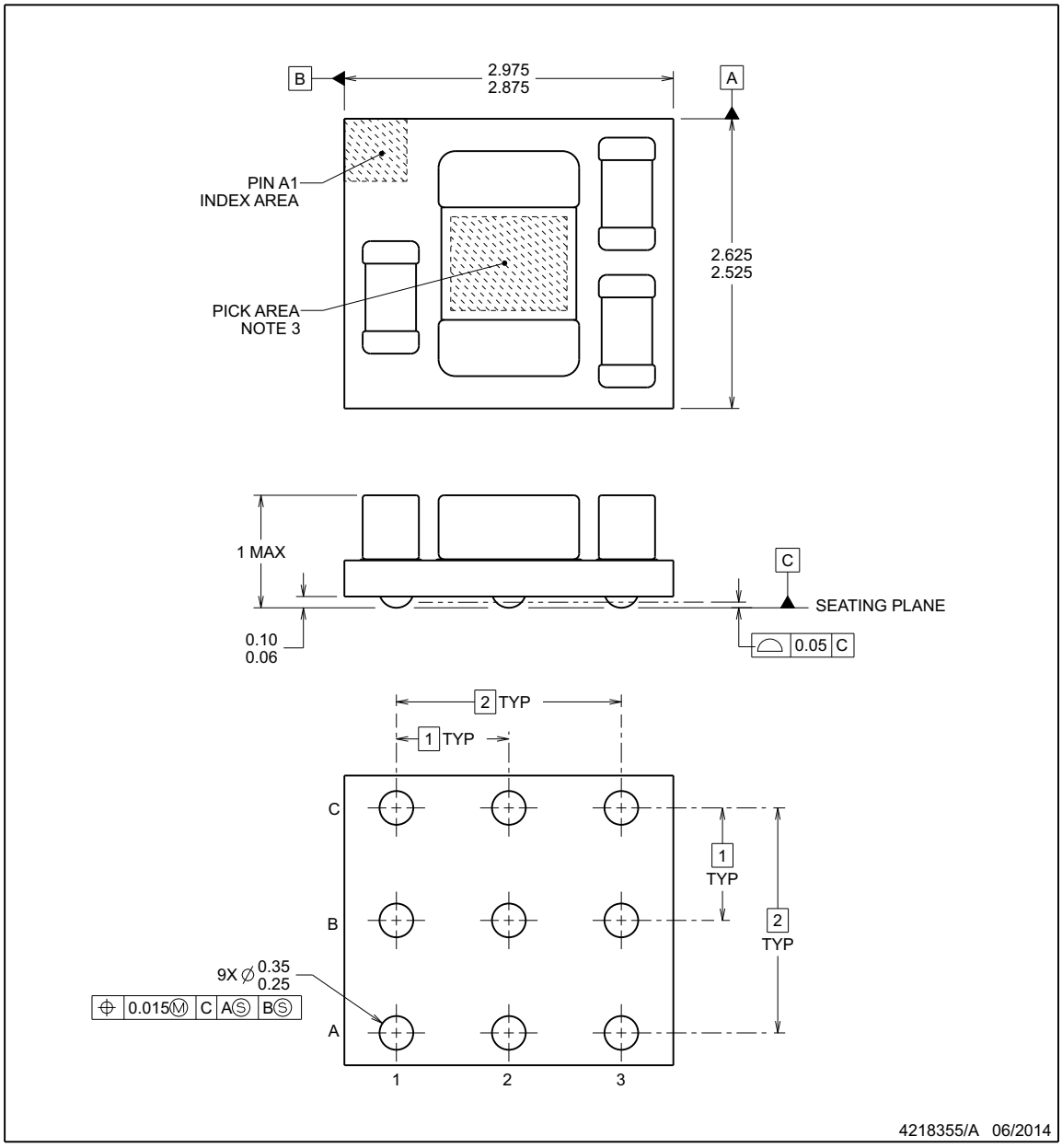
Figure 27. µSIP 9-Pin Dimensions and Markings

PACKAGE OUTLINE

SIP0009A

MicroSiP™ - 1 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments.

NOTES:

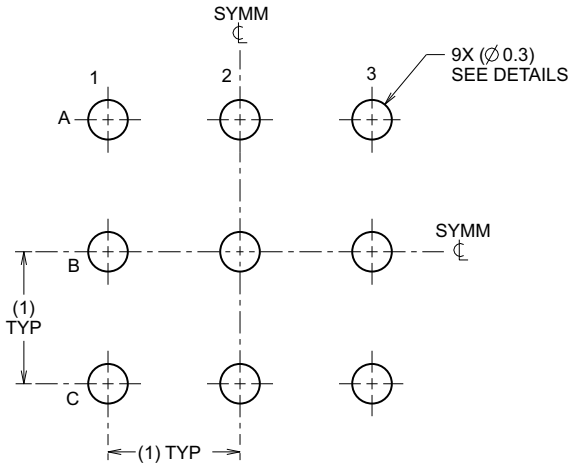
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. For pick and place nozzle recommendation, see product datasheet.
4. Location, size and quantity of each component are for reference only and may vary.

EXAMPLE BOARD LAYOUT

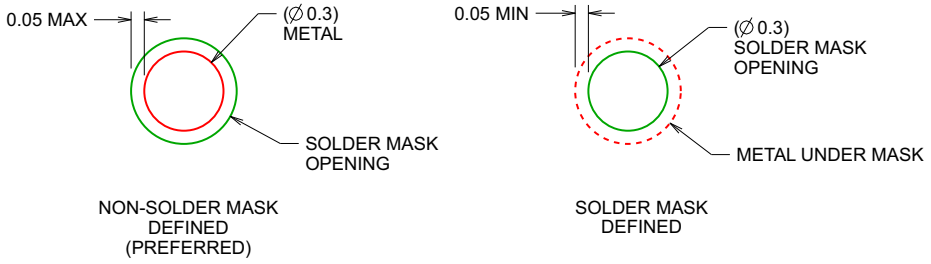
SIP0009A

MicroSiP™ - 1 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS
NOT TO SCALE

4218355/A 06/2014

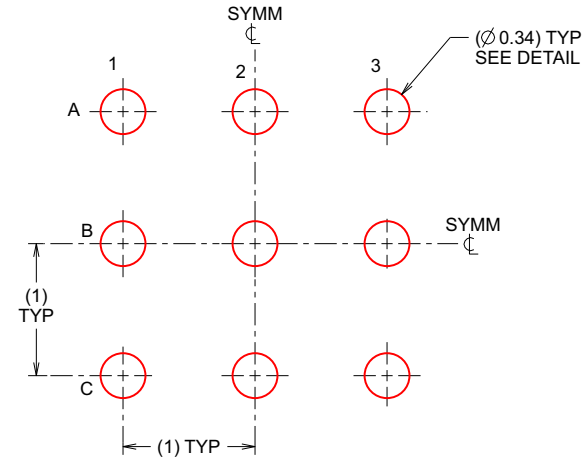
NOTES: (continued)

5. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

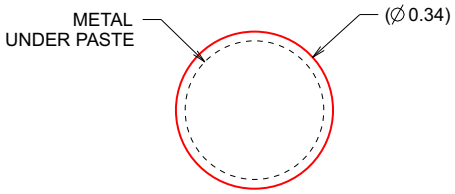
EXAMPLE STENCIL DESIGN

SIP0009A — **MicroSiP™ - 1 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X



SOLDER PASTE DETAIL
TYPICAL

4218355/A 06/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS81256SIPR	ACTIVE	uSiP	SIP	9	3000	RoHS (In Work) & Green (In Work)	OSP	Level-2-260C-1 YEAR	-40 to 85	TT	Samples
TPS81256SIPT	ACTIVE	uSiP	SIP	9	250	RoHS (In Work) & Green (In Work)	OSP	Level-2-260C-1 YEAR	-40 to 85	TT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

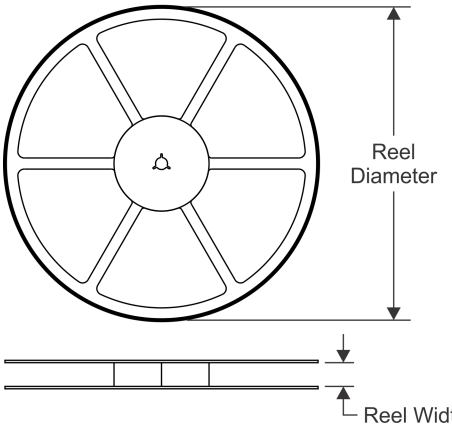
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

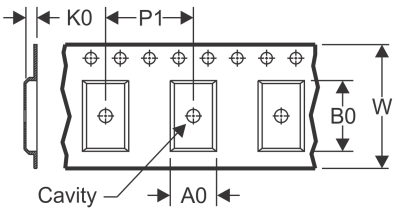
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

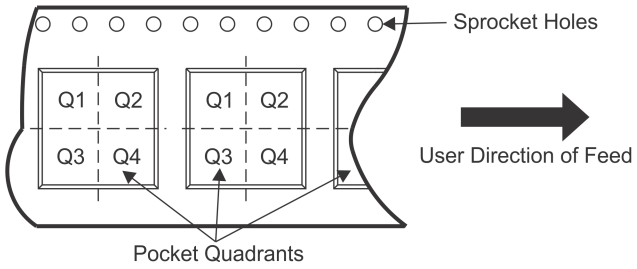


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

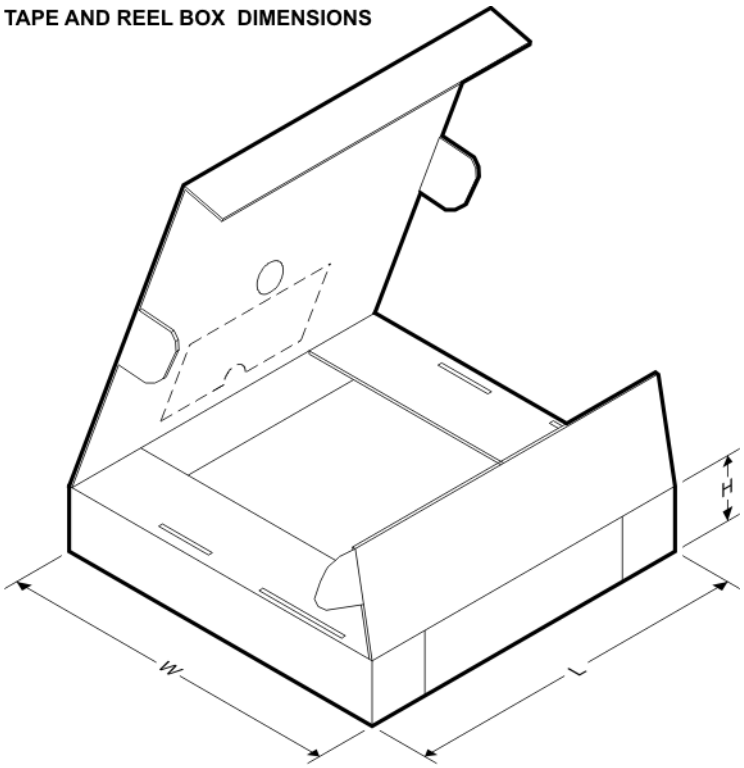
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS81256SIPR	uSiP	SIP	9	3000	178.0	9.0	2.83	3.18	1.2	4.0	8.0	Q2
TPS81256SIPT	uSiP	SIP	9	250	178.0	9.0	2.83	3.18	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS81256SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS81256SIPT	uSiP	SIP	9	250	223.0	194.0	35.0

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