PRODUCT CHANGE NOTIFICATION



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February 9, 2017

PCN#020917

Dear Sir/Madam:

Subject: Notification of Change to LTC3886 Die and Datasheet

Please be advised that Linear Technology Corporation has made enhancements to the LTC3886 product die to improve performance in the following areas:

- 1) Fix errata
- 2) Reduce power up times
- 3) Reduce the ADC update period
- 4) Improve on-chip EEPROM robustness

The documented errata in the LTC3886 are eliminated. Refer to the following link for the current errata documents <u>http://cds.linear.com/docs/en/spec-notice/er3886f.pdf</u>.

 T_{INIT} , the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 70ms to 35ms. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner.

The ADC update period, T_{CONVERT}, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters.

The above changes are shown on the attached pages of the marked up datasheet.

Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.

The new silicon can be identified by the MFR_SPECIAL_ID, PMBus command code 0xE7, with a value of 0x460* where * is a value of 8-F.

No changes were made to the analog sections of the LTC3886, and no PWM characteristics changed. The die changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised product will have successfully completed 1000 hours burn-in before production release.

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will consider this change notice accepted by April 09, 2017. Production shipments of product incorporating the improved die will begin no sooner than April 09, 2017.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail <u>JASON.HU@LINEAR.COM</u>.

Sincerely,

Jason Hu

Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS The \bullet denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, EXTV_{CC} = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Input Voltag	e						
VIN	Input Voltage Range	(Note 12)	٠	4.5		60	V
ΙQ	Input Voltage Supply Current Normal Operation	(Note 14) V _{RUN} = 3.3V, No Caps on TG and BG V _{RUN} = 0V			26 22		mA mA
V _{UVLO}	Undervoltage Lockout Threshold When $V_{\text{IN}} > 4.2V$	V _{INTVCC} Falling V _{INTVCC} Rising			3.7 3.95		v v
T _{INIT}	Initialization Time	Delay from RESTORE_USER_ALL, MFR_REST, or V _{INTVCC} > V _{UVLO} Until TON_DELAY Can Begin			-70 35	5	ms
Control Loop	p						
V _{OUTRO}	Range 0 Maximum V _{OUT} Range 0 Set Point Accuracy Range 0 Resolution Range 0 LSB Step Size, FSR = 16.38	2.0V ≤ V _{OUT} ≤ 13.8V (Note 10)	•	-0.5	14.0 12 4	0.5	V % Bits mV
V _{OUTR1}	Range 1 Maximum V _{OUT} Range 1 Set Point Accuracy Range 1 Resolution Range 1 LSB Step Size, FSR = 8.19V	$1.0V \le V_{OUT} \le 6.6V$	•	-0.5	7.0 12 2	0.5	V % Bits mV
VLINEREG	Line Regulation	16V < V _{IN} < 60V	٠			±0.02	%/V
VLOADREG	Load Regulation	$\Delta V_{ITH} = 1.35V - 0.7V$ $\Delta V_{ITH} = 1.35V - 2.0V$	•		0.01 0.01	0.1 0.1	% %
9 _{m0,1}	Resolution				3		bits
	Error Amplifier g _{m(MAX)}	I _{TH} =1.35V			5.76		mmho
	Error Amplifier g _{m(MIN)}	I _{TH} =1.35V			1.00		mmho
	Error Amplifier g _m LSB Step Size	I _{TH} =1.35V			0.68		mmho
RITHRO,1	Resolution				5		bits
	Compensation Resistor RITHR(MAX)				62		kΩ
	Compensation Resistor RITHR(MIN)				0		kΩ
IISENSE	Input Current	VISENSE = 14V	٠		±1	±2	μA
VI(ILIMIT)	Resolution				3		bits
	VILIM(MAX)	Hi Range Lo Range	•	68 44	75 50	82 56	mV mV
	VILIM(MIN)	Hi Range Lo Range			37.5 25		mV mV
Gate Driver							
TG t _r t _f	TG Transition Time: Rise Time Fall Time	(Note 4) C _{LOAD} = 3300pF C _{LOAD} = 3300pF			30 30		ns ns
BG t _r t _f	BG Transition Time: Rise Time Fall Time	(Note 4) C _{LOAD} = 3300pF C _{LOAD} = 3300pF			20 20		ns
TG/BG t _{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) CLOAD = 3300pF			10		ns
BG/TG t _{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) CLOAD = 3300pF			30		ns
t _{ON(MIN)}	Minimum On-Time				90		ns



ELECTRICAL CHARACTERISTICS	The • denotes the specifications which apply over the specified operating
junction temperature range, otherwise specifications are a	at T _J = 25°C (Note 2). V _{IN} = 16V, EXTV _{CC} = 0V, V _{RUN0} = 3.3V, V _{RUN1} = 3.3V
f_{SYNC} = 350kHz (externally driven), and all programmable	parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OV/UV Output	t Voltage Supervisor						
N	Resolution				9		Bits
VRANGEO	Range 0 Maximum Threshold				14		V
VRANGE1	Range 1 Maximum Threshold		-		7		V
VOUSTPO	Range 0 Step Size, FSR = 16.352V	(Note 10)	1		32		mV
V _{OUSTP1}	Range 1 Step Size, FSR = 8.176V				16		mV
VTHACCO	Range 0 Threshold Accuracy	2V < V _{OUT} < 14V	٠			±2.5	%
V _{THACC1}	Range 1 Threshold Accuracy	1V < V _{OUT} < 7V	٠			±2.5	%
t _{PROPOV1}	OV Comparator to FAULT Low Time	V _{OD} = 10% of Threshold				35	μs
t _{PROPUV1}	UV Comparator to FAULT Low Time	V _{OD} = 10% of Threshold				100	μs
V _{IN} Voltage S	upervisor						
N	Resolution				9		Bits
VIN(RANGE)	Full-Scale Voltage	(Note 11)		4.5		61.32	V
VIN(STP)	Step Size				120		mV
VIN(THACCH)	Threshold Accuracy 12V < V _{IN} < 60V		•			±3	%
VIN(THACCL)	Threshold Accuracy 4.5V < V _{IN} < 15V		٠			±6	%
t _{PROP(VIN)}	Comparator Response Time (VIN_ON and VIN_OFF)	V _{OD} = 10% of Threshold				100	μs
Output Voltag	e Readback						
N	Resolution				16		Bits
	LSB Step Size				250		μV
V _{F/S}	Full-Scale Sense Voltage	(Note 10) V _{RUN} = 0V (Note 8)			16.384		V
VOUT_TUE	Total Unadjusted Error	T _J = 25°C, V _{OUT} > 1.0V (Note 8)	•		0.2	±0.5	%
Vos	Zero-Code Offset Voltage		•			±500	μV
t _{convert}	Conversion Time	(Note 6)			100 90)	ms
V _{IN} Voltage R	eadback	-					
N	Resolution	(Note 5)			10		Bits
V _{F/S}	Full-Scale Input Voltage	(Note 11)			66.56		V
VIN_TUE	Total Unadjusted Error	$T_{J} = 25^{\circ}C, V_{VIN} > 4.5V$				0.4	%
	Occurrence Time	(1)=1= (1)	•		400 00	2	%
LCONVERT	Conversion Time	(Note 6)			100-91	J	ms
Output Curren	It Readdack	(1)-1-5)	_		40		Dite
N	Resolution	(NOTE 5) OV < IVierner ⁺ - Vierner ⁻ I < 16mV			10		BITS
		$16\text{mV} \le V_{\text{ISENSE}}^{+} - V_{\text{ISENSE}}^{-} < 32\text{mV}$			30.52		μV
		$32mV \le V_{ISENSE}^+ - V_{ISENSE}^- < 64mV$			61		μV
	Full Casta Output Output	04INV ≤ VISENSE ⁺ - VISENSE ⁻ < 100mV			122		μν
IF/S	Full-Scale Output Current	(Note /) $R_{ISENSE} = 1 m\Omega$			±100	4.5	A
LOUT_TUE	Total Unadjusted Error	(Note 8) $10\text{mV} \le \text{V}_{\text{ISENSE}} \le 100\text{mV}$	•			±1.5	%
Vos	Zero-Code Offset Voltage					±32	μV
ICONVERT	Conversion Time	(Note 6)			100.90	,	ms



For more information www.linear.com/LTC3886



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ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_J = 25^{\circ}C$ (Note 2). $V_{IN} = 16V$, EXTV_{CC} = 0V, $V_{RUN0} = 3.3V$, $V_{RUN1} = 3.3V$ f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Input Current	Readback	1					
N	Resolution LSB Step Size, Full-Scale Range = 16mV LSB Step Size, Full-Scale Range = 32mV LSB Step Size, Full-Scale Range = 64mV	$\begin{array}{l} (Note 5) \\ 8x \ Gain, \ 0V \leq I_{1N}^+ - I_{1N}^- \leq 5mV \\ 4x \ Gain, \ 0V \leq I_{1N}^+ - I_{1N}^- \leq 20mV \\ 2x \ Gain, \ 0V \leq I_{1N}^+ - I_{1N}^- \leq 50mV \end{array}$			10 15.26 30.52 61		Bits μV μV μV
I _{IN_TUE}	Total Unadjusted Error (Note 8)	$\begin{array}{l} 8x \ Gain, \ 2.5mV \leq I_{1N}^+ - I_{1N}^- \leq 5mV \\ 4x \ Gain, \ 4mV \leq I_{1N}^+ - I_{1N}^- \leq 20mV \\ 2x \ Gain, \ 6mV \leq I_{1N}^+ - I_{1N}^- \leq 50mV \end{array}$	•••			±1.6 ±1.3 ±1.2	% % %
Vos	Zero-Code Offset Voltage					±50	μV
t _{convert}	Conversion Time	(Note 6)			100 9	0	ms
Supply Curren	nt Readback						
N	Resolution LSB Step Size, Full-Scale Range = 256mV	(Note 5)			10 244		Bits µV
CHIP_TUE	Total Unadjusted Error	$20mV \leq I_{IN}^+ - V_{IN} \leq 200mV$	٠			±2.5	%
t _{CONVERT}	Conversion Time	(Note 6)			1 00 9	0	ms
Temperature	Readback (TO, T1)						
T _{RES_T}	Resolution				0.25		°C
T0_TUE	External TSNS TUE (Note 8) MFR_PWM_MODE_LTC3886[5] = 0 MFR_PWM_MODE_LTC3886[5] = 1	ΔV _{TSNS} = 72mV (Note 17) V _{TSNS} ≤ 1.85mV (Note 17)	:			±3 ±7	0° 0°
TI_TUE	Internal TSNS TUE	V _{RUN} = 0.0V (Note 8)			±1		°C
t _{CONVERT_T}	Update Rate	(Note 6)			100-9	0	ms
INTV _{CC} Regul	ator						
VINTVCC_VIN	Internal V _{CC} Voltage No Load	6V < V _{IN} < 60V	٠	4.8	5	5.2	V
V _{LDO_VIN}	INTV _{CC} Load Regulation	I _{CC} = 0mA to 50mA			0.5	±2	%
VINTVCC_EXT	Internal V _{CC} Voltage No Load	5.5V < EXTV _{CC} < 14V	•	4.8	5	5.2	V
V _{LDO_EXT}	INTV _{CC} Load Regulation	I _{CC} = 0mA to 50mA, EXTV _{CC} = 12V			0.5	±2	%
V _{EXT_THRES}	EXTV _{CC} Switchover Voltage	EXTV _{CC} Ramping Positive	٠	4.5	4.7	4.95	V
V _{EXT_HYS}	EXTV _{CC} Hysteresis Voltage				80		mV
V _{DD33} Regula	tor						
V _{DD33}	Internal V _{DD33} Voltage	4.5V < VINTVCC		3.2	3.3	3.4	V
LIM	V _{DD33} Current Limit	$V_{DD33} = GND, V_{IN} = INTV_{CC} = 4.5V$			100		mA
V _{DD33_OV}	V _{DD33} Overvoltage Threshold				3.5		V
V _{DD33_UV}	V _{DD33} Undervoltage Threshold				3.1		V
V _{DD25} Regula	tor	1					
V _{DD25}	Internal V _{DD25} Voltage				2.5		V
LIM	V _{DD25} Current Limit	$V_{DD25} = GND, V_{IN} = INTV_{CC} = 4.5V$			80		mA
Oscillator and	Phase-Locked Loop	1					
f _{osc}	Oscillator Frequency Accuracy	100kHz < f _{SYNC} < 750kHz Measured Falling Edge-to-Falling Edge of SYNC with SWITCH_FREQUENCY = 100.0 and 750.0	•			±10	%
V _{TH(SYNC)}	SYNC Input Threshold	V _{CLKIN} Falling V _{CLKIN} Rising			1 1.5		V V
VOL(SYNC)	SYNC Low Output Voltage	I _{LOAD} = 3mA	•		0.2	0.4	V
ILEAK(SYNC	SYNC Leakage Current in Slave Mode	$0V \le V_{PIN} \le 3.6V$				±5	μA



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eSYNC-00 SYNC to Channel O Phase Relationship Based of TG0 MFR_PVML_CONFIG_LTC3880[20] = 0.2,3 MFR_PVML_CONFIG_LTC3880[20] = 1 0 Deg of 0 eSYNC-01 SYNC to Channel I Phase Relationship Based of TG1 MFR_PVML_CONFIG_LTC3880[20] = 3. 120 Deg of TG1 eSYNC-01 SYNC to Channel I Phase Relationship Based of TG1 MFR_PVML_CONFIG_LTC3880[20] = 3. 120 Deg of TG1 eSYNC-01 MFR_PVML_CONFIG_LTC3880[20] = 3. 180 Deg of TG1 Deg of TG1 Deg of TG1 Deg eSYNC-01 MFR_PVML_CONFIG_LTC3880[20] = 3. 180 Deg of TG1 Deg eSYNC-01 MFR_PVML_CONFIG_LTC3880[20] = 4. 10 Deg MFR_PVML_CONFIG_LTC3880[20] = 5 270 Deg EEPFONC Characteristics 11 27 270 Eretrition (Note 13) T_<<28°C 10 Vers During EEPROM Write Operation Time STCL_SOA, RUN, FAUT 14.40 V Mrs_PVML_CAUNC CAUNTIAL V 1.4 V V Ming Libration Time SCL_SOA, RUN, FAUT 1.4 V V Ming Libration Time	SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
on the Failing Edge of Sync and Rising Edge MRP_PVML_CONFIG_LTC3880[2:0] = 1 00 Deg eSYNC-01 SYNC to Channel 1 Phase Relationship Bage MRP_PVML_CONFIG_LTC3880[2:0] = 4.6 120 Deg eSYNC-01 SYNC to Channel 1 Phase Relationship Edge MRP_PVML_CONFIG_LTC3880[2:0] = 2.4 180 Deg of TG1 SYNC to Channel 1 Phase Relationship Edge MRP_PVML_CONFIG_LTC3880[2:0] = 2.4 270 Deg of TG1 SYNC to Channel 1 Phase Relationship Edge MRP_PVML_CONFIG_LTC3880[2:0] = 1 300 Deg EEPROM Characteristics MRP_PVML_CONFIG_LTC3880[2:0] = 1 300 Deg Eernor Maracteristics 0°C - T_ < 85°C During EEPROM Write	06SANC-00	SYNC to Channel 0 Phase Relationship Based	MFR_PWM_CONFIG_LTC3886[2:0] = 0,2,3			0		Deg
Dir Ho Imm PriviL_OUNG1_LISSB0[2:0] = 4, b 90 Deg eSYNC-01 SYNC to Channel 1 Phase Relationship Based of TG1 MRP_PVM_CONFG_LITG3880[2:0] = 3 120 Deg eSYNC-01 SYNC to Channel 1 Phase Relationship Based of TG1 MRP_PVM_CONFG_LITG3880[2:0] = 3 180 Deg MRP_PVM_CONFG_LITG3880[2:0] = 4.5 240 Deg MRP_PVM_CONFG_LITG3880[2:0] = 1 270 Deg EEPROM Characteristics 0°C < T_ < 85°C During EEPROM Write Operations 10.000 Cycles Eeterion (Note 13) 0°C < T_ < 85°C During EEPROM Write Operations 10 Years Mass_Write Note Nass Write Operation Time STORE USER ALL 0°C < T_ < 85°C		on the Falling Edge of Sync and Rising Edge	MFR_PWM_CONFIG_LTC3886[2:0] = 5			60		Deg
SYNC-01 SYNC to Channel 1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1 MER_PWM_CONFIG_LTC3886[20] = 3 MER_PWM_CONFIG_LTC3886[20] = 6 120 Deg Deg EEPROM Characteristics MER_PWM_CONFIG_LTC3886[20] = 6 240 Deg Eendurance Endurance (Note 13) 0°C < T ₁ < 85°C During EEPROM Write Operations 10.000 Cycles Type 10.100 0°C < T ₁ < 85°C During EEPROM Write Operations 10.000 Cycles Eetrotion (Note 13) 0°C < T ₁ < 85°C During EEPROM Write Operations 10.000 Cycles Tigital Input SCL, SOA, RUN, FAULT <i>n</i> 0°C < T ₁ < 85°C During EEPROM Write Operations		01100	MFR_PWM_CONFIG_LTC3886[2:0] = 1 MFR_PWM_CONFIG_LTC3886[2:0] = 4,6			120		Deg
on the Failing Edge of Sync and Rising Edge of TG1 MRP, PVM, CONFIG, L1C3886[2:0] = 0 MRP, PVM, CONFIG, L1C3886[2:0] = 1 MRP, PVM, CONFIG, L1C3886[2:0] = 6 270 Deg EEPROM Characteristics 0°C < T, < 85°C During EEPROM Write	0SYNC-01	SYNC to Channel 1 Phase Relationship Based	MFR_PWM_CONFIG_LTC3886[2:0] = 3			120		Deg
of 161 WH-PWM, CONFIG_LIC3886[2:0] = 6 240 Upg MFR_PWM, CONFIG_LIC3886[2:0] = 6 300 Deg EEPROM Characteristics 0 0 Deg Endurance (Note 13) 0 0 Cycles Operations 0 0 0 0 Ratention (Note 13) 1_x < 125°C		on the Falling Edge of Sync and Rising Edge	MFR_PWM_CONFIG_LTC3886[2:0] = 0			180		Deg
Imit PWMCONING_LICOSSE(2:0) = 6 2.00 Deg EEPROM Characteristics 0°C < T_J < 85°C During EEPROM Write		01161	MFR_PWM_CONFIG_LTC3886[2:0] = 2,4,5			240		Deg
EEPROM Characteristics Image: Constraint of the second seco			MFR_PWM_CONFIG_LTC3886[2:0] = 6			300		Deg
Endurance (Note 13) 0°C < T ₁ < 85° C During EEPROM Write ● 10,000 Cycles Retention (Note 13) T _J < 125°C	EEPROM Cha	racteristics						
Retention(Note 13)T_J < 125°CIIIIVearsMass_WriteOperation TimeSTORE_USER_ALL, 0°C < T_J < 85°C	Endurance	(Note 13)	0°C < T _J < 85°C During EEPROM Write Operations	•	10,000			Cycles
Mass_WriteMass WriteMass Write Operation TimeSTORE_USER_ALL_0°C < $\tau_2 < 88°C$ During EEPROM Write Operations4404100msDigital Inputs SCL, SDA, RUN, FAULT<	Retention	(Note 13)	T _J < 125°C	٠	10			Years
Digital Inputs SCL, SDA, RUNA, FAULTA ● 2.0 VV V _H Input Ligh Threshold Voltage SCL, SDA, RUN, FAULT ● 1.4 VV V _{HYST} Input Low Threshold Voltage SCL, SDA, RUN, FAULT ● 1.4 VV V _{HYST} Input Capacitance SCL, SDA 0.08 VV Digital Input VP 1.0 pF Digital Input Capacitance NP 10 pF Digital Input Capacitance NP 10 pA Open-Drain Output SCL, SDA, FAUTTA, ALERT, RUNA, SHARE, CLK, PGODON VQL Output Low Voltage 15.1 8.1 V _{IL} Input High Threshold Voltage IsiNK = 3mA ● 0.4 V Digital Inputs SCL, SDA, EAUTR, RUNA SLASSE ● 1.5 1.8 V V _{IL} Input Low Threshold Voltage ● 0.6 1.0 V Leakage Current SDA, SCL, ALERT, RUN VIL Input Leakage Current 0V ≤ V _{PIN} ≤ 5.5V ● ±5 µA Leakage Current FAUTn / PGODD Input Leakage Current 0V ≤ V _{PIN} ≤ 3.6V ● ±2 µA	Mass_Write	Mass Write Operation Time	STORE_USER_ALL, $0^{\circ}C < T_J \le 85^{\circ}C$ During EEPROM Write Operations	•		440	4100	ms
V _H Input High Threshold Voltage SCL, SDA, RUN, FAUET ● 2.0 V V _L Input Low Threshold Voltage SCL, SDA, RUN, FAUET ● 1.4 V V _{PYST} Input Capacitance 0.08 V Digital Input WP 10 µA JerumP Input Pul-Up Current WP 10 µA Open-Drain Output SCL, SDA, FAUTI'n, ALERT, RUNN, SHARE_CLK, PGOOD n VOL 0.4 V Ogen-Drain Output SCL, SDA, FAUTI'n, ALERT, RUNN, SHARE_CLK, PGOOD n 0.6 1.0 µA VoL Output Low Voltage ● 1.5 1.8 V ViL Input Leakage Current 0V ≤ V _{PM} ≤ 5.5V ● ±5 µA Leakage Current TAUT, PGOOD n Input Leakage Current 0V ≤ V _{PM} ≤ 3.6V ±2 µA Digital Filtering of FAUET 0V ≤ V _{PM} ≤ 3.6V ● ±2 µA Digital Filtering of FAUET 0V ≤ V _{PM} ≤ 3.6V ±2 µA Digital Filtering of RUEN 10 µB µB µB 10 µB	Digital Inputs	SCL, SDA, RUN <i>n</i> , FAULT <i>n</i>						
VIL VIL VIYST Input Low Threshold Voltage SCL, SDA, RUN, FAULT ● 1.4 V VIYST Input Low Threshold Voltage SCL, SDA 0.08 V CPN Input Capacitance 0 10 PF Digital Input WP 10 µA Vol. Output SCL, SDA, FAUTA, ALERT, RUNA, SHARE_CLK, PGODD 0.4 V Vol. Output SCL, SDA, FAUTA, ALERT, RUNA, SHARE_CLK, PGODD 0.4 V Vol. Output SCL, SDA, FAUTA, ALERT, RUNA, SHARE_CLK, PGODD 0.4 V Vil. Input High Threshold Voltage 1.5 1.8 V Vil. Input Low Threshold Voltage 0.5 1.0 V Leakage Current SDA, SCL, ALERT, RUN 0.5 1.0 V Leakage Current SUD, SCL, ALERT, RUN 0.5 1.0 V Leakage Current SUD, SCL, ALERT, RUN 0.5 1.0 V Leakage Current SUD, SCL, ALERT, RUN 1.0 ±2 µA Digital Filtering of FAUTA 0V ≤ V _{PIN} ≤ 5.5V ±2 µA Digital Filtering of FO	VIH	Input High Threshold Voltage	SCL, SDA, RUN, FAULT	٠			2.0	۷
V _{PYST} Input Hysteresis SCL, SDA 0.08 V CPM Input Capacitance 10 pF Digital Input WP 10 µA Deven Oratio Output SCL, SDA, FAULT, ALERT, RUNN, SHARE_CLK, PGODD 10 µA Open-Oratio Output SCL, SDA, FAULT, ALERT, RUNN, SHARE_CLK, PGODD 0.4 V Digital InputS SHARE_CLK, WP 0.15 1.8 V Vill Input Low Voltage 0.6 1.0 V Leakage Current SDA, SCL, ALERT, RUN 0V ≤ V _{PIN} ≤ 5.5V 0 ±5 µA Leakage Current FAULT, PGODD 10 V V_PIN ≤ 3.6V ±2 µA Leakage Current FAULT, PGOOD n 10 10 ±2 µA Digital Filtering of FAULT, PGOOD n 10 ±2 µA Input Digital Filtering FAULT n 3 µS Digital Filtering of FAULT n 3 µS Traubut Input Digital Filtering RUN n 10 µS Digital Filtering of GOOD n 10 400 kHz Leawage Current Tout Digital Fi	VIL	Input Low Threshold Voltage	SCL, SDA, RUN, FAULT	٠	1.4			V
Öpin Input Capacitance 10 pF Digital Input WP Input Pull-Up Current WP 10 µA Open-Drain Outputs SCL, SDA, FAULTIN, ALERT, RUNN, SHARE_CLK, PGODON V/U 0utput Low Voltage Isinx = 3mA 0 0.4 V/V Ogletal Inputs SHARE_CLK, WP 0.6 1.5 1.8 V Vil_ Input Low Threshold Voltage 0.6 1.0 V Leakage Current SDA, SCL, ALERT, RUN 0.6 1.0 V Leakage Current SDA, SCL, ALERT, RUN . <t< td=""><td>V_{HYST}</td><td>Input Hysteresis</td><td>SCL, SDA</td><td></td><td></td><td>0.08</td><td></td><td>V</td></t<>	V _{HYST}	Input Hysteresis	SCL, SDA			0.08		V
Digital Input WP Input Pull-Up Current WP 10 µA Open-Drain Outputs SCL, SDA, FAUUTA, ALERT, RUNA, SHARE_CLK, PGOOD <i>n</i> V0L Output Low Voltage Isink = 3mA 0.4 V V0L Output Low Voltage Isink = 3mA 0.4 V Vill Input High Threshold Voltage 0.4 V Vill Input Low Threshold Voltage 0.5 1.5 1.8 V Vill Input Leakage Current 0V ≤ V _{PIN} ≤ 5.5V ● ±5 µA Leakage Current OV ≤ V _{PIN} ≤ 5.5V ● ±2 µA Leakage Current OV ≤ V _{PIN} ≤ 5.5V ● ±2 µA Digital Filtering of FAUUT // FAUUT	CPIN	Input Capacitance					10	pF
IppumP Input Pull-Up Current WP 10 µA Open-Orain Outputs SCL, SDA, FAUIERT, RUNn, SHARE_CLK, PGODDn	Digital Input	WP						
Open-Drain Outputs SCL, SDA, FAULT <i>n</i> , ALERT, RUN <i>n</i> , SHARE_CLK, PG00D <i>n</i> Vol. Output Low Voltage Isink = 3mA Isink = 3mA O.4 V Digital Inputs SHARE_CLK, WP Input High Threshold Voltage I.5 1.8 V Vil. Input Low Threshold Voltage Input Low Threshold Voltage Input Low Threshold Voltage Input Leakage Current SDA, SCL, ÄLERT, RUN Ioc. Input Leakage Current OV <	PUWP	Input Pull-Up Current	WP			10		μA
V _{0L} Output Low Voltage I _{SINK} = 3mA ● 0.4 V Digital Inputs SHARE_CLK, WP	Open-Drain O	utputs SCL, SDA, FAULT <i>n</i> , ALERT, RUN <i>n</i> , SHA	RE_CLK, PGOOD <i>n</i>					
Digital Inputs SHARE_CLK, WP V_{IH} Input High Threshold Voltage•1.51.8V V_{IL} Input Low Threshold Voltage•0.61.0VLeakage Current SDA, SCL, ALERT, RUN I_{0L} Input Leakage Current $0V \le V_{PIN} \le 5.5V$ • ± 5 μA Leakage Current FAULT <i>n</i> , PGODD <i>n</i> I_{GL} Input Leakage Current $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT <i>n</i> TrauxitInput Leakage Current $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT <i>n</i> TrauxitInput Digital Filtering FAULT <i>n</i> TrauxitInput Digital Filtering FAULT <i>n</i> TrauxitInput Leakage Current $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT <i>n</i> TrauxitInput Digital Filtering FAULT <i>n</i> Transition of FAULT <i>n</i>	V _{OL}	Output Low Voltage	I _{SINK} = 3mA	٠			0.4	٧
V _{IL} Input High Threshold Voltage 1.5 1.8 V V _{IL} Input Low Threshold Voltage ● 0.6 1.0 V Leakage Current SDA, SCL, ÄLERT, RUN U <th< td=""><td>Digital Inputs</td><td>SHARE_CLK, WP</td><td></td><td></td><td></td><td></td><td></td><td></td></th<>	Digital Inputs	SHARE_CLK, WP						
VILInput Low Threshold VoltageInput Low Threshold VoltageInput Low Threshold VoltageInput Leakage Current $0V \le V_{PIN} \le 5.5V$ Input Leakage Current $0V \le V_{PIN} \le 5.5V$ Input Leakage Current $0V \le V_{PIN} \le 3.6V$ ± 2 μA Leakage Current FAULT n $0V \le V_{PIN} \le 3.6V$ ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ ± 2 μA Digital Filtering of FAULT n 3 μs Digital Filtering of ODO n 600 μs Digital Filtering of ODO n 600 μs t_{PGOOD} $0Utput Digital Filtering PGOD n600\mu sDigital Filtering of RUN n100\mu st_{HUN}Input Digital Filtering RUN n10\mu sPMBus Interface Timing Characteristics1.3\mu st_{SCL}Serial Bus Operating Frequency\bullet1.3\mu st_{HU}(STA)Hold Time After Start Condition. After This\bullet0.6\mu st_{SU(STA)}Repeated Start Condition Setup Time\bullet0.6\mu st_{SU(STA)}Stop Condition Setup Time\bullet0.6\mu st_{HU}(DAT)Data Hold Time\bullet0.30.9\mu s$	VIH	Input High Threshold Voltage		٠		1.5	1.8	٧
Leakage Current SDA, SCL, ALERT, RUN I_{OL} Input Leakage Current $0V \le V_{PIN} \le 5.5V$ • ± 5 μA Leakage Current $FAULT n, PGODD n$ I_{GL} Input Leakage Current $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of GODO n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of PGODO n $0Utput Digital Filtering PG00D n$ $000 pus$ $000 pus$ Digital Filtering of RUN n 10 μs PMBus Interface Timing Characteristics 0 10 400 kHz taueBus Free Time Between Stop and Start 0.6 μs taueBus Free Time Between Stop and Start 0.6 μs taueStop Condition After This 0.6 μs tsu(STA)Repeated Start Condition After This 0.66 μs tsu(STD)Stop Condition Setup Time 0.66 μs tsu(DAT)Data Hold Time 0.3 0.9 μs	VIL	Input Low Threshold Voltage		٠	0.6	1.0		۷
IonInput Leakage Current $0V \le V_{PIN} \le 5.5V$ • ± 5 μA Leakage CurrentFAULT n, PGOOD nIgLInput Leakage Current $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n $0V \le V_{PIN} \le 3.6V$ • ± 2 μA Digital Filtering of FAULT n 3 μs Digital Filtering of PGOOD n 600 μs t_{FGOOD} $0utput Digital Filtering PGODD n$ 600 μs Digital Filtering of RUN n 100 μs trunInput Digital Filtering RUN n 100 μs PMBus Interface Timing Characteristics 100 400 kHz tauerBus Sree Time Between Stop and Start 0.6 μs tauerBus Free Time Between Stop and Start 0.6 μs tauerStop Condition Setup Time 0.6 μs tsu(STA)Repeated Start Condition Step Time 0.6 μs tsu(STD)Stop Condition Setup Time 0.6 μs tsu(STD)Data Hold Time 0.3 0.9 μs	Leakage Curr	ent SDA, SCL, ALERT, RUN						
Leakage Current FAULT n, PG00D n IgL Input Leakage Current $0V \le V_{PIN} \le 3.6V$ ± 2 μA Digital Filtering of FAULT n 1 3 μs trAULT Input Digital Filtering FAULT n 3 μs Digital Filtering of PG00D n 60 μs trggood Output Digital Filtering PG00D n 60 μs Digital Filtering of RUN n 10 μs trggood Input Digital Filtering RUN n 10 μs PMBus Interface Timing Characteristics 1 1 μs fscL Serial Bus Operating Frequency 1 1 μs taur Bus Free Time Between Stop and Start 1 1.3 μs tho(STA) Hold Time After Start Condition. After This 0 0.6 μs tsu(STA) Repeated Start Condition Setup Time 0.6 0 μs tsu(STA) Deat Hold Time 0 0.6 μs thu(DAT) Data Hold Time 0 0 0 <t< td=""><td>I_{OL}</td><td>Input Leakage Current</td><td>$0V \le V_{PIN} \le 5.5V$</td><td>٠</td><td></td><td></td><td>±5</td><td>μA</td></t<>	I _{OL}	Input Leakage Current	$0V \le V_{PIN} \le 5.5V$	٠			±5	μA
IgL Input Leakage Current $0V \le V_{PIN} \le 3.6V$ ± 2 μA Digital Filtering of FAULT n 3 μs Digital Filtering of PGODD n 3 μs Tegodo Output Digital Filtering PG00D n 60 μs Digital Filtering of RUN n 10 μs Tquin Input Digital Filtering RUN n 10 μs PMBus Interface Serial Bus Operating Frequency \bullet 10 400 kHz tsurf Bus Free Time Between Stop and Start \bullet 1.3 μs $t_{HO}(STA)$ \bullet 0.6 μs tsu(STA) Repeated Start Condition After This \bullet 0.6 10000 μs tsu(STA) Repeated Start Condition Setup Time \bullet 0.6 μs $t_{SO(DT)$ μs $t_{O(DAT)}$ Data Hold Time \bullet 0.6 μs tho(DAT) Data Hold Time \bullet 0.6 μs 0.3 0.9 μs	Leakage Curr	rent FAULT <i>n</i> , PGOOD <i>n</i>						
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trault Input Digital Filtering FAULT n 3 µs Digital Filtering of PGODD n 60 µs Digital Filtering of RUNn 60 µs traum Input Digital Filtering RUNn 10 µs PMBus Interface Timing Characteristics 10 400 kHz tgur Bus Free Time Between Stop and Start 1.3 µs tHD(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated 0.6 100 µs tsu(STA) Repeated Start Condition Setup Time 0.6 µs tsu(STA) Data Hold Time Receiving Data Time 0.6 µs thD(DAT) Data Hold Time Receiving Data Time 0.6 µs thD(DAT) Data Hold Time Receiving Data Time 0.3 0.9 µs	Digital Filteri	ing of FAULT <i>n</i>						
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tpsgood Output Digital Filtering PG00Dn 60 µs Digital Filtering of RUNn 10 µs traun Input Digital Filtering RUNn 10 µs PMBus Interface Timing Characteristics 10 400 kHz fscL Serial Bus Operating Frequency 10 400 kHz taur Bus Free Time Between Stop and Start 1.3 µs tBup(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated 0.6 µs tsu(STA) Repeated Start Condition Setup Time 0.6 µs tsu(STD) Stop Condition Setup Time 0.6 µs tup(DAT) Data Hold Time Receiving Data Transmitting Data 0 µs	Digital Filteri	ing of PGOOD <i>n</i>						
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Input Digital Filtering RUNn 10 µs PMBus Interface Timing Characteristics 10 400 kHz fscL Serial Bus Operating Frequency 10 400 kHz tBuF Bus Free Time Between Stop and Start 1.3 µs tHD(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated 0.6 µs tsu(STA) Repeated Start Condition Setup Time 0.6 µs tsu(STO) Stop Condition Setup Time 0.6 µs thD(DAT) Data Hold Time Receiving Data Transmitting Data µs 0 µs	Digital Filteri	ing of RUN <i>n</i>						
PMBus Interface Timing Characteristics f _{SCL} Serial Bus Operating Frequency Image: 10 400 kHz t _{BUF} Bus Free Time Between Stop and Start Image: 1.3 Jms tHD(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated Image: 0.6 Jms t _{SU(STA)} Repeated Start Condition Setup Time Image: 0.6 Jms t _{SU(STO)} Stop Condition Setup Time Image: 0.6 Jms t _{SU(STO)} Data Hold Time Receiving Data Transmitting Data Image: 0.3 Jms	t _{RUN}	Input Digital Filtering RUNn				10		μs
fsclSerial Bus Operating FrequencyI10400kHztaurBus Free Time Between Stop and StartI1.3µstHD(STA)Hold Time After Start Condition. After This Period, the First Clock Is GeneratedI0.6µstsu(STA)Repeated Start Condition Setup TimeI0.610000µstsu(STO)Stop Condition Setup TimeI0.6µsthD(DAT)Data Hold Time Receiving Data Transmitting DataI0µsImage: State St	PMBus Interf	ace Timing Characteristics						
taur Bus Free Time Between Stop and Start I.3 µs tHD(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated 0.6 µs tsu(STA) Repeated Start Condition Setup Time Image: 0.6 10000 µs tsu(STA) Stop Condition Setup Time Image: 0.6 10000 µs tsu(STA) Data Hold Time Receiving Data Transmitting Data Image: 0.3 0.9 µs	f _{SCL}	Serial Bus Operating Frequency		٠	10		400	kHz
thD(STA) Hold Time After Start Condition. After This Period, the First Clock Is Generated • 0.6 µs tsu(STA) Repeated Start Condition Setup Time • 0.6 10000 µs tsu(STA) Stop Condition Setup Time • 0.6 10000 µs tsu(STO) Stop Condition Setup Time • 0.6 µs thD(DAT) Data Hold Time Receiving Data Transmitting Data • 0 µs • 0.3 0.9 µs	t _{BUF}	Bus Free Time Between Stop and Start		٠	1.3			μs
tsu(STA) Repeated Start Condition Setup Time 0.6 10000 µs tsu(STO) Stop Condition Setup Time 0 0.6 µs tHD(DAT) Data Hold Time Receiving Data Transmitting Data 0 µs	t _{HD(STA)}	Hold Time After Start Condition. After This Period, the First Clock Is Generated		•	0.6			μs
t_{SU(STO)}Stop Condition Setup Time●0.6µst_HD(DAT)Data Hold Time Receiving Data●0µsTransmitting Data●0.30.9µs	t _{su(sta)}	Repeated Start Condition Setup Time		٠	0.6		10000	μs
t _{HD(DAT)} Data Hold Time Receiving Data Transmitting Data 0 μs	t _{SU(STO)}	Stop Condition Setup Time		٠	0.6			μs
Transmitting Data 0.3 0.9 µs	t _{HD(DAT)}	Data Hold Time Receiving Data		•	0			μs
		Transmitting Data		٠	0.3		0.9	μs



