TPS22958x 5.5-V, 4-A / 6-A, 14-mΩ Load Switch with Adjustable Rise Time

1 Features

- Integrated N-Channel Load Switch
- Input Voltage Range: 0.6 V to 5.5 V
- VBIAS Voltage Range: 2.5 V to 5.5 V
- R_{ON} Resistance
  - R_{ON} = 14 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 13 mΩ at V_{IN} = 3.3 V (V_{BIAS} = 5 V)
  - R_{ON} = 13 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 4 A Maximum Continuous Switch Current (DGK Package)
- 6 A Maximum Continuous Switch Current (DGN Package)
- Low Quiescent Current
  - 55 µA at V_{BIAS} = 5 V
- Low Control Input Threshold Enables Use of 1.2 V/1.8 V/2.5 V/3.3 V Logic
- Adjustable Rise Time(1)
- Quick Output Discharge (QOD)(2)
- DGK 8-Pin Package:
  - 3.0 mm x 4.9 mm x 1.1 mm and 0.65 mm pitch
- DGN 8-Pin Package with Thermal Pad:
  - 3.0 mm x 4.9 mm x 1.1 mm and 0.65 mm pitch
- ESD Performance Tested per JEDEC STD.
  - 2-kV HBM and 1-kV CDM
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- GPIO Enable – Active High

(1) See *Adjustable Rise Time* section for CT value vs. rise time

(2) Not featured in the TPS22958N device.

2 Applications

- EPOS
- Factory Automation/Control
- Building Automation
- Printers
- Wave Soldering Manufacturing

3 Description

The TPS22958x is a small, single channel load switch with an adjustable rise time. The device contains an N-Channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 4 A (DGK package) or 6 A (DGN package). The switch is controlled by an on/off input, which is capable of interfacing directly with low voltage control signals.

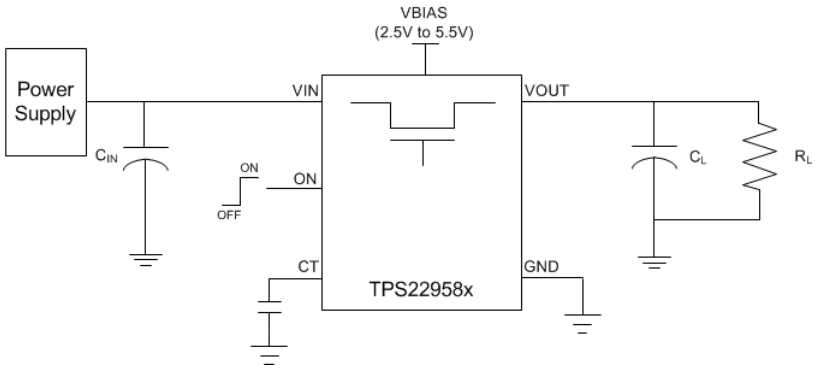
The rise time of the device can be externally controlled in order to avoid inrush current. Attaching a capacitor to the CT pin will change the rise time: increasing the value of the capacitor will increase the rise time. The TPS22958x is available in two space-saving packages (DGK and DGN) with or without a thermal pad for high power dissipation. The device is characterized for operation over the free-air temperature range of -40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TPS22958x	DGK (8)	3.00 mm × 4.90 mm
	DGN (8)	3.00 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

Changes from Original (January 2014) to Revision A	Page
• Initial release of full version.	1

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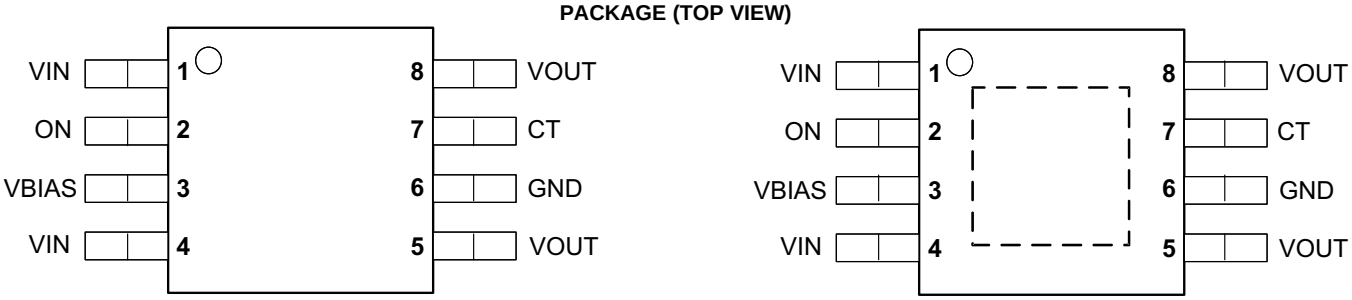
5 Device Comparison Table

DEVICE	R_{ON} AT VIN = VBIAS = 5V	RISE TIME	QUICK OUTPUT DISCHARGE	MAX OUTPUT CURRENT	ENABLE
TPS22958DGK	14 mΩ	Adjustable	Yes	4 A	Active High
TPS22958DGN		Adjustable	Yes	6 A	
TPS22958NDGK		Adjustable	No	4 A	
TPS22958NDGN		Adjustable	No	6 A	

6 Pin Configuration and Functions

PACKAGE (TOP VIEW)



DGK Package **DGN Package**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 4	VIN	I	Switch input. Bypass this input with a ceramic capacitor to GND. These pins should be tied together as shown in Layout Information.
2	ON	I	Active-high switch control input. Do not leave floating.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 to 5.5 V. See *VIN and VBIAS Voltage Range* .
5, 8	VOUT	O	Switch output
6	GND	—	Ground
7	CT	O	Switch slew rate control. Can be left floating.
—	Thermal Pad(1)	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Guidelines* for layout guidelines.

(1) Only available for the DGN package

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current, T_A = 65°C (DGK Package)		4	A
	Maximum continuous switch current, T_A = 75°C (DGN Package)		6	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle (DGK Package)		6	A
	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle (DGN Package)		8	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.6	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{BIAS} = 2.5 to 5.5 V	1.2	5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{BIAS} = 2.5 to 5.5 V	0	0.5	V
T_A	Operating free-air temperature (1)		–40	105	°C
C_{IN}	Input capacitor		1(2)		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.
(2) Refer to the *Application Information* section.

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7.4 Thermal Information

THERMAL METRIC(1) (2)		TPS22958x		UNIT
		DGK (8 PINS)	DGN (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	67.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.3	66.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	107.0	46.8	
ψ_{JT}	Junction-to-top characterization parameter	15.2	5.0	
ψ_{JB}	Junction-to-board characterization parameter	105.4	46.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	14.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.

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7.5 Electrical Characteristics (V_{BIAS} = 5 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 105°C and V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 5 V		-40°C to 85°C		54	60	µA
				-40°C to 105°C			60	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 5 V		-40°C to 85°C		0.5	1	µA
				-40°C to 105°C			1	
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 5 V	V_{IN} = 5 V	-40°C to 85°C		0.5	8	µA
				-40°C to 105°C			10	
			V_{IN} = 3.3 V	-40°C to 85°C		0.1	3	
				-40°C to 105°C			4	
			V_{IN} = 1.8 V	-40°C to 85°C		0.07	2	
				-40°C to 105°C			3	
			V_{IN}= 1.2 V	-40°C to 85°C		0.05	1	
				-40°C to 105°C			2	
			V_{IN} = 0.6 V	-40°C to 85°C		0.04	1	
				-40°C to 105°C			2	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V, V_{BIAS} = 5 V		-40°C to 105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		14	18	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			24	
			V_{IN} = 3.3 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 2.5 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.8 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.5 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.2 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 0.6 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
R_{PD}	Output pulldown resistance	V_{IN} = V_{BIAS} = 5 V, V_{ON} = 0 V, I_{OUT} = 10 mA		-40°C to 105°C		135	160	Ω

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7.6 Electrical Characteristics (V_{BIAS} = 3.3 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 105°C and V_{BIAS} = 3.3 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 3.3 V		-40°C to 85°C		23	27	µA
				-40°C to 105°C			27	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 3.3 V		-40°C to 85°C		0.3	0.7	µA
				-40°C to 105°C			0.7	
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	-40°C to 85°C		0.1	3	µA
				-40°C to 105°C			4	
			V_{IN} = 1.8 V	-40°C to 85°C		0.07	2	
				-40°C to 105°C			3	
			V_{IN}= 1.2 V	-40°C to 85°C		0.05	1	
				-40°C to 105°C			2	
			V_{IN} = 0.6 V	-40°C to 85°C		0.04	1	
				-40°C to 105°C			2	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V, V_{BIAS} = 3.3 V		-40°C to 105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	25°C		14	18	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			24	
			V_{IN} = 2.5 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.8 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.5 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 1.2 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
			V_{IN} = 0.6 V	25°C		13	17	mΩ
				-40°C to 85°C			20	
				-40°C to 105°C			23	
R_{PD}	Output pulldown resistance	V_{IN} = V_{BIAS} = 3.3 V, V_{ON} = 0 V, I_{OUT} = 10 mA		-40°C to 105°C		135	160	Ω

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7.7 Electrical Characteristics (V_{BIAS} = 2.5 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ T_A ≤ 105 °C and V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		-40°C to 85°C		14	17	µA
				-40°C to 105°C			17	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 2.5 V		-40°C to 85°C		0.2	0.5	µA
				-40°C to 105°C			0.5	
$I_{SD, VIN}$	V_{IN} shutdown current (per channel)	V_{ON} = 0 V, V_{OUT} = 0 V, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	-40°C to 85°C		0.1	3	µA
				-40°C to 105°C			4	
			V_{IN} = 1.8 V	-40°C to 85°C		0.07	2	
				-40°C to 105°C			3	
			V_{IN} = 1.2 V	-40°C to 85°C		0.05	1	
				-40°C to 105°C			2	
			V_{IN} = 0.6 V	-40°C to 85°C		0.04	1	
				-40°C to 105°C			2	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V, V_{BIAS} = 2.5 V		-40°C to 105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		15	19	mΩ
				-40°C to 85°C			23	
				-40°C to 105°C			26	
			V_{IN} = 1.8 V	25°C		14	18	mΩ
				-40°C to 85°C			22	
				-40°C to 105°C			25	
			V_{IN} = 1.5 V	25°C		14	18	mΩ
				-40°C to 85°C			22	
				-40°C to 105°C			25	
			V_{IN} = 1.2 V	25°C		14	18	mΩ
				-40°C to 85°C			22	
				-40°C to 105°C			25	
			V_{IN} = 0.6 V	25°C		13	18	mΩ
				-40°C to 85°C			22	
				-40°C to 105°C			25	
R_{PD}	Output pulldown resistance	V_{IN} = V_{BIAS} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 10 mA		-40°C to 105°C		135	160	Ω

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7.8 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25 °C						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		646		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		5		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		769		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		280		
V_{IN} = 0.6 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25 ºC						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		303		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		91		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		126		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		7		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		243		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5V, T_A = 25 ºC						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		983		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		7		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		987		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		518		
V_{IN} = 0.6 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25 ºC						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		611		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		77		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		305		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		7		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		468		

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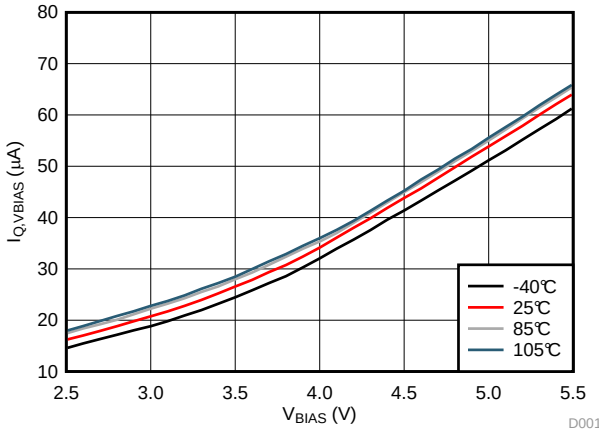
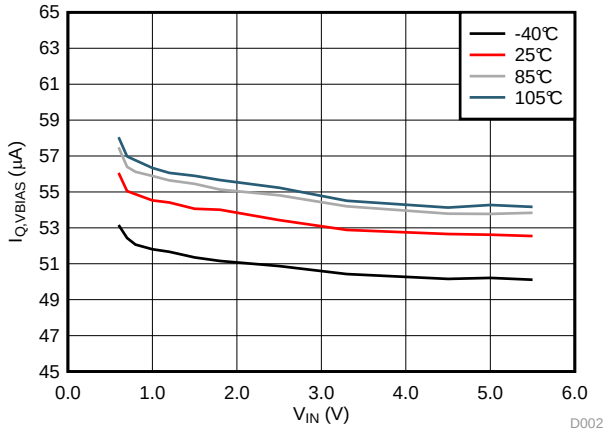
7.9 Typical DC Characteristics



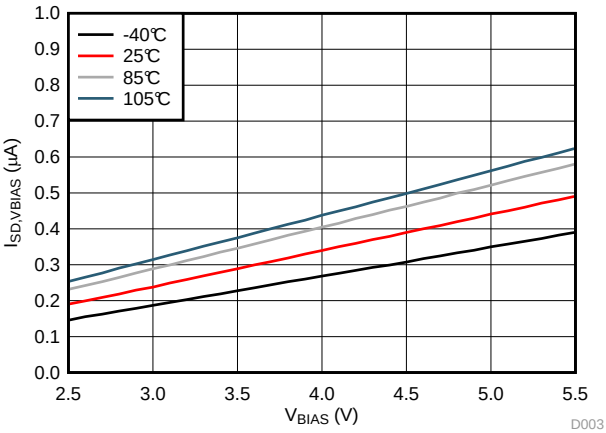
$V_{IN} = V_{BIAS}$ V_{OUT} = Open V_{ON} = 5 V

Figure 1. Quiescent Current vs V_{BIAS}



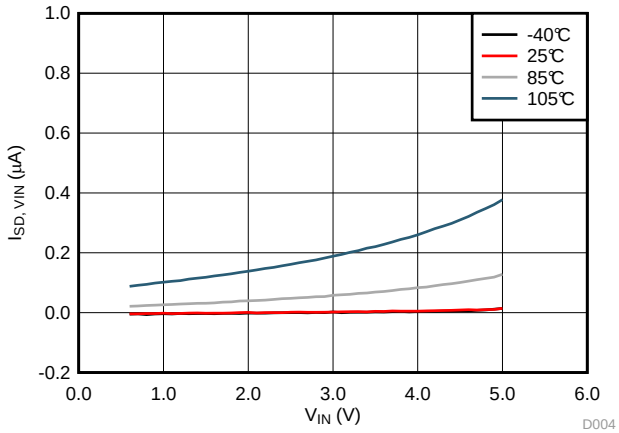
V_{BIAS} = 5 V V_{ON} = 5 V V_{OUT} = Open

Figure 2. Quiescent Current vs V_{IN}



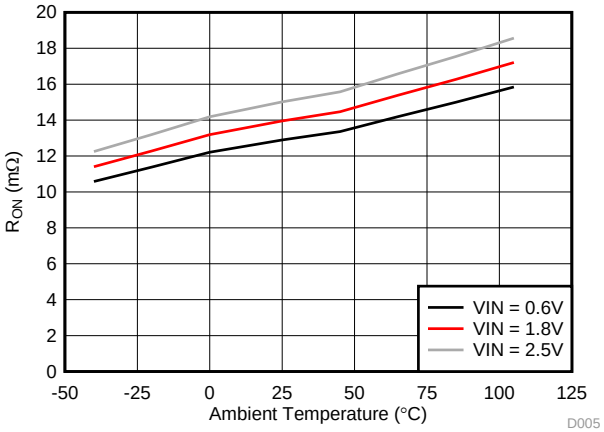
$V_{IN} = V_{BIAS}$ V_{OUT} = 0 V V_{ON} = 0 V

Figure 3. Shutdown Current vs V_{BIAS}



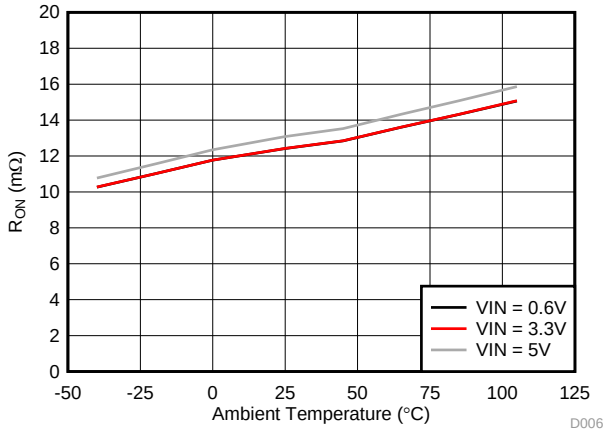
V_{BIAS} = 5 V V_{OUT} = 0 V V_{ON} = 0 V

Figure 4. V_{IN} Shutdown Current vs V_{IN}



V_{BIAS} = 2.5 V V_{ON} = 5 V I_{OUT} = –200 mA

Figure 5. R_{ON} vs Temperature



V_{BIAS} = 5 V V_{ON} = 5 V I_{OUT} = –200 mA

Figure 6. R_{ON} vs Temperature

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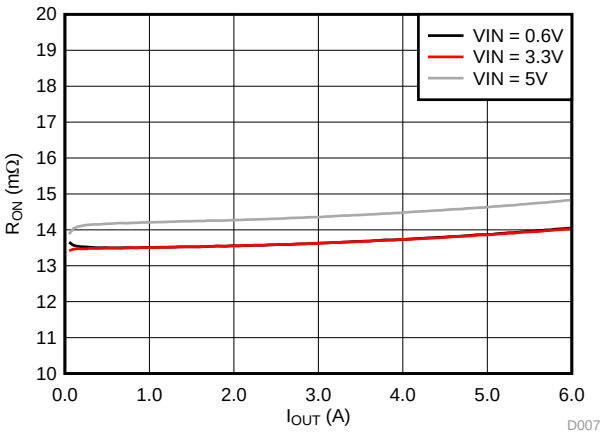
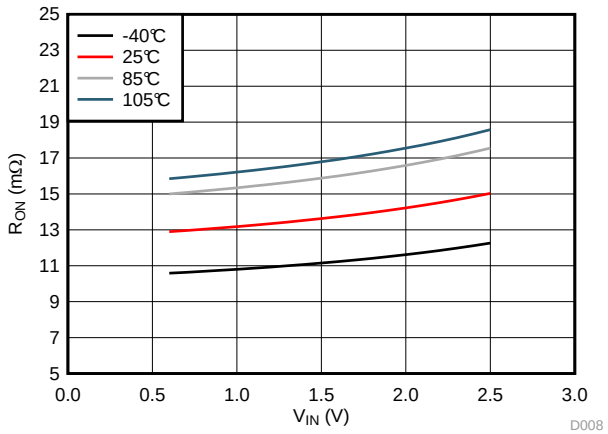
Typical DC Characteristics (continued)



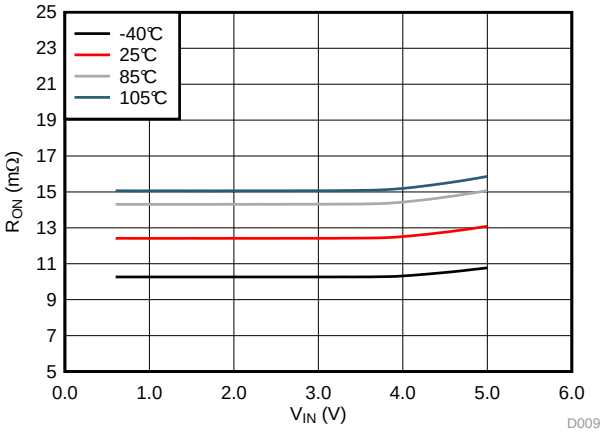
V_{BIAS} = 5 V V_{ON} = 5 V T_A = 25°C

Figure 7. R_{ON} vs I_{OUT} (DGN Package)



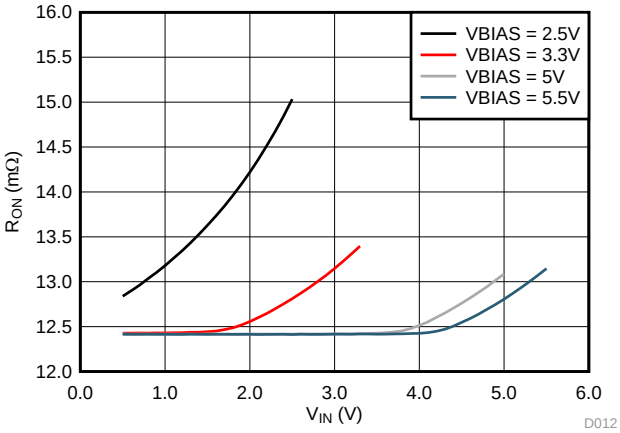
V_{BIAS} = 2.5 V V_{ON} = 5V I_{OUT} = –200 mA

Figure 8. R_{ON} vs V_{IN}



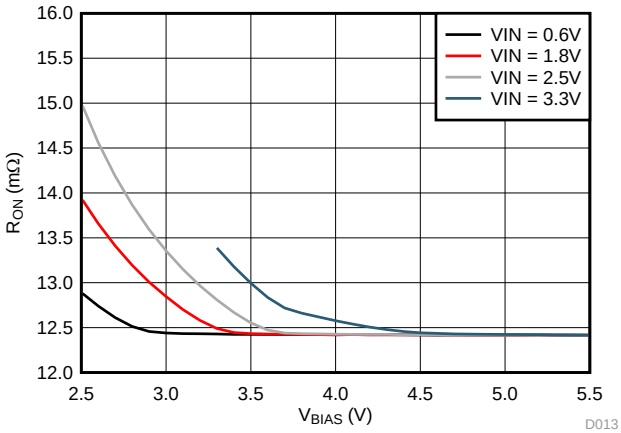
V_{BIAS} = 5 V V_{ON} = 5 V I_{OUT} = –200 mA

Figure 9. R_{ON} vs V_{IN}



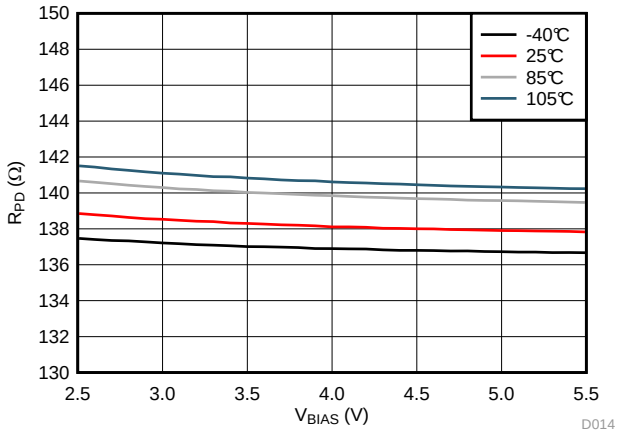
T_A = 25°C V_{ON} = 5 V I_{OUT} = –200 mA

Figure 10. R_{ON} vs V_{IN}



T_A = 25°C V_{ON} = 5 V I_{OUT} = –200 mA

Figure 11. R_{ON} vs V_{BIAS}



V_{IN} = 1.8 V I_{OUT} = 10 mA V_{ON} = 0 V

Figure 12. R_{PD} vs V_{BIAS}

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Typical DC Characteristics (continued)

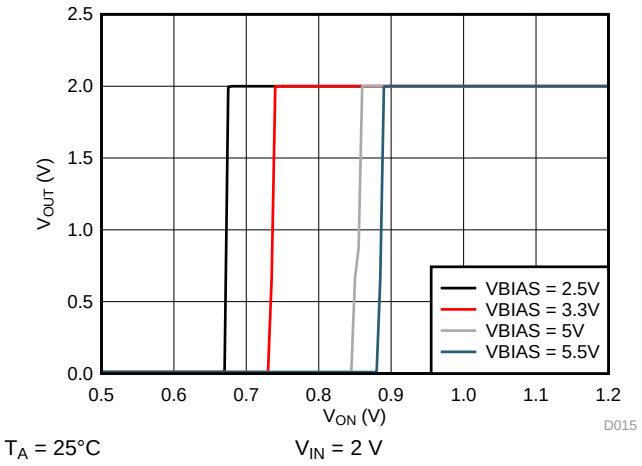

Figure 13. V_{OUT} vs V_{ON}

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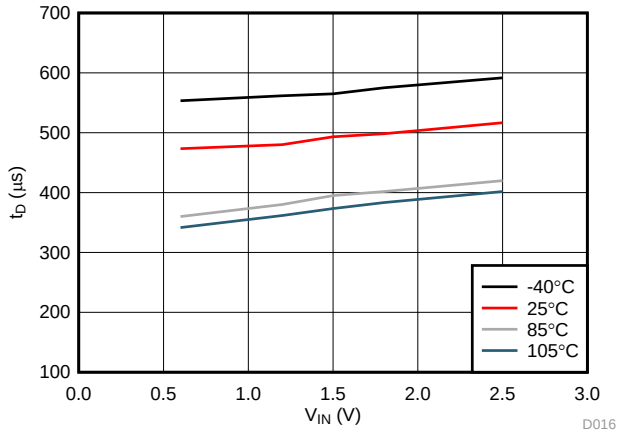
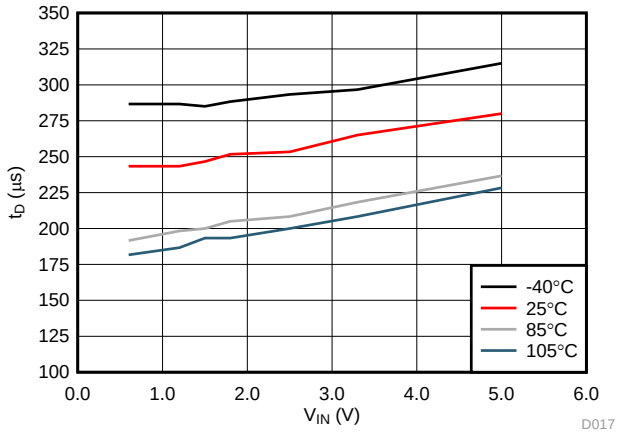
7.10 Typical AC Characteristics

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified)



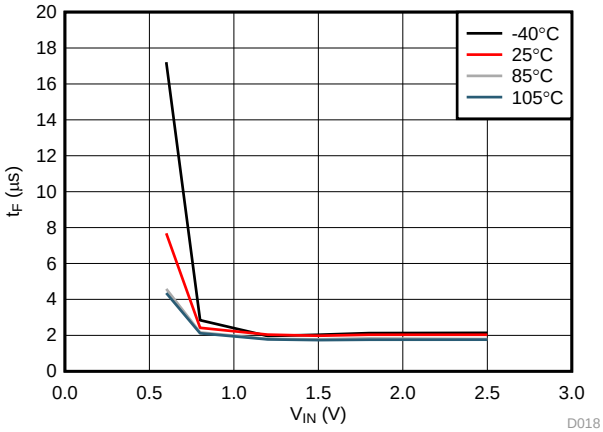
V_{BIAS} = 2.5 V CT= 1000 pF

Figure 14. t_D vs V_{IN}



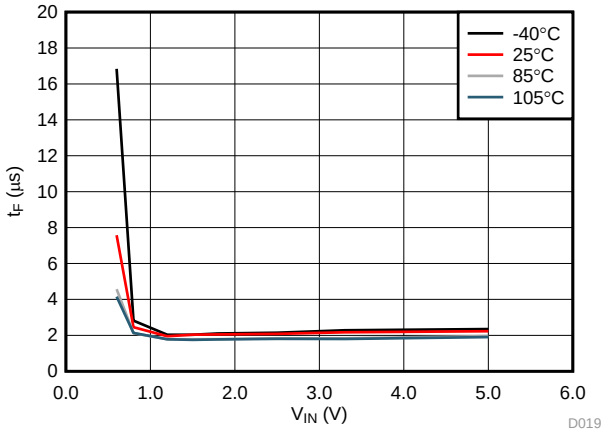
V_{BIAS} = 5 V CT = 1000 pF

Figure 15. t_D vs V_{IN}



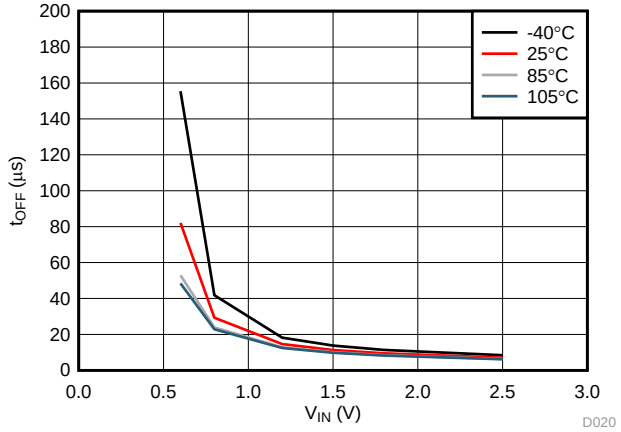
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 16. t_F vs V_{IN}



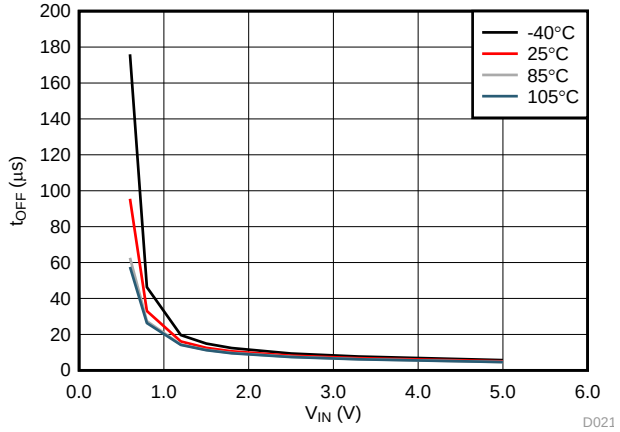
V_{BIAS} = 5 V CT = 1000 pF

Figure 17. t_F vs V_{IN}



V_{BIAS} = 2.5 V CT = 1000 pF

Figure 18. t_{OFF} vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

Figure 19. t_{OFF} vs V_{IN}

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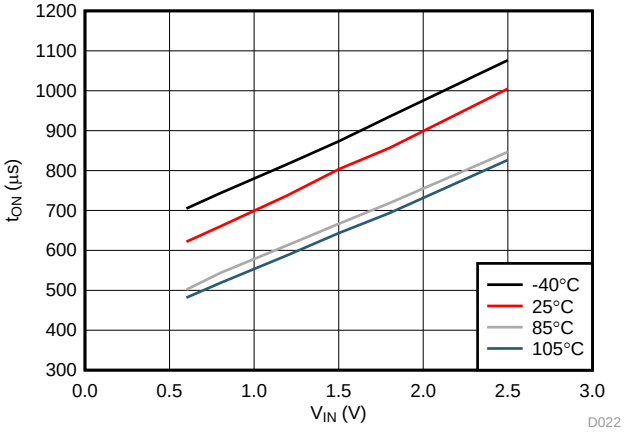
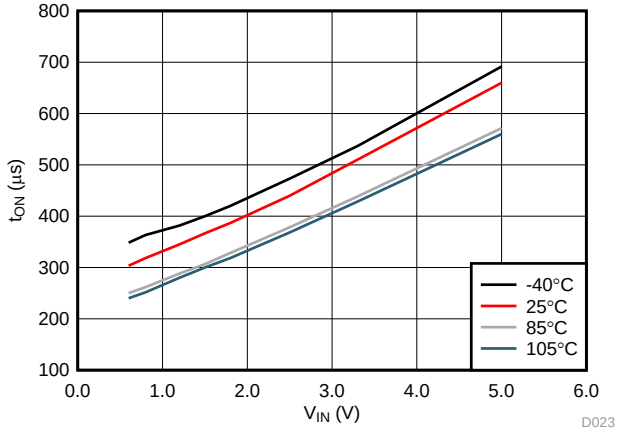
Typical AC Characteristics (continued)



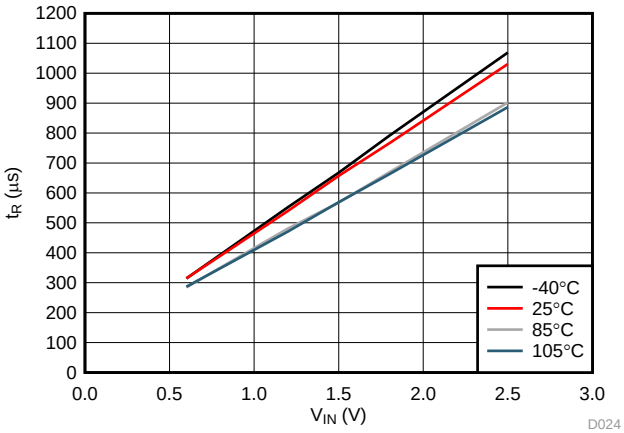
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 20. t_{ON} vs V_{IN}



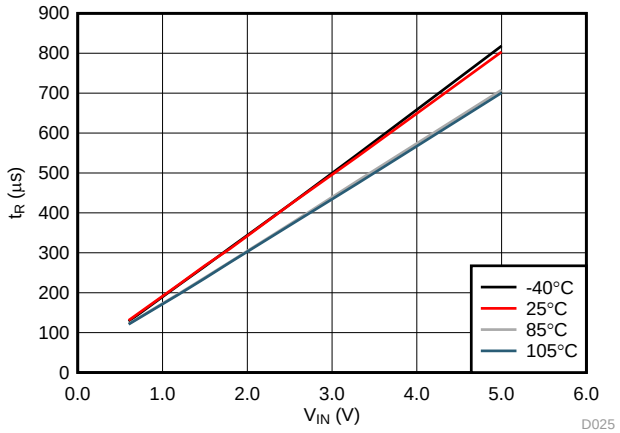
V_{BIAS} = 5 V CT = 1000 pF

Figure 21. t_{ON} vs V_{IN}



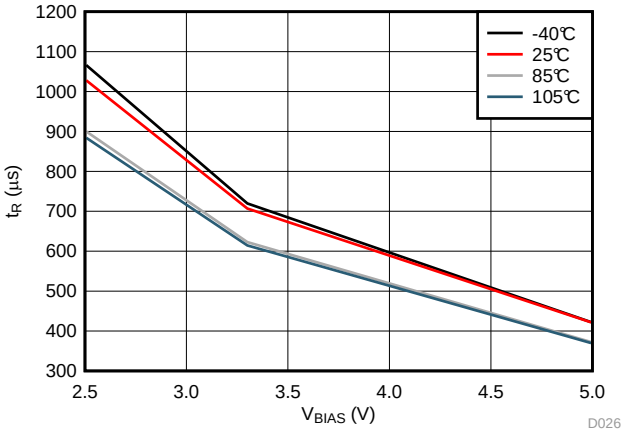
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 22. t_R vs V_{IN}



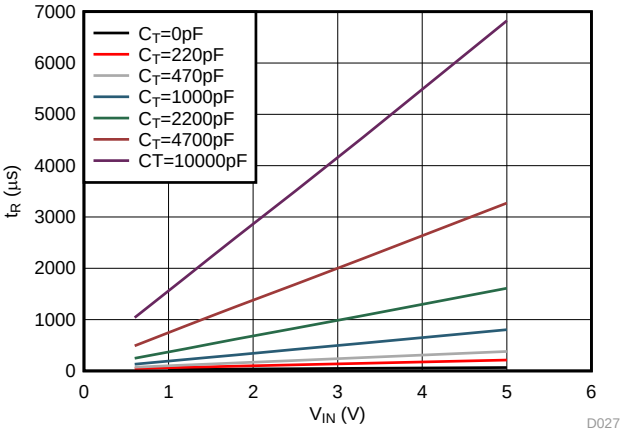
V_{BIAS} = 5 V CT = 1000 pF

Figure 23. t_R vs V_{IN}



V_{IN} = 2.5 V CT = 1000 pF

Figure 24. t_R vs V_{BIAS}



V_{BIAS} = 5 V T_A = 25°C

Figure 25. t_R vs V_{IN}

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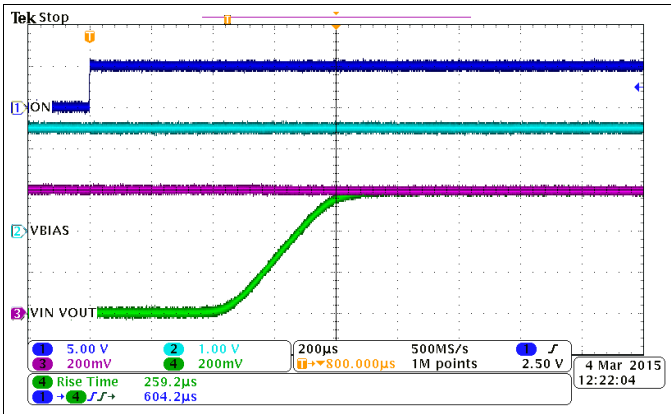
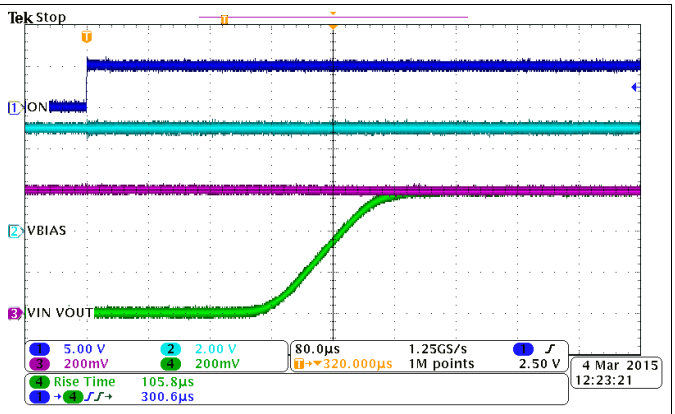
Typical AC Characteristics (continued)



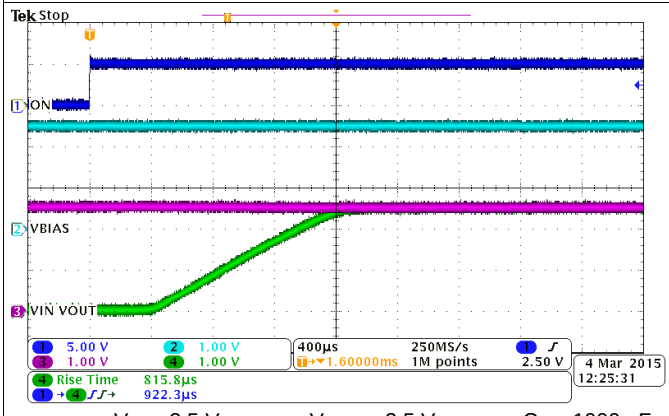
V_{IN} = 0.6 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 26. Turn-on Response Time



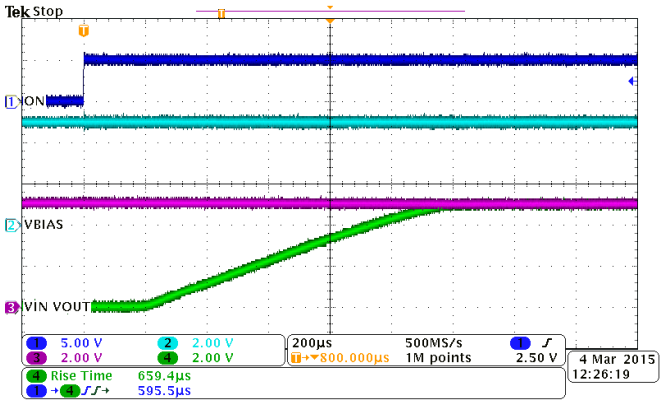
V_{IN} = 0.6 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 27. Turn-on Response Time



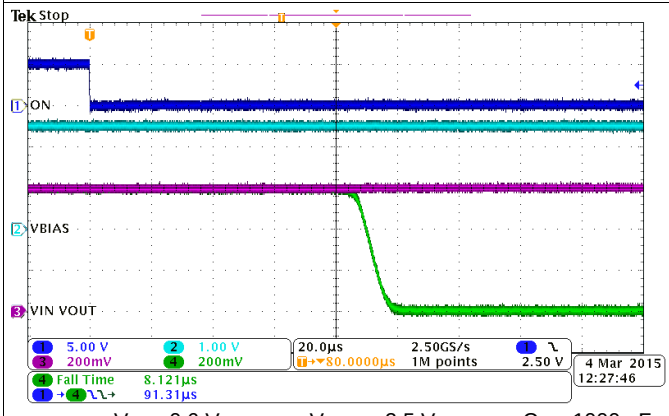
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 28. Turn-on Response Time



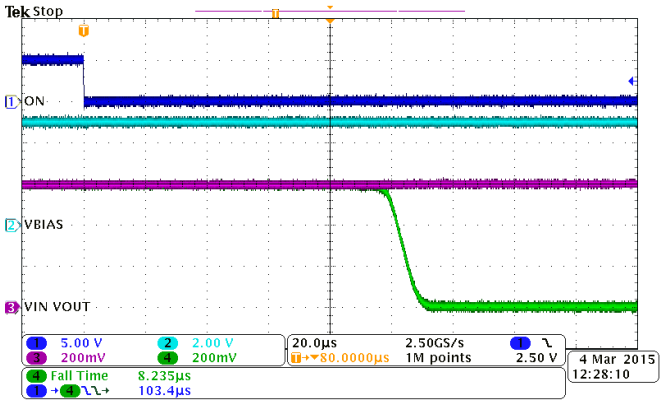
V_{IN} = 5 V V_{BIAS} = 5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 29. Turn-on Response Time



V_{IN} = 0.6 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

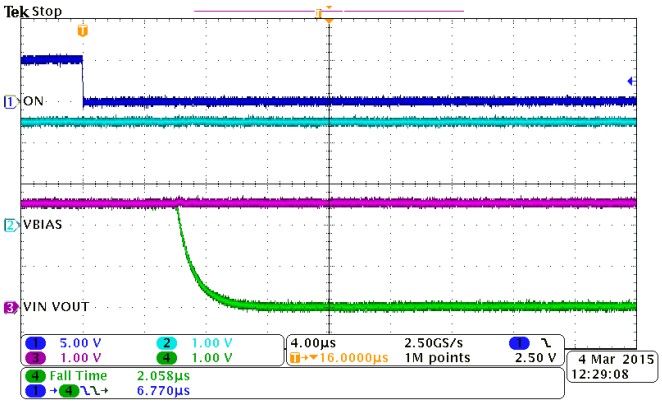
Figure 30. Turn-Off Response Time



V_{IN} = 0.6 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

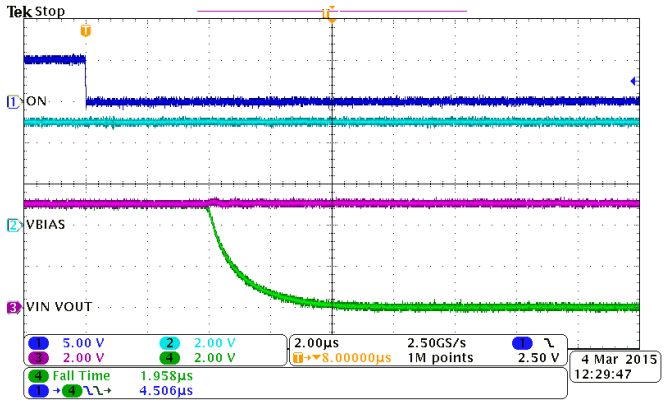
Figure 31. Turn-off Response Time

Typical AC Characteristics (continued)



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 32. Turn-off Response Time



V_{IN} = 5 V V_{BIAS} = 5 V C_T = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 33. Turn-on Response Time

8 Parameter Measurement Information

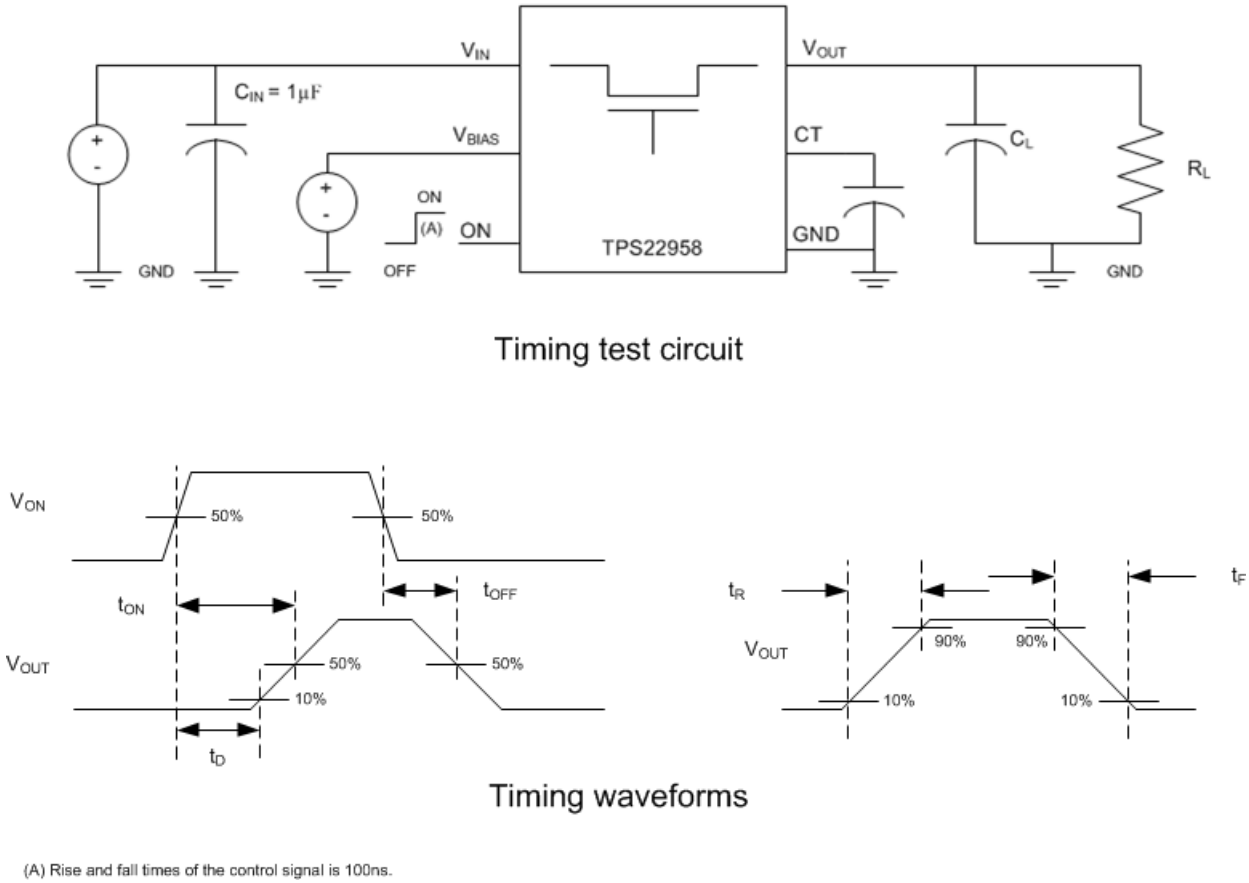


Figure 34. Test Circuit and Timing Waveforms

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9 Detailed Description

9.1 Overview

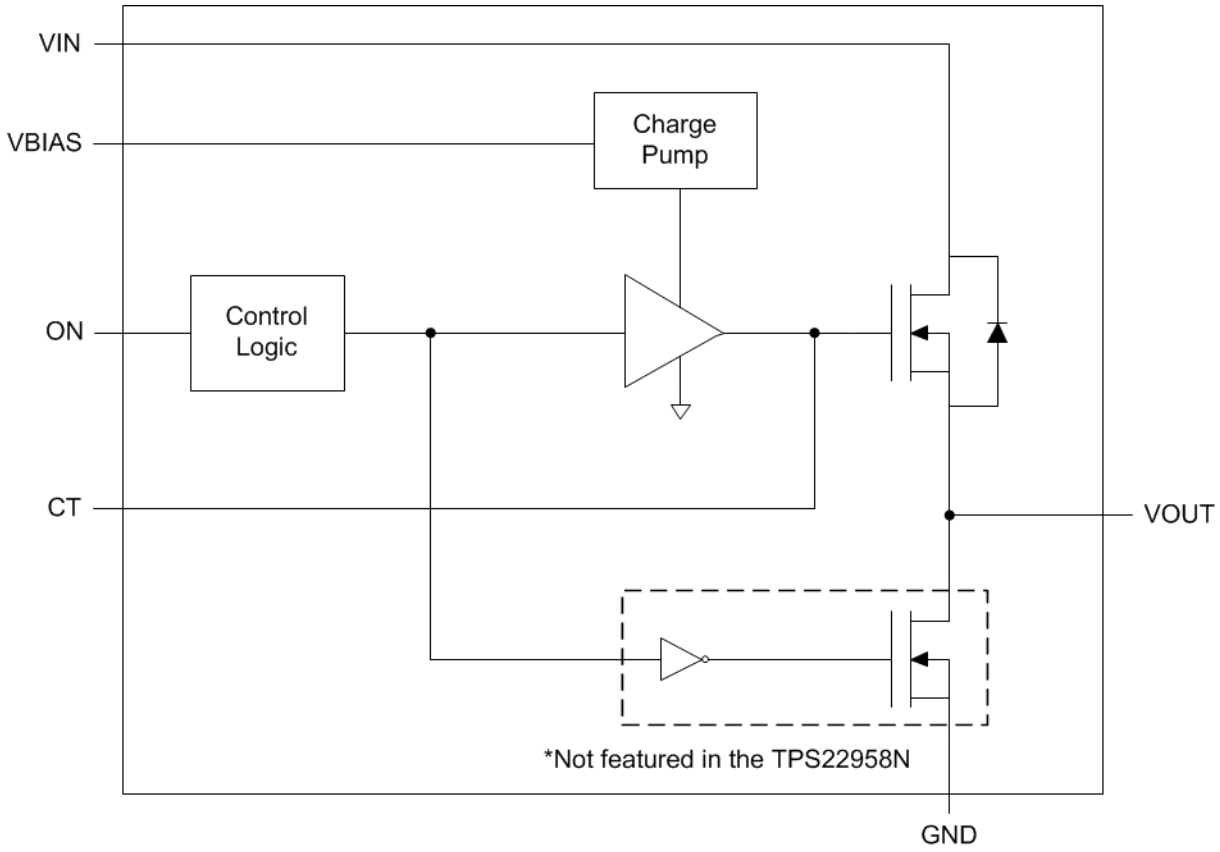
This device is a 5.5 V, 4 A / 6 A, single channel load switch with an adjustable rise time. The device contains an N-channel MOSFET controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn on. The slew rate is set by connecting a capacitor from the CT pin to GND.

The slew rate is proportional to the capacitor on the CT pin. Refer to the *Adjustable Rise Time* section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 to 5.5 V. This circuitry includes the charge pump, QOD, and control logic. For these internal blocks to function correctly, a voltage between 2.5 and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS and the ON pin goes low, the QOD turns on. This connects VOUT to GND through an on-chip resistor and is not a feature for the TPS22958N. The typical pull-down resistance (R_{PD}) is 135 Ω.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

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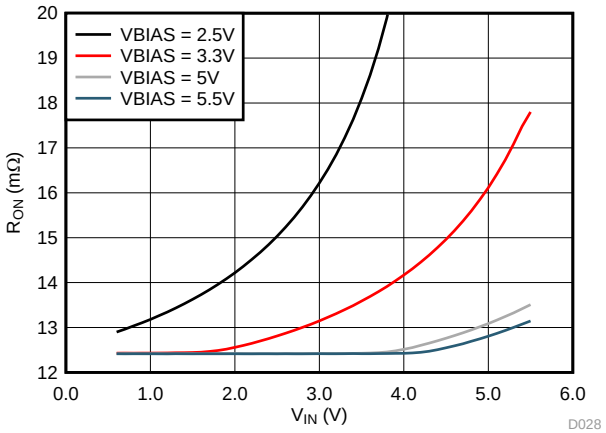
Feature Description (continued)

9.3.2 Quick Output Discharge (QOD)

The TPS22958 includes a QOD feature while the TPS22958N does not. When the device is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 135 Ω and prevents the output from floating while the switch is disabled.

9.3.3 VIN and VBIAS Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still function if $V_{IN} > V_{BIAS}$ but will exhibit an R_{ON} greater than what is listed in the Electrical Characteristics table. See Figure 35 for an example of a typical device. R_{ON} increases as V_{IN} exceeds the V_{BIAS} voltage. For the maximum voltage ratings on the VIN and VBIAS pins, please refer to the Absolute Maximum Ratings table.



T_A = 25°C I_{OUT} = -200 mA V_{ON} = 5 V

Figure 35. R_{ON} vs V_{IN}

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Feature Description (continued)

9.3.4 Adjustable Rise Time

A capacitor from the CT pin to GND sets the slew rate, and it should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with V_{BIAS} = 5 V is:

SR = 0.146 × CT + 14.78

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 14.78 is µs/V.
- The units for the constant 0.146 is µs/(V×pF) (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

Table 1. Rise Time Table

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 0.8 V	VIN = 0.6 V
0	79	59	41	37	33	26	23
220	227	158	97	86	74	55	48
470	397	270	160	139	116	88	72
1000	769	522	301	258	211	153	126
2200	1659	1118	640	548	450	315	256
4700	3445	2314	1315	1128	927	656	528
10000	7310	4884	2778	2372	1950	1379	1103

9.4 Device Functional Modes

The following table lists the VOUT pin connections for a particular device as determined by the ON pin.

Table 2. VOUT Functional Table

ON (Control Input)	TPS22958	TPS22958N
L	GND	Open
H	VIN	VIN

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10 Application and Implementation

10.1 Application Information

10.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor can be placed between VIN and GND. A 1 µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends to have an input capacitor about 10× higher than the output capacitor to avoid excessive voltage drop.

10.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI recommends a C_{IN} greater than C_L. A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

10.1.3 Power Supply Sequencing Without a GPIO Input

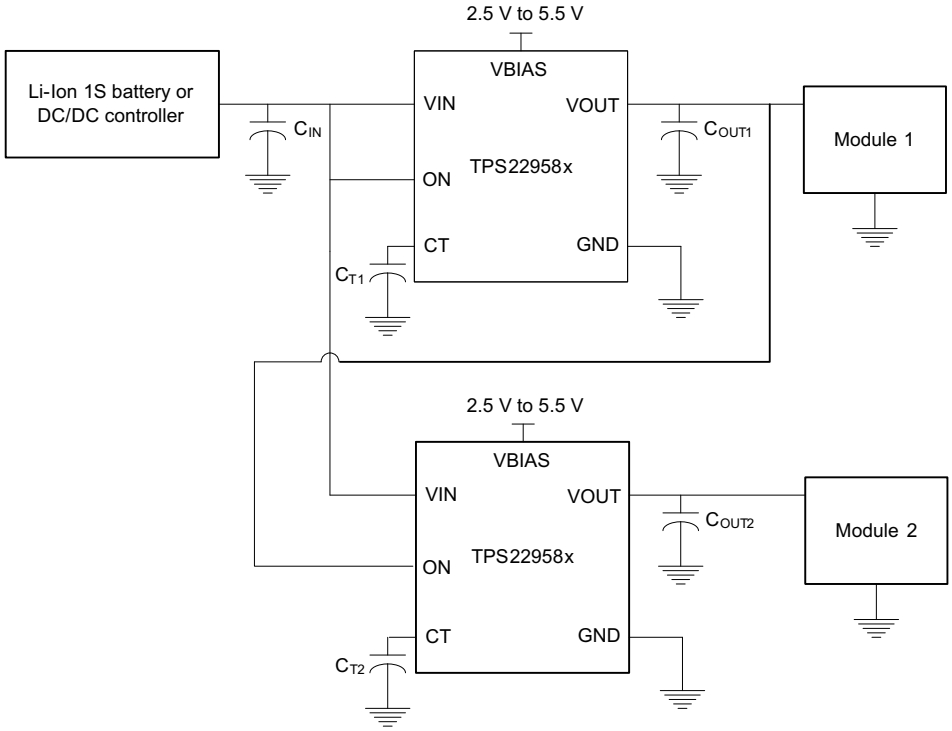

Figure 36. Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a pre-determined manner. The TPS22958x can solve the problem of power sequencing without adding any complexity to the overall system. Figure 36 shows the configuration required for powering up two modules in a fixed sequence. The output of the first load switch is tied to the enable of the second load switch, so when Module 1 is powered the second load switch is enabled and Module 2 is powered.

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10.2 Typical Application

This application demonstrates how the TPS22958 can be used to power a downstream load with a large capacitance. The example in Figure 37 is powering a 22 µF capacitive output load.

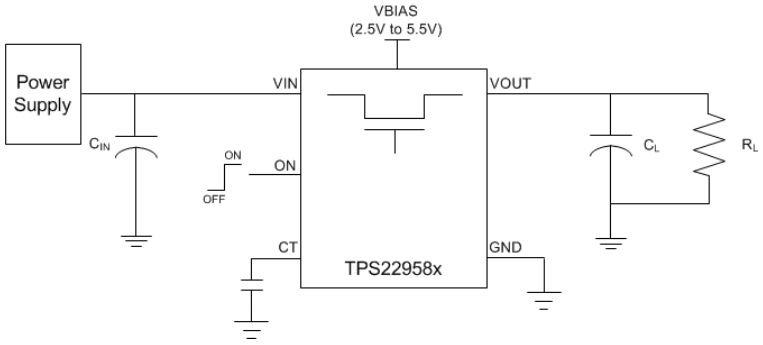

Figure 37. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5.0 V
Load current	4 A
Output capacitance (C_L)	22 µF
Allowable inrush current on VOUT	0.33 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current
- Allowable inrush current on VOUT due to C_L capacitor

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 2 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (2)$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 3.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled (3)

The device offers adjustable rise time for VOUT and allows the user to control the inrush current during turn-on through the CT pin. The appropriate rise time can be calculated using the design requirements and the inrush current equation (Equation 3).

330 mA = 22 µF × 3.3 V / dt (4)

dt = 22 µF × 3.3 V / 300mA (5)

dt = 220 µs (6)

To ensure an inrush current of less than 330 mA, choose a CT based on Table 1 or Equation 1 value that will yield a rise time of more than 220 µs. See the oscilloscope captures in the *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current. See Table 1 for correlation between rise times and CT values.

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.2.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 7.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}}$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22958)
- T_A = ambient temperature of the device
- $R_{\theta JA}$ = junction to air thermal impedance. See *Thermal Information* . This parameter is highly dependent upon board layout. (7)

For the DGK package, V_{BIAS} = 5 V, and V_{IN} = 3.3 V, the maximum ambient temperature with a 4 A load can be determined by using the following calculation:

$$P_D = I^2 \times R \quad (8)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times I^2 \times R \quad (10)$$

$$T_A = 125°C - 185.7°C/W \times (4\ A)^2 \times 20\ m\Omega = 65.6°C \quad (11)$$

Therefore, with the conditions mentioned above, a maximum ambient temperature of 65.6°C is recommended.

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For the DGN package, V_{BIAS} = 5 V, and V_{IN} = 3.3 V, the maximum ambient temperature with a 4 A load can be determined by using the following calculation:

$$P_D = I^2 \times R \quad (12)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (13)$$

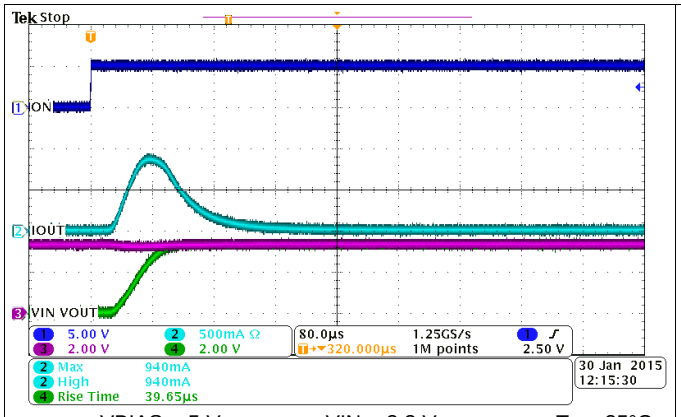
$$T_A = T_{J(MAX)} - R_{\theta JA} \times I^2 \times R \quad (14)$$

$$T_A = 125°C - 67.0°C/W \times (4\ A)^2 \times 20\ m\Omega = 103.6°C \quad (15)$$

Therefore, with the conditions mentioned above, a maximum ambient temperature of 103.6°C is recommended.

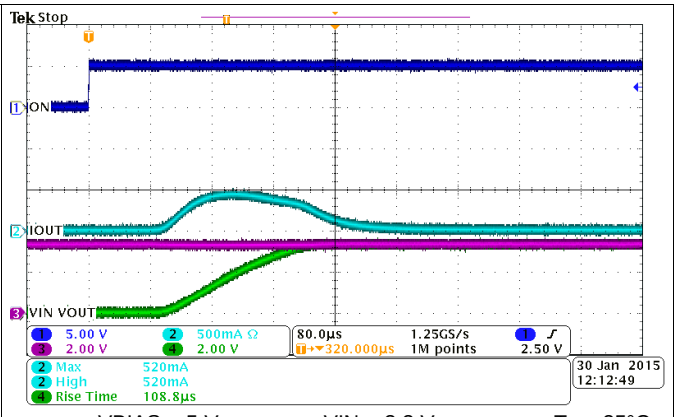
10.2.3 Application Curves

The three scope captures show the usage of a CT capacitor in conjunction with the device. A higher CT value results in a slower rise and a lower inrush current.



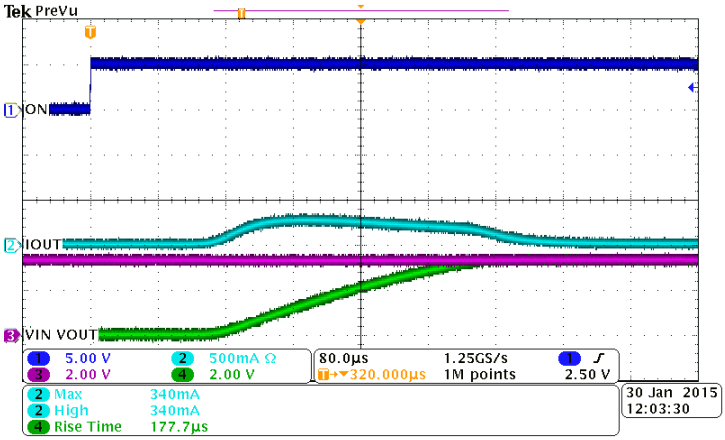
VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = Open C_L = 22µF

Figure 38. Inrush Current Without CT Capacitor



VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = 220 pF C_L = 22µF

Figure 39. Inrush Current With CT = 220 pF



VBIAS = 5 V VIN = 3.3 V
CT = 470 pF C_L = 22µF T_A = 25°C

Figure 40. Inrush Current With CT = 470 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 to 5.5 V and V_{IN} range of 0.6 to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using the minimum recommended input capacitance of 1 uF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input. To avoid ringing on the VBIAS pin from a noisy power supply, a bypass capacitance of 0.1 µF is recommended.

The requirements for large input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

12 Layout

12.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current. When connecting the two VIN or VOUT pins together, an equal trace length should be used to avoid an unequal distribution of current through each pin.
- Use vias under the exposed thermal pad to connect to the power ground plane for thermal relief during high current operation.
- VIN pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- VOUT pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The CT capacitor should be placed as close to the device pins as possible. The typical recommended CT capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

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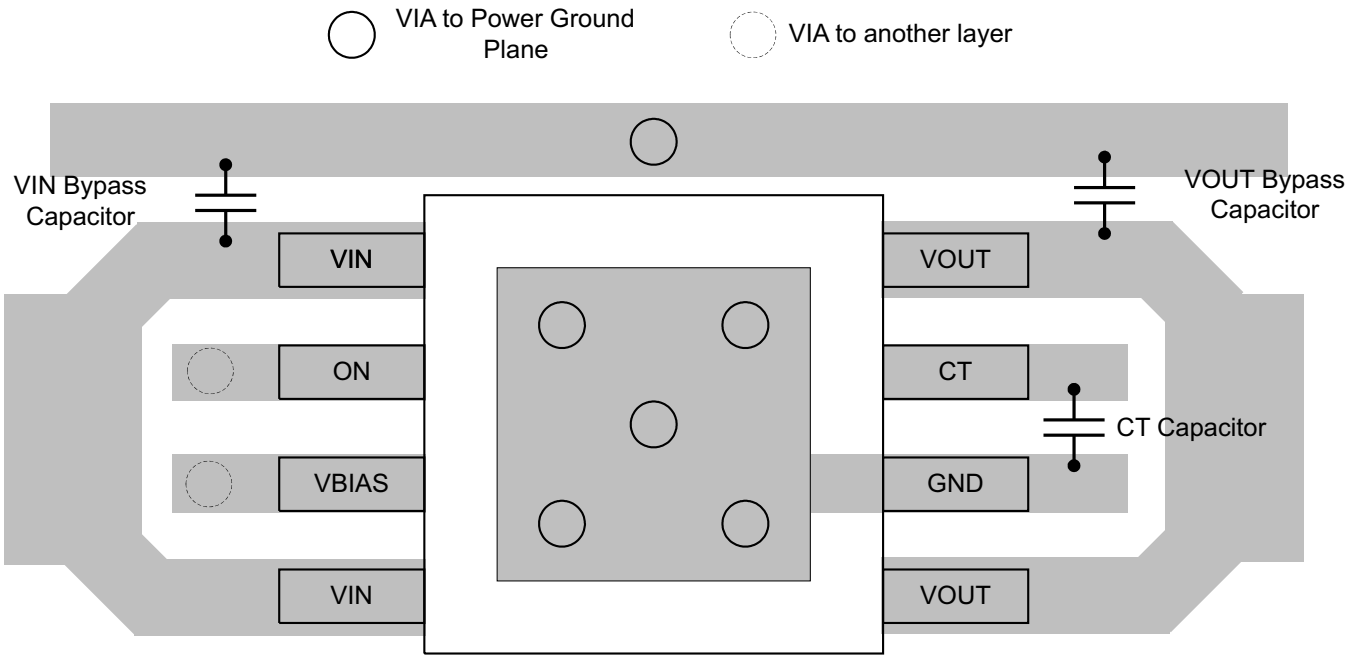
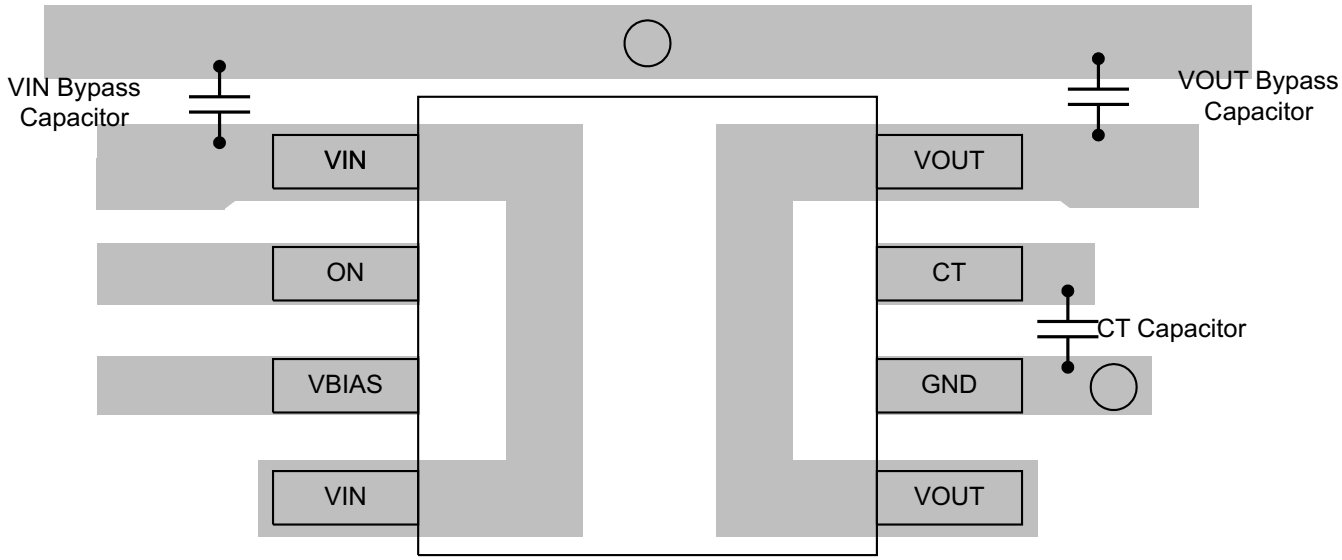
12.2 Layout Example



DGN Package



DGK Package

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22958	Click here	Click here	Click here	Click here	Click here
TPS22958N	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22958DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	(ZBUO, ZBUX)	Samples
TPS22958DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBVX	Samples
TPS22958NDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBWX	Samples
TPS22958NDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBXX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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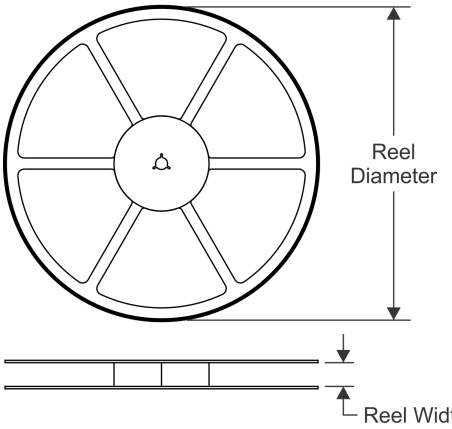
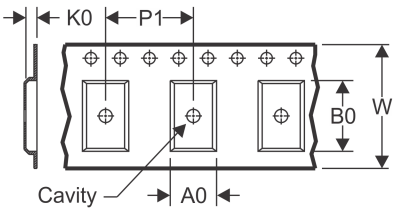
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

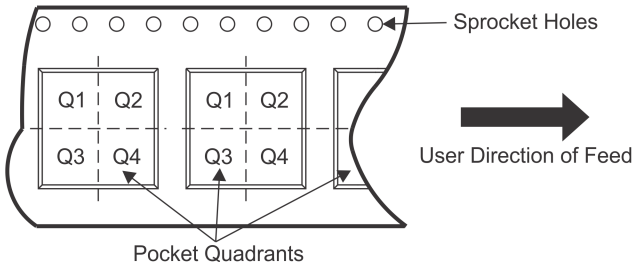


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

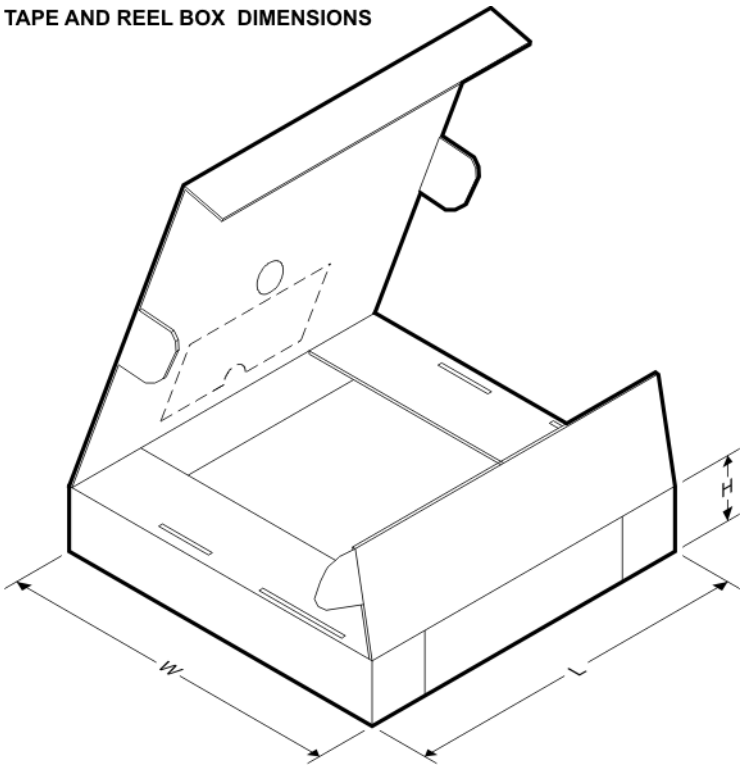
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22958DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS22958DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958NDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958NDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

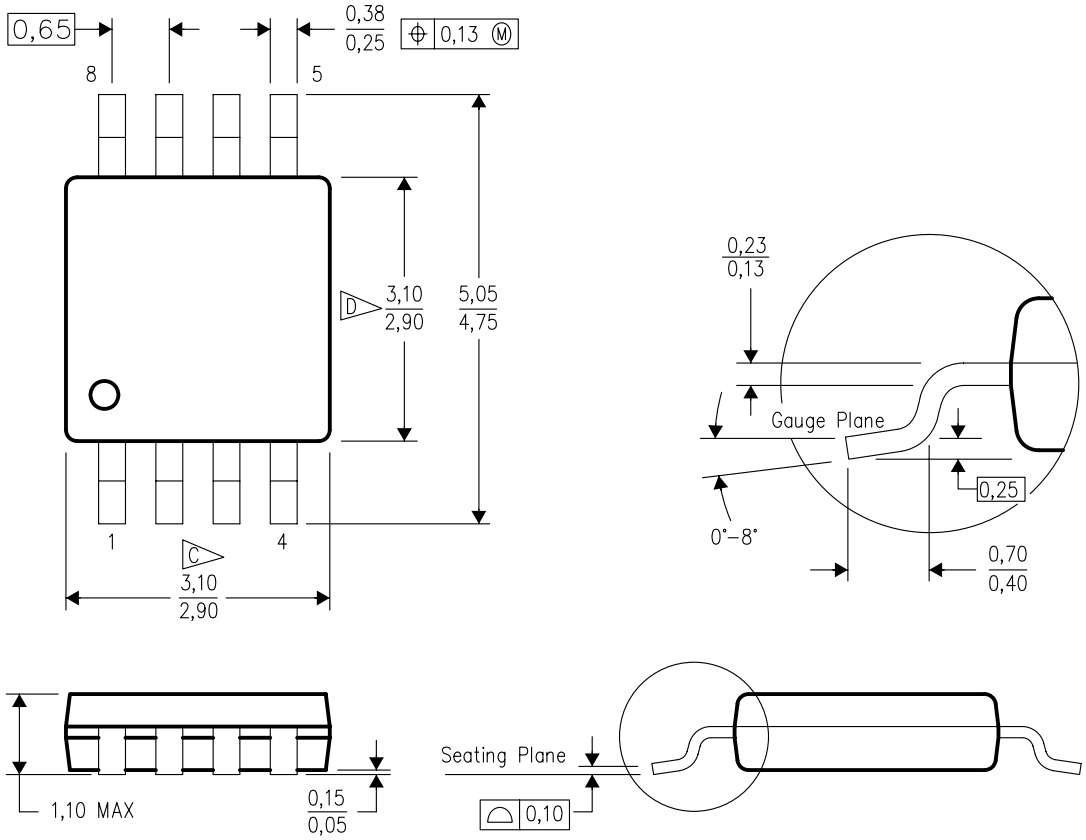
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22958DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
TPS22958DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TPS22958DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS22958NDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TPS22958NDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0

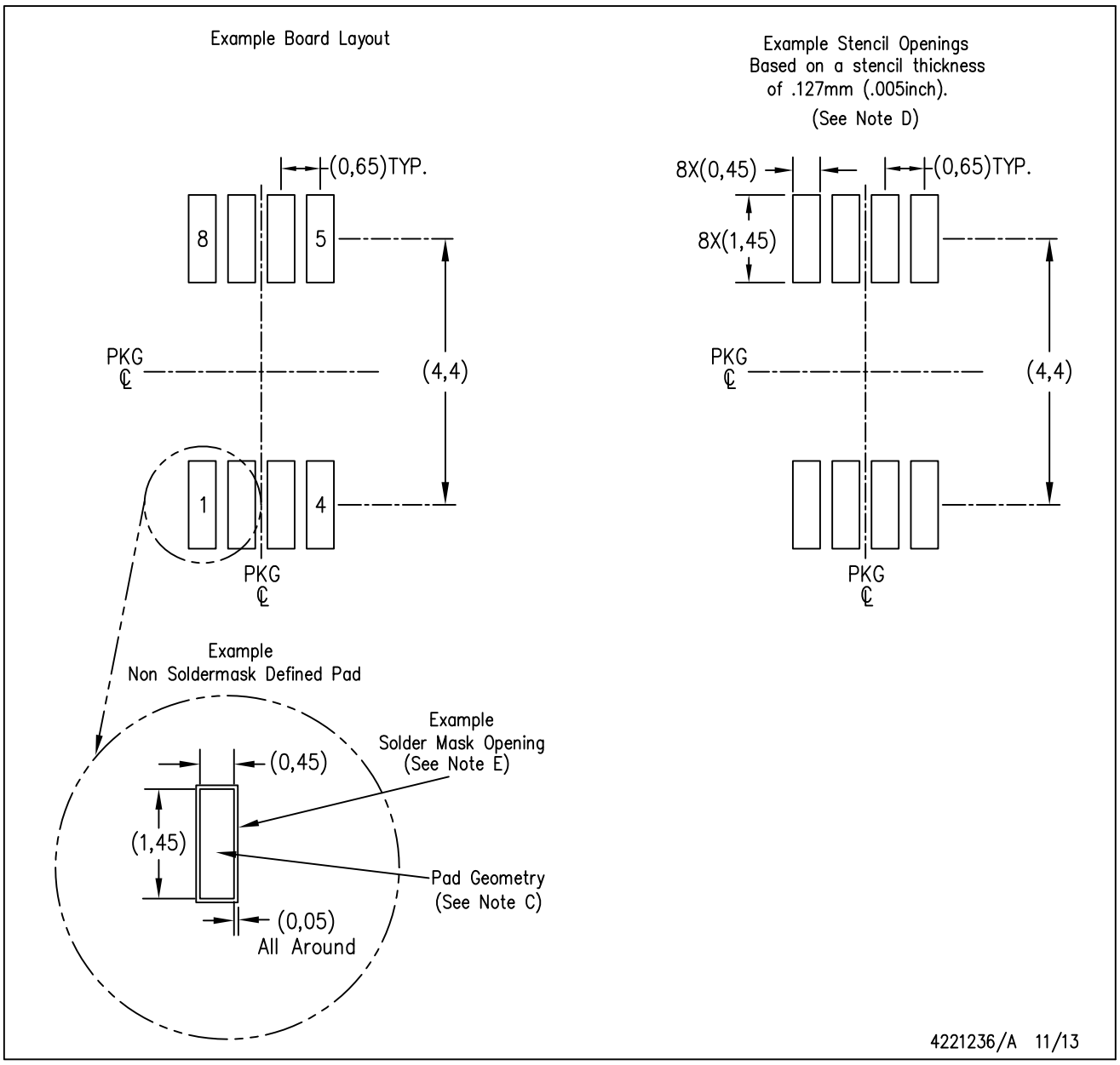
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

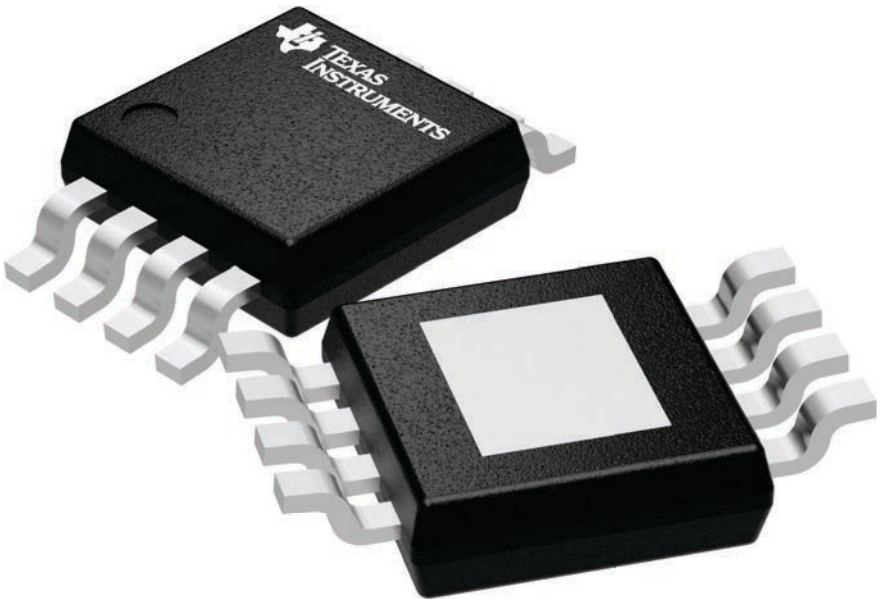
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

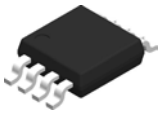
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

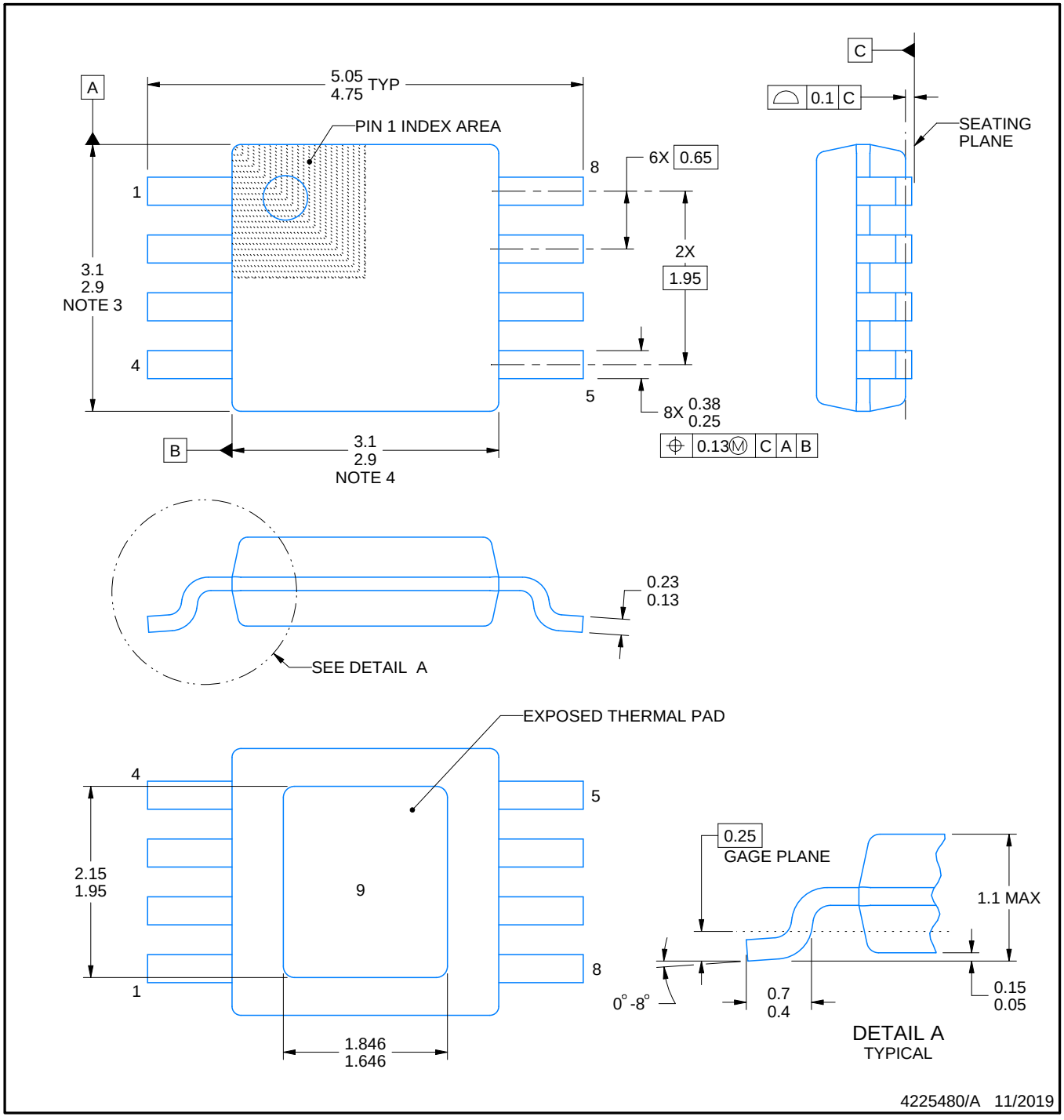
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

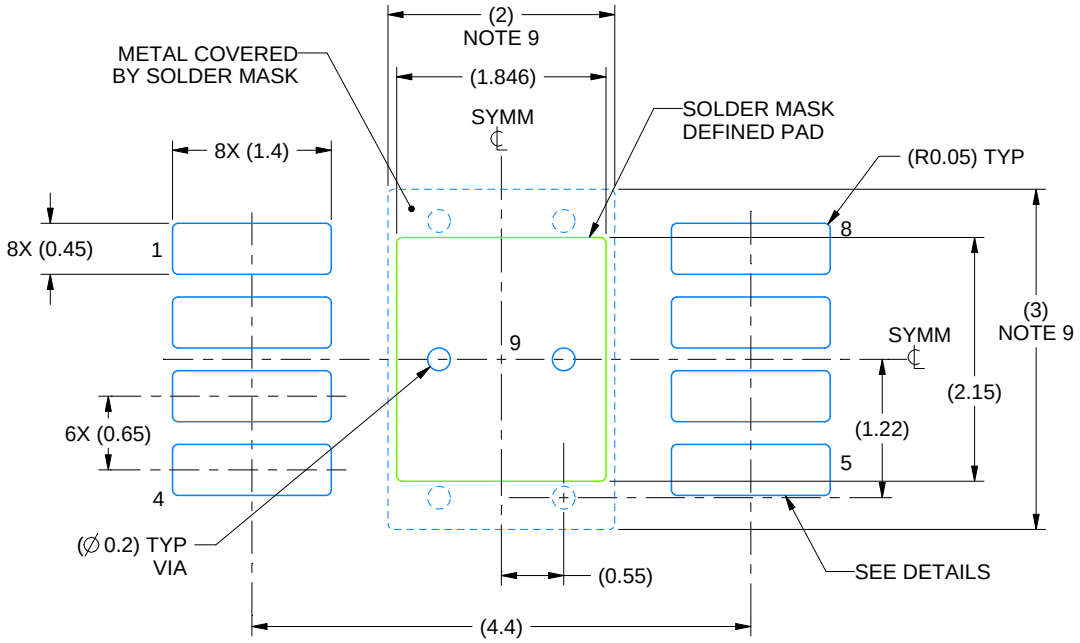
SMALL OUTLINE PACKAGE



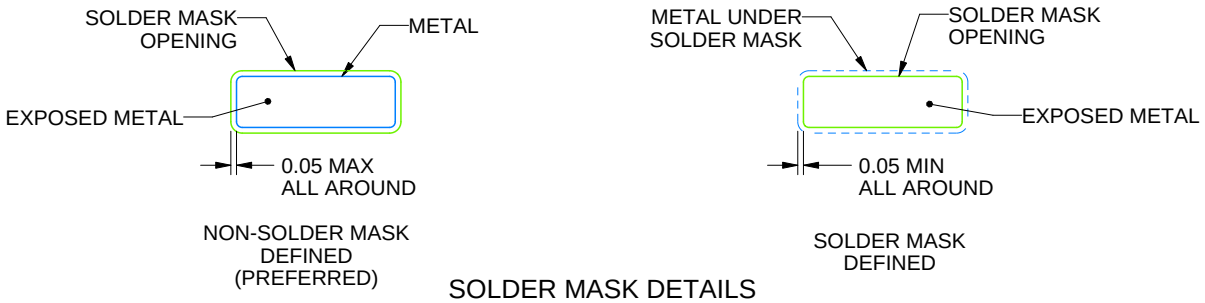
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

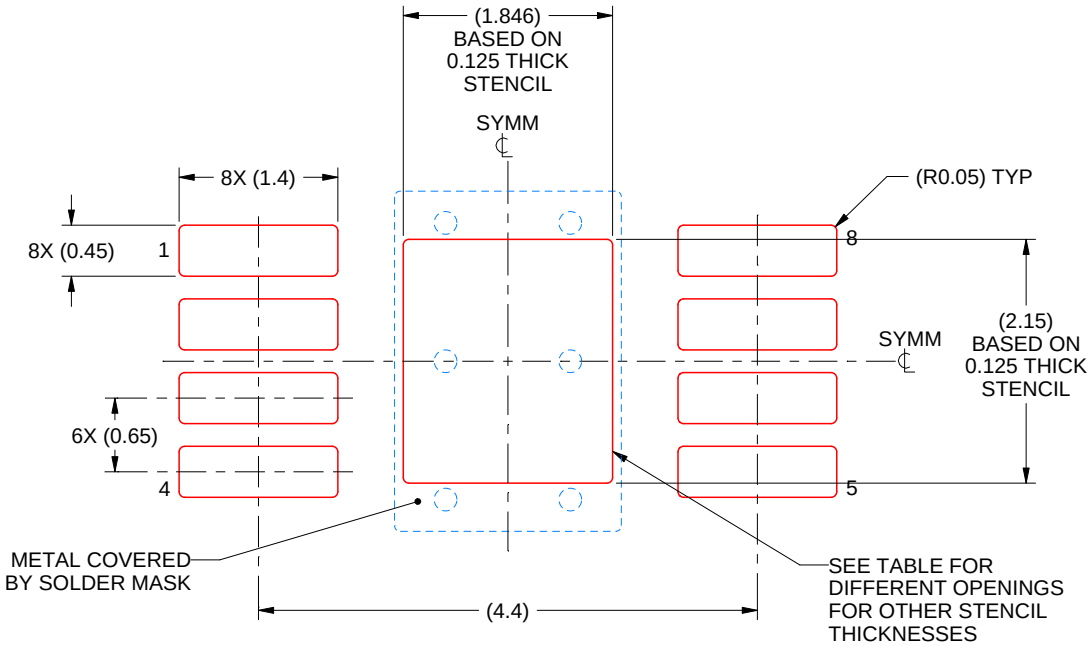


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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