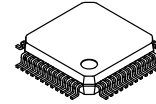


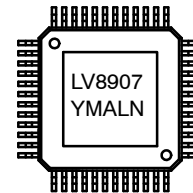
Sensorless Three-phase BLDC Motor Controller and Predriver, Automotive

LV8907UW



SPQFP48 7x7
CASE 131AN

MARKING DIAGRAM



Y = Production Year
M = Production Month
A = Assembly Start Week
LN = Lot Number

Overview

The LV8907 is a high performance, sensorless three-phase Brushless DC (BLDC) motor controller with predrivers for automotive applications. An integrated two-stage charge pump provides gate current for a wide range of ultra low $R_{DS(ON)}$ NFETs. The device offers a rich set of system protection and diagnostic functions such as overcurrent, overvoltage, short-circuit, undervoltage, overtemperature and many more. It supports open-loop as well as closed-loop speed control with user configurable startup, speed setting and proportional/integral (PI) control coefficients, making it suitable for a wide range of motor and load combinations. With a built-in linear regulator for powering external circuits, a watchdog timer, and a LIN (Local Interconnect Network) transceiver, the LV8907 offers a very small system solution.

The LV8907 stores system parameters in embedded one-time programmable (OTP) non-volatile memory in addition to RAM system memory. An SPI interface is provided for parameter setting and monitoring the system status. With the operating junction temperature tolerance up to 175°C and electrically LIN compatible control signals (PWM and Enable), the LV8907 is an ideal solution for stand-alone BLDC motor control systems.

Features

- AEC-Q100 Qualified and PPAP Capable
- Operating Junction Temperature Up to 175°C
- Operating Voltage Range from 5.5 V to 20 V with Tolerance from 4.5 V to 40 V
- Embedded Proprietary Sensorless Trapezoidal and Pseudo-sinusoidal Commutation
- Supports Open-loop as well as Closed-loop Speed Control
- Integrated Predrivers for Driving Six N-MOSFETs
- Two-stage Charge Pump for Continuous 100% Duty Cycle Operation
- 5 V /3.3 V Regulator, LIN Transceiver and Watchdog Timer Applications Using an External Microcontroller
- Configurable Speed Settings and PI Control Coefficients
- Various System Protection Features Including:
 - ◆ Shoot through Protection Using Configurable Dead Time
 - ◆ Drain-source Short Detection
 - ◆ Cycle-by-cycle Current Limit and Overcurrent Shutdown
 - ◆ Overvoltage and Undervoltage Shutdown
 - ◆ Overtemperature Warning and Shutdown
 - ◆ Input PWM Fault Detection

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|---------|-----------------------|
| LV8907UWR2G | SQFP48K | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Applications

- Pumps (Fuel, Oil, Coolant, Hydraulic Controls, vacuum, ...)
- Fans and Blowers (HVAC, Radiator, Condenser, Battery, Inverter, Charger, ...)
- Compressors

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LV8907 BLOCK DIAGRAM

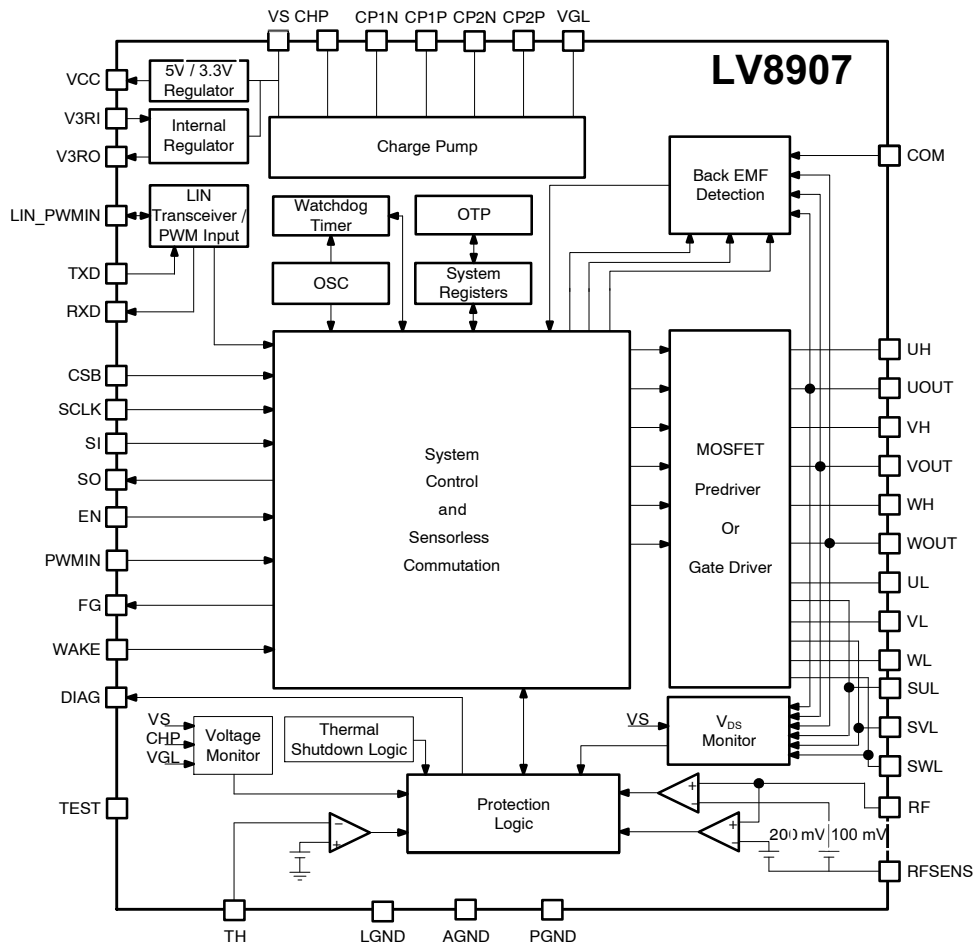


Figure 1. LV8907 Block Diagram

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APPLICATION BLOCK DIAGRAMS

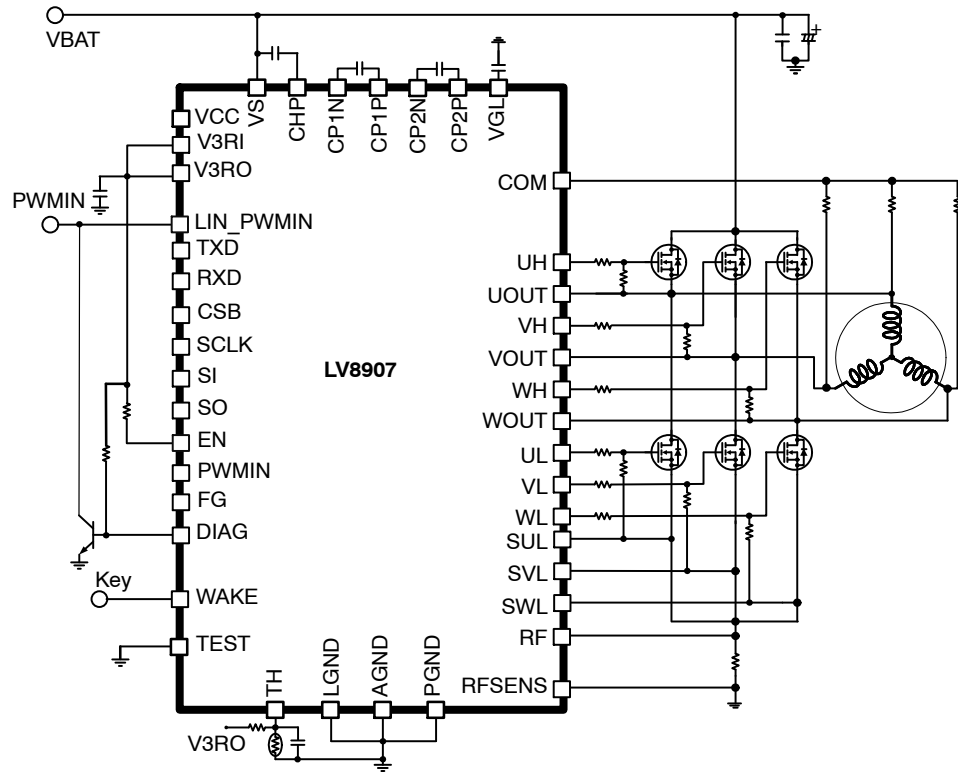


Figure 2. Example of Stand-alone Configuration

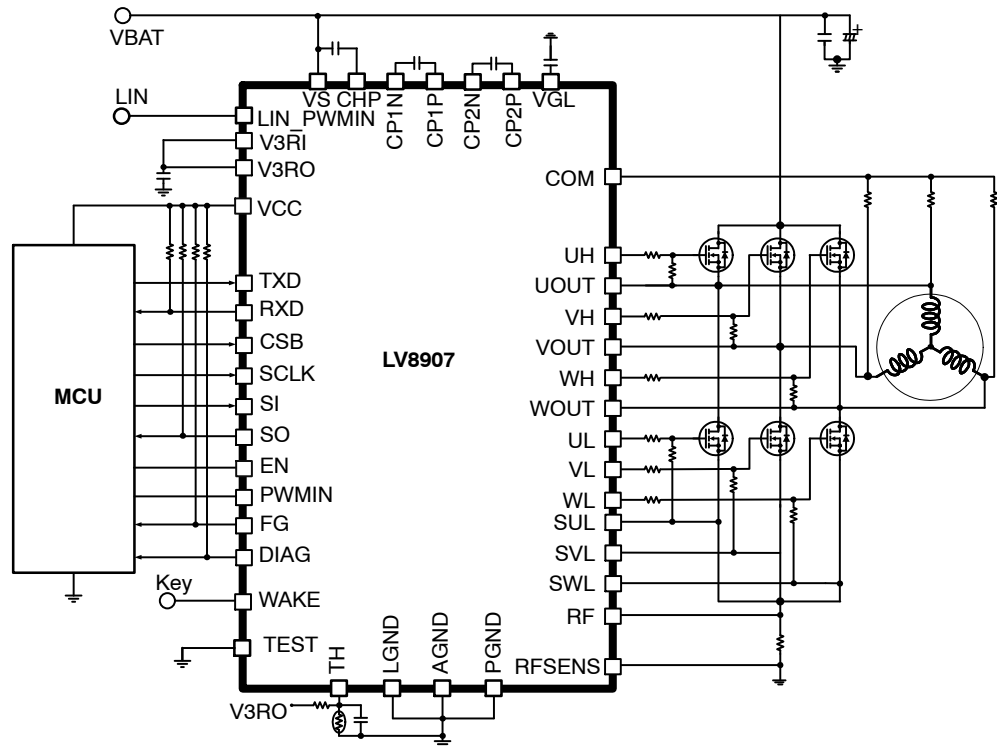


Figure 3. Example of LIN Based Control Configuration

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PIN ASSIGNMENTS

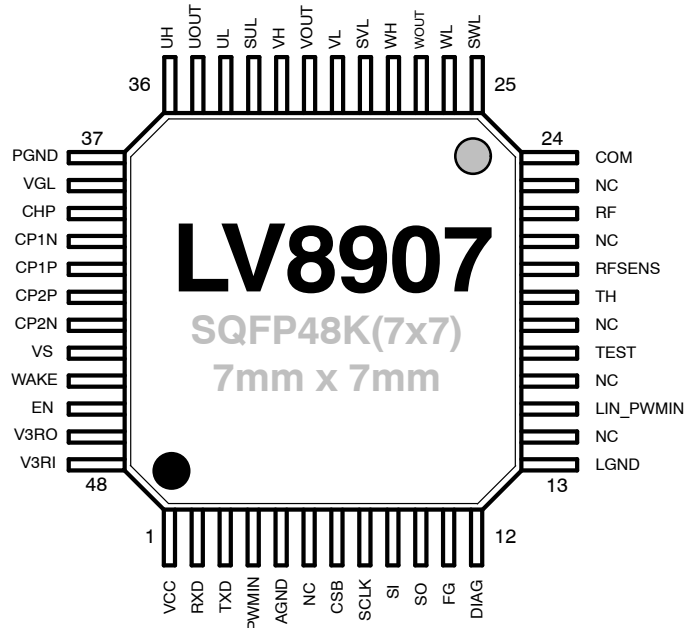


Figure 4. LV8907 Pinout

PIN DESCRIPTION

| Pin Name | Pin No | Description | Page |
|-----------|-----------------------|---|------|
| VCC | 1 | 5 V or 3.3 V regulator output pin. (Selected by internal register setting) Power supply for microcontroller. Connect capacitor to AGND for stability | 14 |
| RXD | 2 | Open drain logic level output of LIN_PWMIN received data. Use pull-up to a voltage less than or equal to VS | 16 |
| TXD | 3 | Logic level input of transmit data for LIN_PWMIN | 16 |
| PWMIN | 4 | Digital level PWM input pin for direct drive or speed register selection details. Input polarity can be programmed for either active high or active low | 15 |
| AGND | 5 | Analog GND pin | |
| NC | 6, 14, 16, 18, 21, 23 | No Connections | |
| CSB | 7 | Active low SPI interface chip selection pin | 19 |
| SCLK | 8 | SPI interface clock input pin | 19 |
| SI | 9 | Active high SPI interface serial data input pin | 19 |
| SO | 10 | Open drain SPI interface serial data output pin | 19 |
| FG | 11 | Open drain back electromotive force (BEMF) transition output pin. The frequency division ratio is selectable via register settings | 18 |
| DIAG | 12 | Programmable open drain diagnostic output | 16 |
| LGND | 13 | LIN Block GND pin. Must be connected to AGND on the PCB | |
| LIN_PWMIN | 15 | LIN transceiver input/output. Register selectable as high voltage PWM input with a $V_{VS}/2$ threshold | 16 |
| TEST | 17 | Factory test pin. Connect to GND | |
| TH | 19 | Thermistor input pin for power stage temperature detection. If the input voltage is below the threshold voltage, an error is triggered. The error threshold is programmable. To disable tie to V3RO | 17 |
| RFSENS | 20 | Shunt resistance reference pin. Connect this pin to the GND side of the Shunt resistor with Kelvin leads | 17 |

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PIN DESCRIPTION (continued)

| Pin Name | Pin No | Description | Page |
|----------------------|----------------|--|------|
| RF | 22 | Output current detect pin. Connect this pin to higher terminal of the shunt resistor with Kelvin leads | 17 |
| COM | 24 | COM input pin. Connect this pin to the motor neutral point if available. This point may be derived from a resistive network with 1k resistors to the phases | 12 |
| SUL SVL SWL | 33 29 25 | Current return path for low-side gate drive. Short-circuit shutoff level is measured between this pin and its corresponding phase pin | 16 |
| UL VL WL | 34 30 26 | Gate driver output pin for the low-side Nch Power FET. Use gate resistors for wave-shaping | 16 |
| UOUT VOUT WOUT | 35 31 27 | Current return path for high-side gate drive and reference for high-side short-circuit shutoff. | 16 |
| UH VH WH | 36 32 28 | Gate driver output pin for the high-side Nch Power FET. Use gate resistors for wave-shaping | 16 |
| PGND | 37 | GND pin for the charge pump | |
| VGL | 38 | Power supply pin for low-side gate drive. Connect decoupling capacitor between this pin and GND | 14 |
| CHP | 39 | Power supply pin for high-side gate drive. Connect decoupling capacitor between this pin and VS | 14 |
| CP1N | 40 | Charge transfer pin of the Charge pump (1N). Connect capacitor between CP1P and CP1N | 14 |
| CP1P | 41 | Charge transfer pin of the Charge pump (1P). Connect capacitor between CP1P and CP1N | 14 |
| CP2P | 42 | Charge transfer pin of the Charge pump (2P). Connect capacitor between CP2P and CP2N | 14 |
| CP2N | 43 | Charge transfer pin of the Charge pump (2N). Connect capacitor between CP2P and CP2N | 14 |
| VS | 44 | Power supply pin | 13 |
| WAKE | 45 | WAKE pin. "H" = Operating mode, "L" or "Open" = Sleep mode. In Sleep mode all gate drivers are high impedance. To protect the power stage, pull-down resistors on the gate lines may be required | 13 |
| EN | 46 | Motor stage Enable pin. "H" = Normal enabled mode; "L" or "Open" = Standby mode. In Standby mode all gate drivers driven low. Motor freewheeling | 13 |
| V3RO | 47 | 3V regulator output pin. Connect capacitor between this pin and AGND | 14 |
| V3RI | 48 | 3V regulator input pin (internally connected to control, and logic circuits). Connect to V3RO pin | 14 |

NOTE: The exposed pad should be either left floating electrically or connected ground.

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PIN CIRCUIT

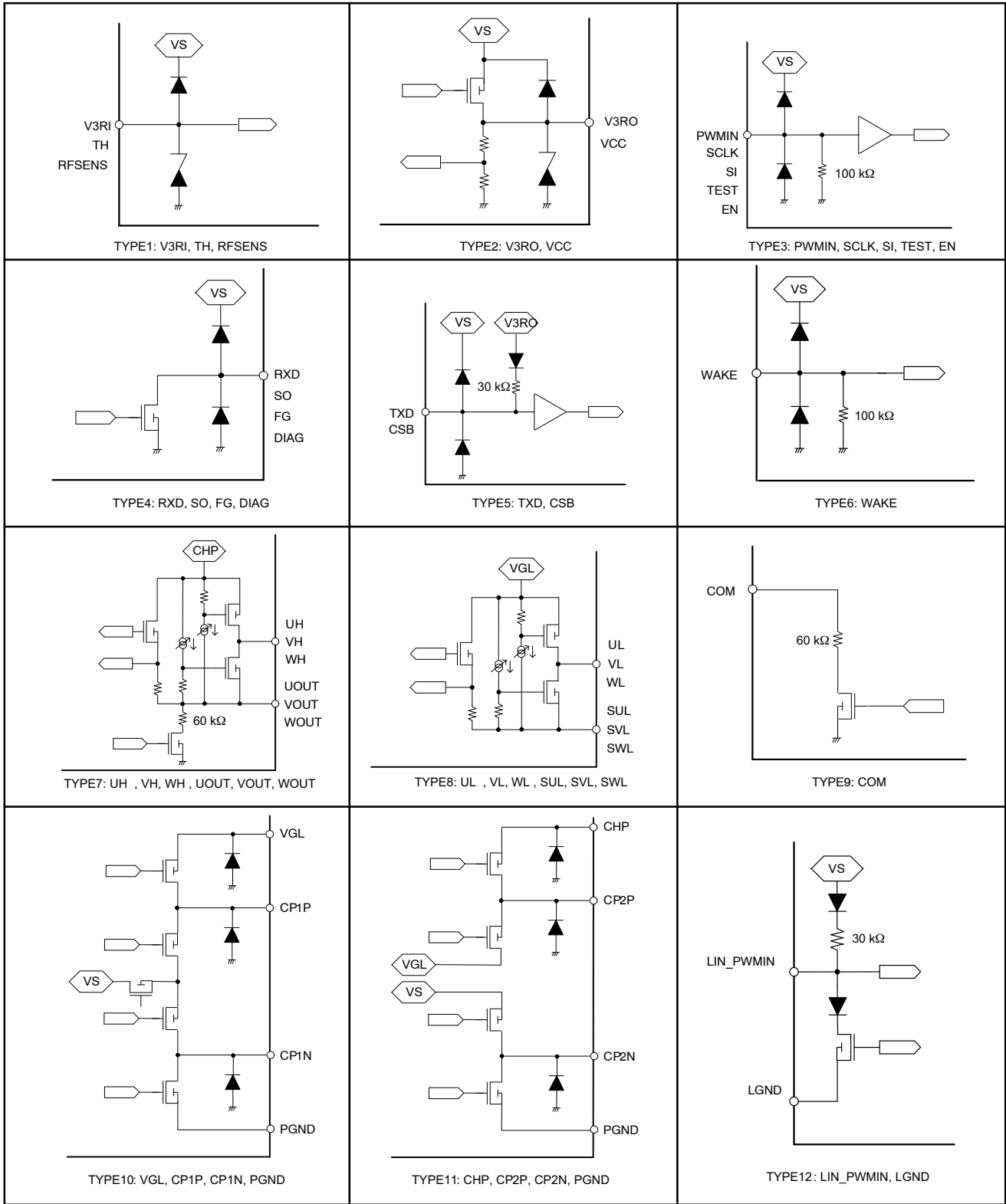


Figure 5. Pin Circuit

LV8907UW

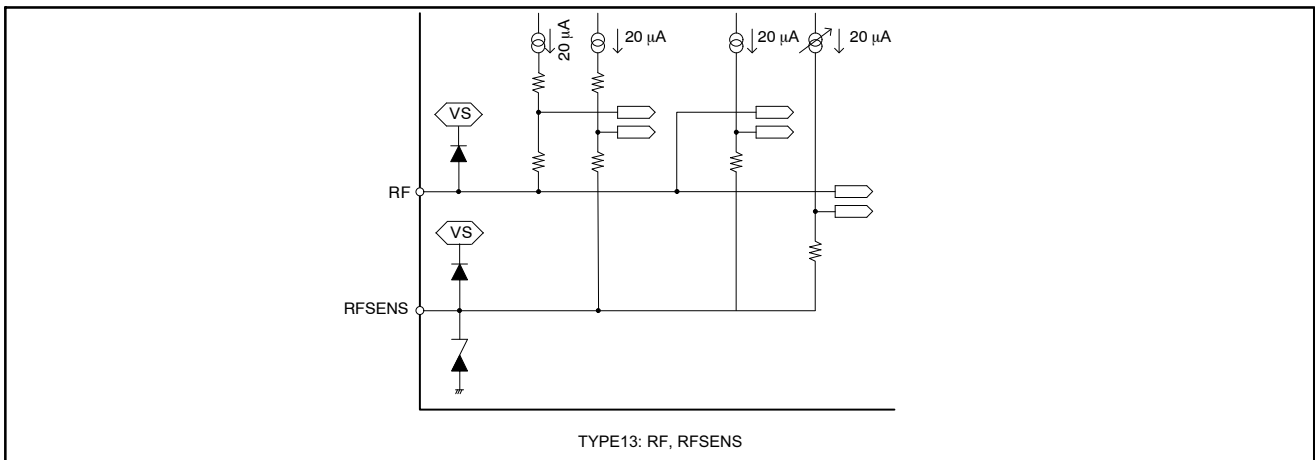


Figure 6. Pin Circuit (continued)

ABSOLUTE MAXIMUM RATINGS

| Parameter | Pins | Ratings | Unit |
|--|--|-------------|------|
| Supply Voltage | VS | -0.3 to 40 | V |
| Charge Pump Voltage (High-side) | CHP | -0.3 to 40 | V |
| Charge Pump Voltage (Low-side) | VGL | -0.3 to 16 | V |
| Logic Power Supply | VR3I, VR3O | -0.3 to 3.6 | V |
| 5 V Regulator Voltage | VCC | -0.3 to 5.5 | V |
| Digital I/O Voltage1 | WAKE, EN | -0.3 to 40 | V |
| Digital I/O Voltage2 | CSB, SCLK, SI, PWMIN, TXD, TEST | -0.3 to 5.5 | V |
| Digital Output Voltage | DIAG, FG, SO, RXD | -0.3 to 40 | V |
| LIN Bus Voltage | LIN_PWMIN Voltage differential between Pins are 60 V or less | -40 to 40 | V |
| RF Input Voltage | RF | -3 to 3.6 | V |
| RFSENS Input Voltage | RFSENS | -0.3 to 1.0 | V |
| TH Input Voltage | TH | -0.3 to 3.6 | V |
| Voltage Tolerance | UOUT, VOUT, WOUT, COM | -3 to 40 | V |
| High-side Output | UH, VH, WH | -3 to 40 | V |
| Low-side Output | UL, VL, WL | -3 to 16 | V |
| Low-side Source Output Voltage | SUL, SVL, SWL | -3 to 3.6 | V |
| Voltage between HS Gate and Phase | UH-UOUT, VH-VOUT, WH-WOUT | -0.3 to 40 | V |
| Voltage between LS Gate and Source | UL-SUL, VL-SVL, WL-SWL | -0.3 to 16 | V |
| Output Current | UH, VH, WH, UL, VL, WL pulsed (duty 5%) | 50 400 | mA |
| Open Drain Output Current | DIAG, FG, SO, RXD | 10 | mA |
| Thermal Resistance ($R_{\theta JA}$) | With Board (Note 1) | 47 | °C/W |
| ESD Human Body Model | AEC Q100-002 | 2 | kV |
| ESD Charged Device Model | AEC Q100-011 | 750 | V |
| Storage Temperature | | -55 to 150 | °C |
| Junction Temperature | | -40 to 150 | °C |
| | (Note 2) | 150 to 175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 76.2 × 114.3 × 1.6 mm, glass epoxy board.

2. Operation outside the Operating Junction temperature is not guaranteed. Operation above 150°C should not be considered without a written agreement from **onsemi** Engineering staff.

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ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from -40°C to 150°C , for supply Voltage $6.0\text{ V} \leq \text{VS} \leq 20\text{ V}$. Typical values at 25°C and $\text{VS} = 12\text{ V}$ unless specified otherwise. (Note 4)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|----------|--|-----|-----|-----|--------------------|
| Supply-voltage Range | VS | | 6 | 12 | 20 | V |
| | | Device fully functional | 5.5 | | 20 | V |
| | | Full logic functionality, driver stage off | 4.5 | | 40 | V |
| Supply Current Into VS | I_{s1} | V3RO = V3RI | | 15 | 25 | mA |
| | I_{s2} | Sleep Mode | | 40 | 80 | μA |
| Operational Junction Temperature | Topj | | -40 | | 150 | $^{\circ}\text{C}$ |

OUTPUT BLOCK (UH, VH, WH, UL, VL, WL)

| | | | | | | |
|----------------------------------|---------|---------------------------------|--|----|----|----------|
| Low-side Output On-resistance 1 | RON(L1) | "L" level $I_o = 10\text{ mA}$ | | 6 | 15 | Ω |
| Low-side Output On-resistance 2 | RON(L2) | "H" level $I_o = -10\text{ mA}$ | | 12 | 22 | Ω |
| High-side Output On-resistance 1 | RON(H1) | "L" level $I_o = 10\text{ mA}$ | | 6 | 15 | Ω |
| High-side Output On-resistance 2 | RON(H2) | "H" level $I_o = -10\text{ mA}$ | | 12 | 22 | Ω |

DRIVE OUTPUT BLOCK (PWM BLOCK)

| | | | | | | |
|----------------------------------|------------------------|--|------|------|------|-----|
| Drive Output PWM Frequency | fPWMO | PWMF = 0 Low frequency mode | 18.5 | 19.5 | 20.5 | kHz |
| Output PWM Duty Cycle Resolution | $\Delta\text{PWMDUTY}$ | PWMF = 0 Low frequency mode (Note 5) | | | 0.2 | % |

3V CONSTANT VOLTAGE OUTPUT

| | | | | | | |
|--------------------|-----------------------|---------------------------------------|-------|-----|-------|----|
| Output Voltage | V3RO | | 3.135 | 3.3 | 3.465 | V |
| Voltage Regulation | ΔV3R1 | VS = 6.0 to 20 V | | | 50 | mV |
| Load Regulation | ΔV3REG2 | $I_o = 5\text{ mA}$ to 25 mA | | | 50 | mV |
| Current Limit | IV3RO | Not for external loads > 5 mA | 50 | | | mA |

VCC 5 V CONSTANT VOLTAGE OUTPUT

| | | | | | | |
|--------------------|----------------------|---------------------------------------|------|------|------|----|
| Output Voltage | VC5RO | VS = 6.0 to 20 V | 4.75 | 5.00 | 5.25 | V |
| Voltage Regulation | ΔVC5R1 | VS = 6.0 to 20 V | | | 50 | mV |
| Load Regulation | ΔVC5R2 | $I_o = 5\text{ mA}$ to 25 mA | | | 50 | mV |
| Current Limit | IVCC5V | | 50 | | | mA |

VCC 3 V CONSTANT VOLTAGE OUTPUT

| | | | | | | |
|--------------------|----------------------|---------------------------------------|-------|-----|-------|----|
| Output Voltage | VC3RO | | 3.135 | 3.3 | 3.465 | V |
| Voltage Regulation | ΔVC3R1 | VS = 6.0 to 20 V | | | 50 | mV |
| Load Regulation | ΔVC3R2 | $I_o = 5\text{ mA}$ to 25 mA | | | 50 | mV |
| Current Limit | IVCC3V3 | | 50 | | | mA |

LOW-SIDE GATE VOLTAGE OUTPUT (VGL PIN)

| | | | | | | |
|--------------------------|-------|--|------|------|------|---|
| Low-side Output Voltage1 | VGLH1 | $6.0 < \text{VS} \leq 8.0\text{ V}$ $I_o = -10\text{ mA}$ | 8.0 | 12.0 | 14.0 | V |
| Low-side Output Voltage2 | VGLH2 | $8.0 < \text{VS} \leq 20\text{ V}$ $I_o = -10\text{ mA}$ | 10.0 | 12.0 | 14.0 | V |

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ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from -40°C to 150°C , for supply Voltage $6.0\text{ V} \leq \text{VS} \leq 20\text{ V}$. Typical values at 25°C and $\text{VS} = 12\text{ V}$ unless specified otherwise. (Note 4)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
|-----------|--------|-----------|-----|-----|-----|------|

HIGH-SIDE OUTPUT VOLTAGE (CHP PIN)

| | | | | | | |
|---|-------|--|------------|-------------|-------------|-----|
| Internal Charge Pump Oscillator Frequency | FCP | SSCG = 0 | 49.6 | 52.1 | 54.6 | kHz |
| Boost Voltage1 | VGHH1 | $6.0 < \text{VS} \leq 8.0\text{ V}$ $I_o = -10\text{ mA}$ | VS +6.0 | VS +12.0 | VS +14.0 | V |
| Boost Voltage2 | VGHH2 | $8.0 < \text{VS} \leq 20\text{ V}$ $I_o = -10\text{ mA}$ | VS +9.0 | VS +12.0 | VS +14.0 | V |

PWMIN INPUT PIN IN LOW FREQUENCY MODE

| | | | | | | |
|---------------------------|---------|--|-----|-----|------|----|
| Input PWM Frequency Range | fLPWM | | 5.3 | | 1000 | Hz |
| PWM Signal Timeout | TLPWMIN | | | 210 | 220 | ms |

PWMIN INPUT PIN IN HIGH FREQUENCY MODE

| | | | | | | |
|---------------------------|-------|--|---|--|------|-----|
| Input PWM Frequency Range | fHPWM | | 0 | | 18.5 | kHz |
|---------------------------|-------|--|---|--|------|-----|

DIGITAL INPUT PIN (CSB, TXD)

| | | | | | | |
|--------------------------|--------|--|----------------------|------|----------------------|------------|
| High-level Input Voltage | VIH1 | | $0.8 \times V_{3RO}$ | | | V |
| Low-level Input Voltage | VIL1 | | | | $0.2 \times V_{3RO}$ | V |
| Input Hysteresis Voltage | VIHYS1 | | 0.1 | 0.35 | $0.6 \times V_{3RO}$ | V |
| Pull-up Resistance | RDVI1 | | 15 | 30 | 60 | k Ω |

DIGITAL INPUT PIN (SCLK, SI, PWMIN, TEST)

| | | | | | | |
|--------------------------|--------|--|----------------------|------|----------------------|------------|
| High-level Input Voltage | VIH2 | | $0.8 \times V_{3RO}$ | | | V |
| Low-level Input Voltage | VIL2 | | | | $0.2 \times V_{3RO}$ | V |
| Input Hysteresis Voltage | VIHYS2 | | 0.1 | 0.35 | $0.6 \times V_{3RO}$ | V |
| Pull-down Resistance | RDVI2 | | 50 | 100 | 200 | k Ω |

WAKE INPUT PIN

| | | | | | | |
|-------------------------------|-------|--|-----|-----|-----|------------|
| High-level Input Voltage | VIH3 | | 2.5 | | | V |
| Low-level Input Voltage | VIL3 | | | | 0.6 | V |
| Internal Pull-down Resistance | RDVI3 | | 50 | 100 | 200 | k Ω |

EN INPUT PIN

| | | | | | | |
|--------------------------|--------|--|----------------------|------|----------------------|------------|
| High-level Input Voltage | VIH4 | | $0.8 \times V_{3RO}$ | | | V |
| Low-level Input Voltage | VIL4 | | | | $0.2 \times V_{3RO}$ | V |
| Input Hysteresis Voltage | VIHYS4 | | 0.1 | 0.35 | $0.6 \times V_{3RO}$ | V |
| Pull-down Resistance | RDVI4 | | 50 | 100 | 200 | k Ω |

DIGITAL OUTPUT PIN (SO, FG, DIAG, RXD)

| | | | | | | |
|------------------------|-------|-------------------------------------|--|--|-----|---------------|
| Output Voltage | VOL | $I_o = 1\text{ mA}$ pull-up current | | | 0.2 | V |
| Output Leakage Current | ILOLK | | | | 10 | μA |

CURRENT LIMIT/OVERCURRENT PROTECTION (RF, RFSENS)

| | | | | | | |
|---|------|-------------------------------|-----|-----|-----|----|
| Current Limit Voltage | VRF1 | Voltage between RF and RFSENS | 90 | 100 | 110 | mV |
| Overcurrent Detection Voltage Threshold | VRF2 | Voltage between RF and RFSENS | 180 | 200 | 220 | mV |

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ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from -40°C to 150°C , for supply Voltage $6.0\text{ V} \leq \text{VS} \leq 20\text{ V}$. Typical values at 25°C and $\text{VS} = 12\text{ V}$ unless specified otherwise. (Note 4)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
|-----------|--------|-----------|-----|-----|-----|------|

EXTERNAL THERMAL PROTECTION (TH)

| | | | | | | |
|---------------------------|------------------------------|--|-------|------------------------------|-------|---|
| Threshold Voltage Falling | VTH0 VTH1 VTH2 VTH3 | THTH[1:0] = 00 THTH[1:0] = 01 THTH[1:0] = 10 THTH[1:0] = 11 | -10% | 0.35 0.30 0.25 0.20 | +10% | V |
| Hysteresis Range | VTHHYS | | 0.025 | 0.05 | 0.075 | V |

THERMAL PROTECTION

| | | | | | | |
|---|----------------|---|------------|----|--|--------------------|
| Thermal Warning Temperature | TTW0 TTW1 | Junction Temperature (Note 5) TSTS = 0 TSTS = 1 | 125 150 | | | $^{\circ}\text{C}$ |
| Thermal Warning Temperature Hysteresis | TTWHYS | Junction Temperature (Note 5) | | 25 | | $^{\circ}\text{C}$ |
| Thermal Shutdown Temperature | TTSD0 TTSD1 | Junction Temperature (Note 5) TSTS = 0 TSTS = 1 | 150 175 | | | $^{\circ}\text{C}$ |
| Thermal Shutdown Temperature Hysteresis | TTSDHYS | Junction Temperature (Note 5) | | 25 | | $^{\circ}\text{C}$ |

VOLTAGE MONITORING (VS, CHP, VGL, VCC)

| | | | | | | |
|--|----------|-------------------------------------|--------|------|--------|---|
| VS Undervoltage Detection | VSLV | | 4.8 | | 5.1 | V |
| VS Undervoltage Detection Hysteresis | VSLVHYS | | 0.1 | 0.25 | 0.4 | V |
| VS Overvoltage Detection | VSHV | | 20 | | 24 | V |
| Overvoltage Detection Hysteresis | VSHVHYS | | 0.5 | 1.0 | 1.5 | V |
| CHP Undervoltage Detection | CHPLV | | VS+4.5 | | VS+5.5 | V |
| CHP Undervoltage Detection Hysteresis | CHPLVHYS | | 0.2 | 0.4 | 0.7 | V |
| VGL Undervoltage detection | VGLLV | | 4.5 | | 5.5 | V |
| VGL Undervoltage Detection Hysteresis | VGLLVHYS | | 0.2 | 0.4 | 0.7 | V |
| VCC3.3 Undervoltage Detection | VCLV3 | REGSEL = 0, VCEN = 1, VCLVPO = 0 | 2.3 | | 2.7 | V |
| VCC3.3 Undervoltage Detection hysteresis | VCLVHYS3 | REGSEL = 0, VCLVPO = 0 | 0.1 | 0.25 | 0.4 | V |
| VCC5.0 Undervoltage Detection | VCLV5 | REGSEL = 1, VCEN = 1, VCLVPO = 0 | 3.8 | | 4.2 | V |
| VCC5.0 Undervoltage Detection Hysteresis | VCLVHYS5 | REGSEL = 1, VCLVPO = 0 | 0.1 | 0.25 | 0.4 | V |

LIN_PWMIN PIN (LIN TRANSMITTER)

| | | | | | | |
|---|--------------|---|----|----|-----|---------------|
| LIN Output Current Bus in Dominant State | Ibus_pas_dom | Driver OFF Vbus = 0 V, VS = 7 V & 18 V | -1 | | | mA |
| LIN Output Current Bus in Recessive State | Ibus_pas_rec | Driver OFF Vbus = VS, VS = 7 V & 18 V | | | 20 | μA |
| Short-circuit Current Limitation | Ibus_lim | Driver ON Vbus = VS, VS = 7 V & 18 V | 40 | | 200 | mA |
| Internal Pull-up Resistance | Rslave | VS = 7 V & 18 V | 20 | 30 | 47 | k Ω |

LV8907UW

ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from -40°C to 150°C , for supply Voltage $6.0\text{ V} \leq \text{VS} \leq 20\text{ V}$. Typical values at 25°C and $\text{VS} = 12\text{ V}$ unless specified otherwise. (Note 4)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
|-----------|--------|-----------|-----|-----|-----|------|

LIN_PWMIN PIN (LIN RECEIVER & PWMIN)

| | | | | | | |
|--------------------------|---------|-----------------|---------|--|--------|---|
| High Level Input Voltage | Vbusdom | VS = 7 V & 18 V | 0.6×VS | | VS | V |
| Low Level Input Voltage | Vbusrec | VS = 7 V & 18 V | 0 | | 0.4×VS | V |
| Input Hysteresis Voltage | Vbushys | VS = 7 V & 18 V | 0.05×VS | | 0.2×VS | V |

AC CHARACTERISTICS LIN_PWMIN PIN

| | | | | | | |
|---|----------------|--|-------|--|-------|----|
| Duty Cycle 1 | D1 | Threcmax = 0.744VS Thdommax = 0.581VS VS = 7.0 V & 18 V, tbit = 50 μs D1 = tBusrecmin / (2×tbit) | 0.396 | | 0.5 | |
| Duty Cycle 2 | D2 | Threcmin = 0.422VS Thdommin = 0.284VS VS = 7.6 V & 18 V, tbit = 50 μs D1 = tBusrecmax / (2×tbit) | 0.5 | | 0.581 | |
| Duty Cycle 3 | D3 | Threcmax = 0.778VS Thdommax = 0.616VS VS = 7.0 V & 18 V, tbit = 96 μs D1 = tBusrecmin / (2×tbit) | 0.417 | | 0.5 | |
| Duty Cycle 4 | D4 | Threcmin = 0.389VS Thdommin = 0.251VS VS = 7.6 V & 18 V, tbit = 96 μs D1 = tBusrecmax / (2×tbit) | 0.5 | | 0.59 | |
| Propagation Delay Bus Recessive to RXD = High | Trx_pdr | VS = 7 V & 18 V | | | 6 | μs |
| Propagation Delay Bus Dominant to RXD = Low | Trx_pdf | VS = 7 V & 18 V | | | 6 | μs |
| Symmetry of Receiver Propagation Delay | Trx_sym | trx_pdr–Trxpdf | –2 | | 2 | μs |
| Normal Slope Rise Time 12 | T_rise_norm 12 | VS = 12 V, LINSLP = 0 L1, L2 (Note 6) | | | 22.5 | μs |
| Normal Slope Fall Time 12 | T_fall_norm 12 | VS = 12 V, LINSLP = 0 L1, L2 (Note 6) | | | 22.5 | μs |
| Symmetry of Normal Slope 12 | T_sym_norm 12 | VS = 12 V, LINSLP = 0 L1, L2 (Note 6) | –4 | | 4 | μs |
| Normal Slope Rise Time 3 | T_rise_norm 3 | VS = 12 V, LINSLP = 0, L3 (Note 6) | | | 27 | μs |
| Normal Slope Fall Time 3 | T_fall_norm 3 | VS = 12 V, LINSLP = 0, L3 (Note 6) | | | 27 | μs |
| Symmetry of Normal Slope 3 | T_sym_norm 3 | VS = 12 V, LINSLP = 0, L3 (Note 6) | –5 | | 5 | μs |
| Low Slope Rise Time | T_rise_low | VS = 12 V, LINSLP = 0, L3 (Note 6) | | | 62 | μs |
| Low Slope Fall Time | T_fall_low | VS = 12 V, LINSLP = 0, L3 (Note 6) | | | 62 | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not tested in production. Guaranteed by design.

4. Load conditions Rbus/Cbus: L1 = 1 kΩ / 1 nF, L2 = 660 Ω / 6.8 nF, L3 = 500 Ω / 10 nF Typical Operating Conditions.

DETAILED FUNCTIONAL DESCRIPTION

The LV8907 integrates full sensorless brushless DC motor commutation and Proportional/Integral (PI) speed control. A robust startup algorithm combined with OTP registers for important system parameters make this IC a solution of choice for many BLDC applications which need to turn a motor in one direction only such as pumps, fans, etc. No detailed BLDC commutation knowledge is necessary.

Building a BLDC application with the LV8907 is even simpler than building a DC motor. Only a PWM pulse train is necessary to control the motor – either directly or via speed control. Switch-only applications are also possible. Speed and error information can be fed back to the control unit via FG and DIAG outputs.

If more complex operation and flexibility are required the LV8907 can be combined with a small microcontroller. The LV8907 implements motor commutation and includes all necessary support circuitry for the microcontroller such as:

- 5 V / 3.3 V Power supply
- Integrated watchdog timer

- LIN Transceiver
- External Temperature Sensor

In case of system errors such as a missing control signal, or a watchdog error, the LV8907 includes auto-run settings. If one of those errors occur and connection to the microcontroller is lost, the motor can continue running at a predefined fixed duty cycle of 25%, 50%, 75% or 100%.

Motor Commutation

Motor position is detected using the BEMF of the un-driven phase of a rotating three-phase motor relative to its neutral point connected to COM. Once an adequate BEMF level has been detected voltages applied via PWM to the other two phases of the motor maintain rotation. The digital equivalent of the BEMF signal appears at FG.

Two different PWM patterns can be selected via register MRCONF12 to match motors with trapezoidal or sinusoidal BEMF.

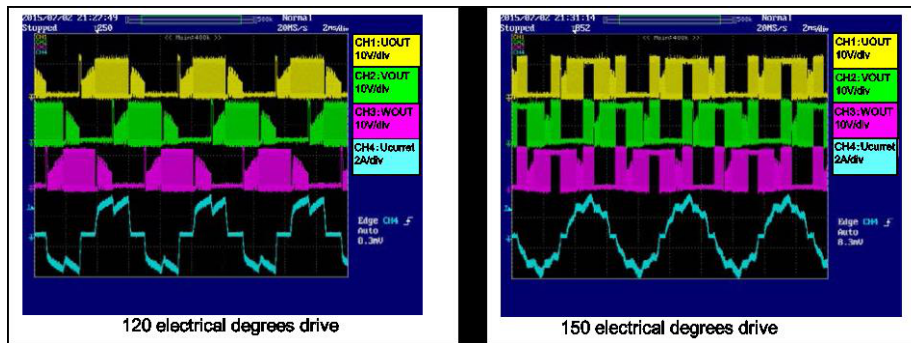


Figure 7. Trapezoidal vs. Sinusoidal Drive @ 50% Duty Cycle
(CH1 = U Phase Voltage, CH2 = V Phase Voltage, CH3 = W Phase Voltage, CH4 = U Phase Current)

Figure 7 shows a comparison of a motor driven with normal trapezoidal commutation (left) vs. one driven with sinusoidal drive. With sinusoidal drive each phase is driven 150 electrical degrees with soft transitioning. This results in sinusoidal drive current with lower total harmonic distortion, reducing both torque ripple and noise. Trapezoidal drive results in a higher voltage across the motor phases and may be preferable for high torque and high speed operation.

Maximum Motor Speed

The maximum physical motor speed of the application is limited by the internal clock to approximately 48000 electrical RPM. If this is exceeded the LV8907 coasts the motor until BEMF detection and drive can resume.

Commutation Angle Adjustment

In trapezoidal commutation mode it is possible to advance the commutation angle by up to 28 electrical degrees as defined in register LASET. Early commutation adjusts the

rotor magnetic field positioning and allows for higher motor speeds at the expense of efficiency. Advancing commutation can be done dynamically by a companion microcontroller.

Motor Startup

BEMF is used for rotor position sensing but for BEMF generation the motor has to be rotating. A stopped motor will initially be driven open-loop until BEMF can be detected.

Open-loop operation is motor parameter dependent. The most critical parameters depend on load and motor inertia. They are initial commutation frequency and PWM duty cycle (which affects motor flux density).

In the LV8907, the initial commutation frequency is programmed with register STOSC. Flux density is regulated by limiting startup current with a current ramp. During this ramp the current limit is increased in 16 steps from 0 to the maximum current defined by the external shunt. The ramp time from 105 ms to 6.72 s is defined in register SSTT.

Register SSTEN allows to disable the current ramp if necessary.

Fixed motor speed will be applied until either a valid BEMF has been detected in all three phases or the startup timer expires.

Motor Lock

This timer begins after the end of the current ramp and can be programmed from 420 ms to 6.72 s in register CPTM. If the timer expires a locked rotor error is flagged. In automatic retry mode, the LV8907 will restart after standby mode for time of eight times of CPTM.

Spin-up of Rotating Motors

The LV8907 can perform freewheeling detection before applying the open-loop spin-up algorithm described above. If the motor is already turning in the right direction the IC will continue with closed-loop commutation. If the motor is turning in the wrong direction, the IC will wait for the motor to stop and then perform open-loop startup.

There are two scenarios where this behavior might not be desirable:

1. Fast Startup is required
Freewheeling detection takes up to one electrical revolution of the motor, which may be unacceptable for some applications. In this case freewheeling detection can be disabled by setting FRREN. See section “Fast Startup”
2. Wind-milling backwards
Should the motor be driven by some external force as it is freewheeling in the wrong direction the LV8907 will potentially wait forever. Should startup under these conditions be required, freewheeling detection must be disabled as well

Chip Activation, Shutdown and System States

After power up of VS and WAKE above 2.5 V the LV8907 wakes up. Standby mode is entered after VS has exceeded 5.5 V (min.).

A high level on WAKE > 2.5 V (max.) activates the IC from sleep mode which enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and after 32 counts of the system clock (3.2 μs typical) releases the internal digital reset which simultaneously starts the external regulator VCC and the charge pump, and loads the system register contents from OTP into the internal registers. During the entire wake-up sequence of 8 ms (typ.) DIAG is masked for charge pump and VCC undervoltage. After wake-up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.

A high on EN takes the LV8907 from Standby to Normal mode. Normal mode allows motor control and SPI access is limited. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.

The IC is shut down by taking WAKE below 0.6 V (min.). WAKE has priority over the state of EN, if EN hold functionality is desired; it needs to be implemented with an external diode from EN to WAKE.

System States

LV8907 has three operating modes. The operating modes are controlled by WAKE and EN.

Sleep Mode:

Sleep mode is a power saving mode. All circuits are powered down, charge pump is inactive and the SPI port is unusable. Activating WAKE allows the transition from the sleep mode to either Standby or Normal mode.

Standby Mode:

In Standby mode the OTP content has been transferred into the Main-register. In this mode all outputs are turned off. Any internal writable register that is not locked can be configured by SPI interface.

Normal Mode:

In normal mode, outputs can be controlled and all blocks are active. All registers can be read through the SPI interface.

| Mode | WAKE | EN | Internal bias | Logic | VCC | Charge pump | Drivers |
|---------|------|----|---------------|--------|---------|-------------|---------|
| Sleep | L | × | Disable | Reset | Disable | Disable | High-Z |
| Standby | H | L | Enable | Active | Enable | Enable | Low |
| Normal | H | H | Enable | Active | Enable | Enable | Enable |

Supply Voltage Transients

The LV8907 is well suited to operate during typical automotive transients. It is fully functional during start-stop transients, as it maintains all specified parameters for supply voltages from 6 V < VS < 20 V. If the supply voltage falls below 5 V, for example during cold-cranking, undervoltage error is flagged, but digital functionality is maintained until the internal regulator falls below its undervoltage lockout level of 2.2 V. The VCC regulator must be configured for 3.3 V if low transient operation is desired.

If overvoltage protection is enabled in MRCONF10 an overvoltage error is indicated if the supply rises beyond 20 V(min). In both under- and overvoltage error modes, the power stage drivers UH, VH, WH and UL, VL, and WL go low, turning the external power stage high impedance and letting the motor freewheel. The LV8907 will re-engage the motor after conditions have returned to normal.

System Power Supplies

Three power supplies are integrated into the LV8907:

- An internal 3.3 V regulator provides power to the digital and interface section
- The VCC regulator can be configured to provide 5 V or 3.3 V to an external processor and other loads
- A dual stage charge pump allows 100% duty cycle operation and maintains full enhancement to the power stage at low input voltages

Internal Regulator V3RO, V3RI

The internal regulator is supplied from VS, provides 3.3 V at V3RO. V3RI is connected to the power supply inputs of the control and logic circuit blocks. V3RO and V3RI need to be connected externally and bypassed to the GND plane for stability. V3RO must not be used for external loads.

VCC Regulator

The VCC regulator may power external loads up to 50 mA(max). VCC becomes active during Standby mode and can be configured via register REGSEL to provide 5 V or 3.3 V. Undervoltage error is flagged if the output voltage

drops below 4.2 V in 5 V operation, or 2.7 V in 3.3 V operation.

The VCC regulator can be enabled or disabled with register VCEN.

Charge Pump Circuit for CHP and VGL

LV8907 has an integrated charge pump circuit for low-side and high-side predriver supply. Low-side drive voltage at VGL is 12 V(typ.) and high-side drive voltage at CHP is VS + 12 V(typ.). For functionality see Figure 8.

Undervoltage protection for the low-side drivers activates if VGL falls below 4.8 V in which case the output FET's will be turned off and VGL undervoltage error is flagged in register MRDIAG. Overvoltage protection for the high-side drivers activates if VS becomes greater than 20 V(min). In that event the driver stage is disabled, overvoltage error is flagged in register MRDIAG, and both VGL and CHP are discharged to prevent output circuit destruction.

The charge pump circuit operates nominally at 52.1 kHz. A SSCG function is provided to add a spread-spectrum component for EMI reduction.

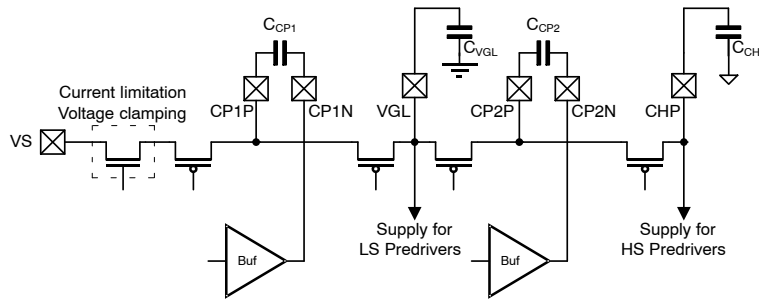


Figure 8. Charge Pump Circuit

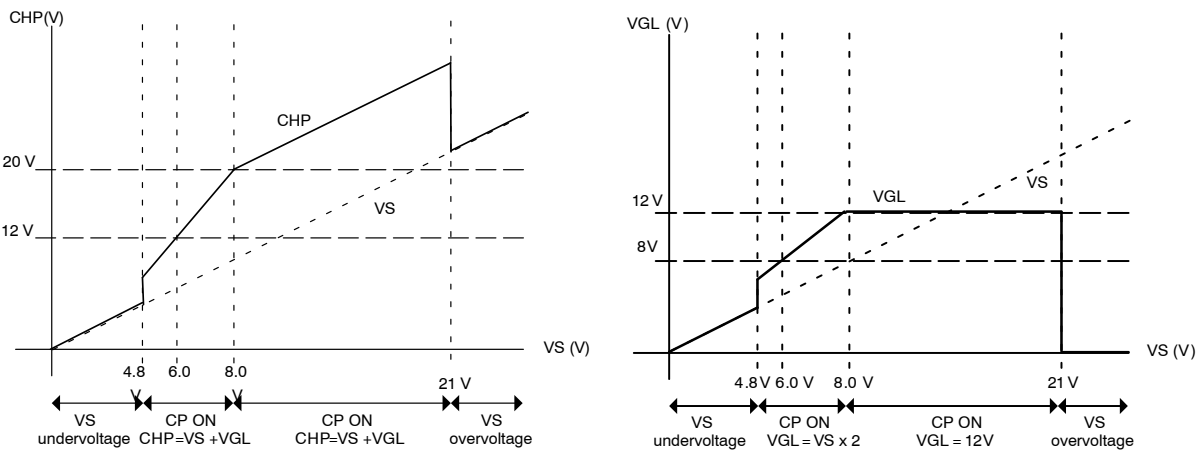


Figure 9. High-side and Low-side Gate Voltages

INPUT PWM and SPEED CONTROL

The LV8907 provides three speed control methods through the input PWM signal:

1. Direct PWM pass-through
2. Indirect PWM translation
3. Closed-loop speed control

Direct PWM Pass-through

The input PWM frequency and duty cycle are directly fed to the power stage. This allows a companion microprocessor direct control over duty cycle and output frequency up to 18.5 kHz. No input frequency detection takes place in this mode, so 100% and 0% duty cycle can be applied.

NOTE: It is important not to exceed 18.5 kHz to maintain reliable BEMF detection.

When the register bit PWMF is set 1, this control method is selected.

Indirect PWM Translation

This is the preferred mode for stand-alone operation. In this mode the input PWM signal is compared against minimum and maximum PWM frequency thresholds to allow for more robust operation. Frequencies above 1 kHz are ignored and frequencies below 5.3 Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The duty cycle of the PWM input signal is measured with a resolution of 9 bits. There is an inherent delay to detect and utilize this duty cycle information, the motor will start up after the delay time (max. 1/8th of the PWM input signal period).

If faster startup is necessary, see section “Fast Startup” below. If no frequency is detected after 210 ms (typ.) the PWMPO flag is set in system warning register MRDIAG1. Even without PWM input the LV8907 can run as described below in section “Fast Startup”.

If a valid frequency was detected, the LV8907 evaluates the input duty cycle and translates it into an output duty cycle as shown in Figure 10. The output PWM frequency is fixed to 19.5 kHz (typ.).

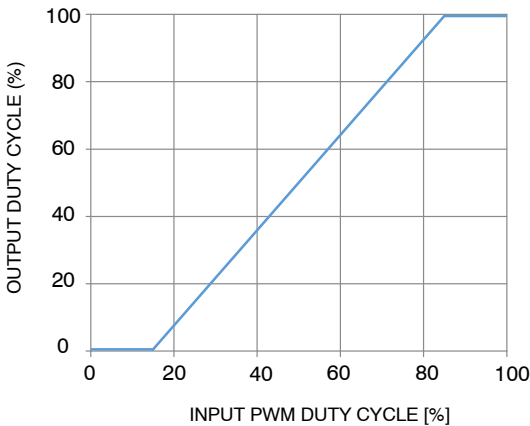


Figure 10. Duty Cycle Translation

Input duty cycles lower than 15% are considered a motor-off command and will also reset the error registers. Input to output duty cycle translation is described by the following formula:

$$d_{OUT} = \begin{cases} 0 & , & 0 < d_{IN} < 15 \\ \frac{10}{7}(d_{IN} - 15) & , & 15 < d_{IN} < 85 \\ 100 & , & 85 < d_{IN} < 100 \end{cases} \quad (\text{eq. 1})$$

Closed-Loop Speed Control

For stand-alone operation, the LV8907 offers a PI controller for motor speed which is activated by clearing bit SCEN. Frequencies above 1 kHz are ignored and frequencies below 5.3 Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The output PWM frequency is fixed to 19.5 kHz (typ.).

LV8907 provides nine target speed values which are stored in registers FGT0 to FGT8. In speed control mode the input PWM duty cycle is encoded as a selector for these registers as shown in Figure 11. A duty cycle hysteresis allows for stable register selection.

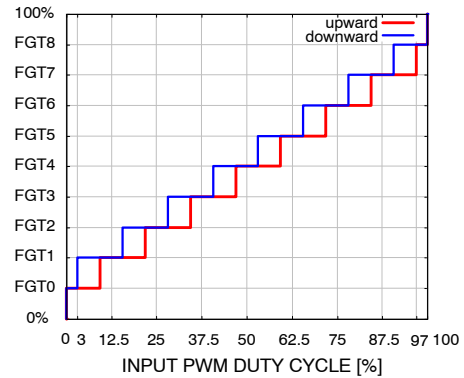


Figure 11. Target Speed Register Selection by Input PWM Duty Cycle

A duty cycle of 50% with a variation band of 6.25% for example will select the motor speed value stored in the 4th speed register FGT4. This allows for non-linear speed curves. When using a companion microcontroller it is possible to write to the speed register in real time during operation to achieve finer RPM resolution. For more information see section “Target speed setting”.

The Control Algorithm

The LV8907 controls the motor speed by comparing the selected target speed to the actual motor speed and incorporating a PI controller with configurable gains for the P and I components which are stored in register MRSPCT0 and MRSPCT1 respectively.

Ramping of Speed Control Values

While tight control is required for optimal speed tracking, it may be undesirable during large input changes as it may lead to sudden supply loading, increasing noise and motor wear. To limit the slope of the control signal, register STEPSEL imposes a ramp on an input step to slew the speed response of the motor.

Decreasing motor speed too fast results in energy recuperation back into the system. To limit overvoltage during energy recuperation, the variable DWNSET allows either

1. to distribute the recuperation energy over a longer period of time or
2. to prevent energy recuperation entirely

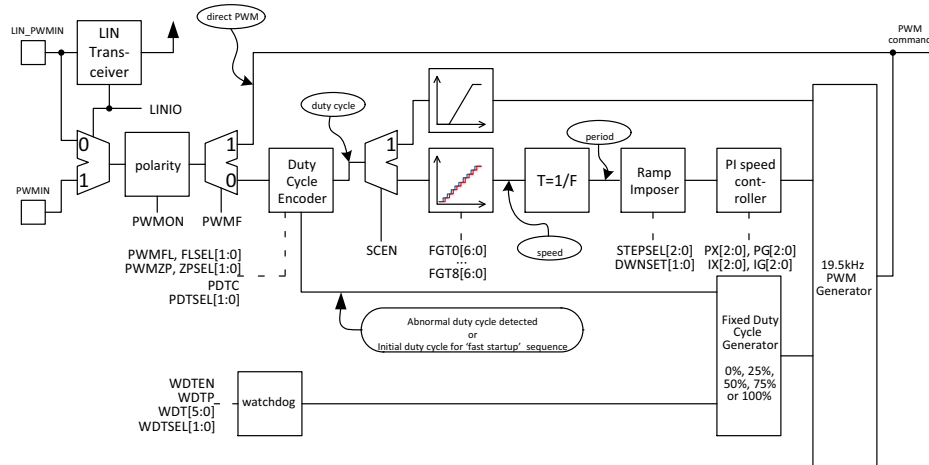


Figure 12. PWM Command Flow and Related Registers

Fast Startup

It may be desirable to have the motor start immediately after EN goes high and not wait for PWM input duty cycle evaluation. Two register settings enable motor operation during this evaluation time: bit PDTC determines if the motor should be running during this time at all, and PDTSEL selects a motor duty cycle of 25, 50, 75 or 100%. This is used as the initial value of the duty cycle command for the closed-loop speed control mode. To guarantee smooth transition from fast startup to PWM operation it is important to apply a comparable external PWM duty cycle at startup. Also make sure that FRREN = 1 to improve startup speed.

Abnormal Duty Cycle Operation (100% or 0%)

For normal duty cycle controlled operation the PWM signal is expected to have a frequency between 5.3 Hz and 1kHz. If no frequency is detected, the LV8907 will flag PWMPO error and enter 0% or 100% duty cycle mode depending on the level of the PWM signal (all low or all high). Operation during this mode can be selected to be either no motor operation, or motor operation at a fixed motor duty cycle of 25, 50, 75 or 100% as defined by the variables PWMFL and FLSEL or PWMZP and ZPSEL. These PWM values do not enter into the speed control loop.

Speed Feedback FG

The motor speed is shown at open drain output FG where the transitions are direct representations of the BEMF signal transitions on the motor. The relationship between motor rotation and FG pulses is defined in register FGOF.

Fault Output DIAG

A low on open drain output DIAG indicates a system fault and a shutdown of the driver stage. Per default all system faults self-recover when the fault condition is removed. For some potentially destructive faults such as overcurrent, FET short-circuit and locked rotor conditions, it is possible to latch the fault condition. For more information on system diagnostics see section “System Errors and Warnings”.

LIN Transceiver

LIN_PWMIN can be used as a local interconnect network (LIN) 2.2 A compatible LIN transceiver by setting the LINIO bit and connecting an external microcontroller to RXD and TXD. The microcontroller must handle the LIN communication and control the LV8907 through EN, PWMIN and the SPI interface. The LIN transceiver can be switched to low slope mode to reduce electromagnetic emissions by setting LINSLP = 1. For more information on the automotive LIN bus protocol consult publicly available documentation.

Gate Drive Circuit

The gate drive circuit of the LV8907 includes 3 half-bridge drivers which control external N-channel FETs for the motor phases U, V and W. The high-side drivers UH, VH, WH switch their gate connection either to CHP or the respective phase connection UOUT, VOUT and WOUT. The low-side drivers are switched from VGL to the corresponding source connection SUL, SVL, SWL. Both high and low-side switches are not current controlled. Slope control has to be implemented with external components.

Current shoot through protection of the bridge drivers is implemented by a dead time counter that delays the turning-on of the complementary switch. The dead time can be programmed from $100\text{ns} < t_{\text{FDTI}} < 3.2 \mu\text{s}$ into 5 bit parameter FDTI.

To protect against external shorts the drain-source voltage of the active external Power FETs is monitored as well. 4 bit register FSCDL selects a short-circuit shutoff voltage $100 \text{ mV} < V_{\text{FSCLD}} < 1.6 \text{ V}$. To suppress false triggering during the rising edge of FET activation, a four bit masking time can be programmed in FSCDT.

Current Limit and Overcurrent Shutoff

An integrated current sense amplifier implements current limiting and overcurrent shutoff by measuring the motor phase current across a single shunt between RF and RFSENS.

Figure 13 shows a summary of the current limit and the overcurrent shutoff, and the descriptions for each function are in the following sections.

Cycle-by-cycle Current Limit

If the voltage between RF and RFSENS exceeds $V_{\text{RF1}} = 100 \text{ mV}(\text{typ.})$, the active bridge is turned off until the next PWM period. To suppress switching transients a current limit blanking time $0.1 \mu\text{s} < t_{\text{CLMASK}} < 1.6 \mu\text{s}$ can be programmed into register CLMASK.

During soft start this current limit is ramped from 0 to 100 mV in 16 steps during a programmable time $105 \text{ ms} < t_{\text{SSTT}} < 6.72 \text{ s}$ as defined in register SSTT.

Overcurrent Shutoff

If the bit OCPEN is set and the voltage between RF and RFSENS exceeds $V_{\text{RF2}} = 200 \text{ mV}(\text{typ.})$, the LV8907 goes into overcurrent shutoff and all gate drivers are driving low turning the power FETs high impedance. To suppress switching transients an overcurrent shutoff blanking time $0.2 \mu\text{s} < t_{\text{OCMASK}} < 3.2 \mu\text{s}$ can be programmed into register OCMASK.

| Current | Purpose | Flag | Sense point | Threshold | Turn-off | Recovery |
|----------------|-----------|------|--------------------|--------------|----------|----------------|
| Cycle-by-cycle | Limiter | None | Sense Resistor VRF | 100 mV | PWM FET | Next PWM cycle |
| Short to VS | Protector | OCPO | Sense Resistor VRF | 200 mV | All FET | 52.4 ms later |
| | | FSPO | FET VDS | configurable | | |
| Short to GND | Protector | FSPO | FET VDS | configurable | All FET | 52.4 ms later |

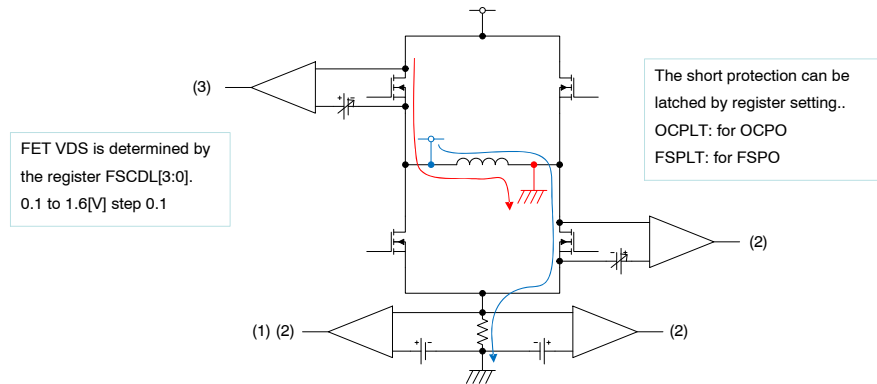


Figure 13. Current Limit vs. Overcurrent Shutoff

Temperature Sensing

The LV8907 measures internal die temperature and implements internal thermal warning and shutoff. It is also possible to protect external devices by monitoring the voltage at pin TH. Internal and external overtemperature can shut down the driver section.

Internal Overtemperature Measurement

A thermal warning is issued if the internal temperature of the device reaches approximately 25°C below the overtemperature shutoff level. The shutoff level is selected by bit TSTS as 150°C or $175^{\circ}\text{C}(\text{min})$.

External Overtemperature Shutoff

An analog comparator triggers external overtemperature error if the voltage at pin TH falls below the two bit programmable level $0.2 \text{ V} < V_{\text{THTH}} < 0.35 \text{ V}$ as defined by register THTH. For external temperature measurement connect a resistor between V3RO and TH and an NTC between TH and AGND. The programmed threshold voltage at V_{THTH} should be reached at the intended thermal shutdown temperature of the external component to be protected. During the overtemperature condition, the gate drivers are disabled and a flag, THPO in MRDIAG0 is set.

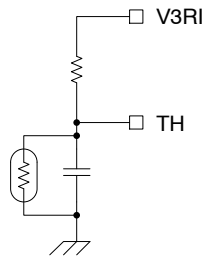


Figure 14. Example Circuit for External Temperature Sensing

Watchdog Operation

The LV8907 includes a watchdog timer to monitor a companion microcontroller and disable the motor if the microcontroller stops working properly. Bit WDTEN enables and disables the watchdog timer. Access to this bit can be blocked – see section “OTP Registers” for details. The enabled watchdog will issue an error whenever the watchdog time $1.64 \text{ ms} < t_{WDT} < 104.96 \text{ ms}$ expires. A write of 00h to register MRRST resets the watchdog timer.

A watchdog timeout can result in either a motor stop, or motor operation at four predefined duty cycles (25%, 50%, 75%, 100%) as defined by WDTP and WDTSEL. The duty cycle is directly applied to the power stage, not through the speed selection registers. The microprocessor is not re-set.

System Errors and Warnings

All system errors and most warnings cause a transition on DIAG. The polarity of this transition can be selected in bit DIAGSEL. The ability of stand-alone applications without microcontroller to react to errors and warnings is limited. For this case various auto-retry strategies are implemented.

If a companion microcontroller exists, more complex error handling is possible and DIAG should be connected to an interrupt input of the microcontroller. Errors that may cause serious damage such as short-circuit, overcurrent and locked rotor can be latched by enabling the corresponding latch bit in MRCONF10. In this case the LV8907 will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset
- EN low
- Low frequency PWM less than 15% duty cycle
- SPI write of FFh to MRRST

If bit DLTO is set ONLY latched errors will cause a transition of DIAG. To detect the other less serious errors and warnings, the diagnostic registers MRDIAG0/MRDIAG1 have to be read regularly via SPI access.

Table 1. ERROR REGISTER: MRDIAG0[7:0]

| Bit | Error | Description | Maskable | Latchable | Self Recovery when Latch Function Turned Off |
|-----|---------|--------------------|----------|-----------|---|
| 0 | OCPO | Overcurrent Error | × | × | After 52.4 ms (typ.) the motor will re-start |
| 1 | VSLVPO | VS Undervoltage | | | Motor is re-started when voltage recovers |
| 2 | VSOVPO | VS Overvoltage | × | | Motor is re-started when voltage recovers |
| 3 | CHPLVPO | CHP Undervoltage | | | Motor is re-started when voltage recovers |
| 4 | VGLLVPO | VGL Undervoltage | | | Motor is re-started when voltage recovers |
| 5 | FSPO | FET Short-circuit | × | × | After 52.4 ms (typ.) the motor will re-start |
| 6 | THPO | Thermal Protection | × | | Motor is re-started when temperature recovers |
| 7 | CPO | Locked Rotor | × | × | Wait 8 t_{CPTM} periods (see “Motor Lock”) |

5. See register MRCONF10 for error activation and masking and MRCONF11 for latching options.

Table 2. WARNING REGISTER: MRDIAG1[7:0]

| Bit | Warning | Description | DIAG | Blankable | Effect |
|-----|--------------|--------------------------|------|-----------|--|
| 0 | THWPO | Junction Temp. Warning | × | × | The IC has exceeded the warning temperature but stays in Normal operation |
| 1 | THSPO | Junction Overtemperature | × | | The IC has exceeded the shutoff temperature. Drivers are shut down during overtemperature |
| 2 | WDTPPO | Watchdog Timeout | × | × | Driver stage is shut off or continues with preselected duty cycle (25, 50, 75, 100%) |
| 3 | STUPO | Startup Operation | | | The motor is running open-loop |
| 4 | SPCO | Loss of Speed Lock | | | Target speed and actual speed are more than 6.25% different |
| 5 | Internal Use | | | | |
| 6 | VCLVPO | VCC Undervoltage | × | × | Driver stage off |
| 7 | PWMPO | PWM Input Fault | × | | No PWM signal detected. Driver stage is shut off or continues with preselected duty cycle (25, 50, 75, 100%) |

6. An “x” in column “DIAG Blank” means that it is possible to prevent a warning from triggering DIAG see register MRCONF10 for details.

SPI Interface

In the LV8907 the SPI interface is used to perform general communications for status reporting, control and programming.

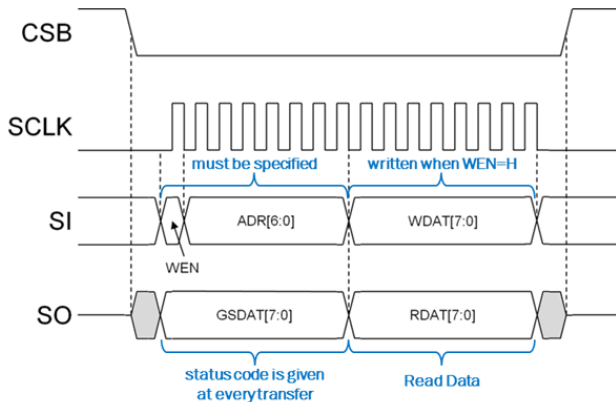


Figure 15. SPI Format

SPI communications with the LV8907 follows established industry standard practices including the use of WEN and start and stop bits as shown above. Data is transferred MSB first and both clock and data are transferred as ‘true’ data with the higher level indicating a logical 1 or true state. If WEN is LOW, the register data is transferred from LV8907 to the microcontroller. If WEN is HIGH, the register data is transferred from the microcontroller to the LV8907 register.

There are two items to be especially careful of with the general communication scheme:

1. Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable with the LV8907
2. It is important the system master uses the clock and data polarities and phases as shown above. Both the clock and data on some systems can be inverted for various reasons but must arrive at the LV8907 per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half of a bit time exists to eliminate transmission delay hazards

The first byte returned on all transactions is always the status register, GSDAT, and contains information such as the busy flag during programming operations.

GSDAT[7:0]

| Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 | |
|-------|-------|------|-------|-------|------|-----------|------|---------------------------------|
| ORBEN | STUPO | SACF | DIAGS | LATCH | OBSY | SMOD[1:0] | | |
| | | | | | | 0 | 0 | Sleep mode (MRACK[7:0] = FFh) |
| | | | | | | 0 | 1 | Device start up time |
| | | | | | | 1 | 0 | Standby mode |
| | | | | | | 1 | 1 | Normal mode (MRACK [7:0] = 55h) |
| 0 | × | × | 0 | 0 | 0 | × | × | Normal Operation |
| | | | | | 1 | | | OTP busy with read/write access |
| | | | | 1 | | | | Latched shutdown condition |
| | | | 1 | | | | | Failure Condition |
| | | 0 | | | | | | Last SPI access OK |
| | | 1 | | | | | | Last SPI access failed* |
| | 1 | | | | | | | Startup mode |
| 1 | | | | | | | | OTP integrity test mode |

The following SPI failures are detectable and reported collectively in GSDAT as general SPI failures:

- Any access to an address which are outside the defined address space
- The number of SCLK transitions is not 16 within one word transfer

- Any access to MRCONF, MRACS, ORCONF, ORACS while OBSY = 1 (during write operations)
- Write access to MRODL register while OBSY = 1 (during write operations)

LV8907UW

- Write access to any of the main registers after setting MSAENB = 1 (Implies MRxxxx registers are locked)
- Write access to any of the OTP registers after OSAENB = 1 (Implies ORxxxx registers are locked)
- Write access attempt to a read only or locked register
- SI signal changed at positive edge of SCLK (Incorrect data/sclk phase setup)

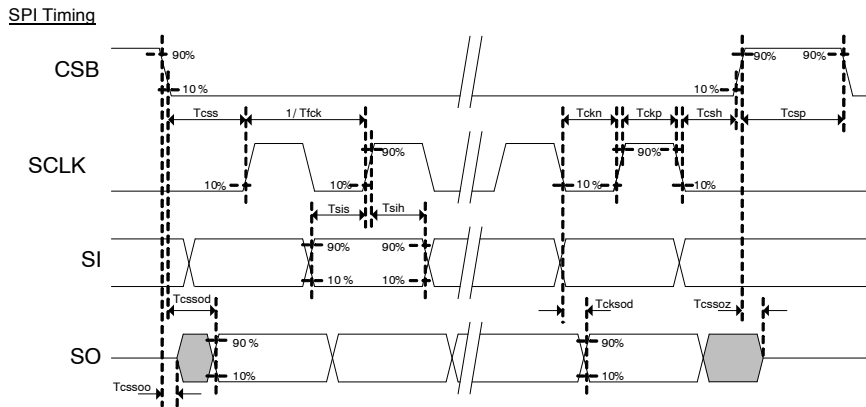


Figure 16. SPI Timing Chart

SPI TIMING $T_J = -40$ to 150°C , $V_S = 4.5$ to 20 V. Pull-up resistance of SO pin = 2.4 k Ω , Output load of SO pin = 30 pF.

| Symbol | Comment | Min | Typ | Max | Unit |
|--------|-----------------------------------|------|-----|-----|------|
| Tfck | SCLK clock frequency | | | 500 | kHz |
| Tckp | SCLK high pulse width | 950 | | | ns |
| Tckn | SCLK low pulse width | 950 | | | ns |
| Tcss | CSB setup time | 950 | | | ns |
| Tcsh | CSB hold time | 950 | | | ns |
| Tcsp | CSB high pulse width | 1900 | | | ns |
| Tsis | SI setup time | 450 | | | ns |
| Tsih | SI hold time | 450 | | | ns |
| Tcssod | CSB fall edge to SO delay time | | | 950 | ns |
| Tcksod | SCLK fall edge to SO delay time | | | 950 | ns |
| Tcssoo | CSB fall edge to SO data out time | 0 | | | ns |
| Tcssoz | CSB rise edge to SO Hi-Z out time | | | 950 | ns |

REGISTER DESCRIPTION

SPI Register Map

The SPI interface allows read access to the entire address space. The Main registers can only be written in Standby

mode and then only if the write lock bit MSAENB has never been set high.

SPI REGISTER MAP

| Addr | Register | Description | Write Enable | Standby Mode | Normal Mode |
|------------------------------------|----------|---|--------------|--------------|--------------|
| IC SETUP REGISTER | | | | | |
| 00h | MRCONF0 | Main function General purpose setup | MSAENB | Read / Write | Read |
| 01h | MRCONF1 | PWM Input Specification | MSAENB | Read / Write | Read |
| 02h | MRCONF2 | Soft start EN setup / FG output setup / Dead time setup | MSAENB | Read / Write | Read |
| 03h | MRCONF3 | PWM undetected operation mode setup Soft start setting | MSAENB | Read / Write | Read |
| 04h | MRCONF4 | Activation frequency setup | MSAENB | Read / Write | Read |
| 05h | MRCONF5 | Current limit detection timing setup / Overcurrent detection setup | MSAENB | Read / Write | Read |
| 06H | MRCONF5 | For Internal Use Only | MSAENB | Read / Write | Read |
| 07h | MRCONF7 | Sync rectification setup Protection setup FET short Protection | MSAENB | Read / Write | Read |
| 08h | MRCONF8 | SSCG Protection setup Locking Protection Overheat protection | MSAENB | Read / Write | Read |
| 09h | MRCONF9 | WDT setup | MSAENB | Read / Write | Read |
| 0Ah | MRCONF10 | Error / warning masks and DIAG output setup | MSAENB | Read / Write | Read |
| 0Bh | MRCONF11 | Speed FB operation setup at deceleration WDT protection operation setup Latch setup | MSAENB | Read / Write | Read |
| 0Ch | MRCONF12 | Lead angle setup Silent drive setup STEP at the time of changing Speed FB target revolution | Always OK | Read / Write | Read / Write |
| SPEED CONTROL SETUP | | | | | |
| 10h | MRSPCT0 | Proportional Gain Setup | Always OK | Read / Write | Read / Write |
| 11h | MRSPCT1 | Integral Gain Setup | Always OK | Read / Write | Read / Write |
| 12h | MRSPCT2 | 3.125% Input PWM | Always OK | Read / Write | Read / Write |
| 13h | MRSPCT3 | 12.5% Input PWM | Always OK | Read / Write | Read / Write |
| 14h | MRSPCT4 | 25% Input PWM | Always OK | Read / Write | Read / Write |
| 15h | MRSPCT5 | 37.5% Input PWM | Always OK | Read / Write | Read / Write |
| 16h | MRSPCT6 | 50% Input PWM | Always OK | Read / Write | Read / Write |
| 17h | MRSPCT7 | 62.5% Input PWM | Always OK | Read / Write | Read / Write |
| 18h | MRSPCT8 | 75% Input PWM | Always OK | Read / Write | Read / Write |
| 19h | MRSPCT9 | 87.5% Input PWM | Always OK | Read / Write | Read / Write |
| 1Ah | MRSPCT10 | 96.875% Input PWM | Always OK | Read / Write | Read / Write |
| SYSTEM DIAGNOSTICS AND TEST | | | | | |
| 20h | MRACS | Lock Bits for OTP and Main Register write | | Read | Read |
| 30h | MRACK | SPI Operation Diagnostics | - | Read | Read |
| 31h | MRODL | OTP data READ | Always OK | Read / Write | Read |
| 32h | MRRST | For WDT/Protection Reset | Always OK | Read / Write | Read / Write |

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SPI REGISTER MAP

| Addr | Register | Description | Write Enable | Standby Mode | Normal Mode |
|------------------------------------|----------|--------------------------------------|--------------|--------------|-------------|
| SYSTEM DIAGNOSTICS AND TEST | | | | | |
| 33h | MRORB | For OTP Zapping check | Always OK | Read / Write | Read |
| 34h | MRDIAG0 | Protection status check | - | Read | Read |
| 35h | MRDIAG1 | Protection status check | - | Read | Read |
| 38h | TEST1 | Production test register 1 | | | |
| ... | | | | | |
| 3C | TEST5 | Production test register 5 | | | |
| OTP MEMORY SECTION | | | | | |
| 40h | ORCONF0 | Default states of MRCONF0 – MRCONF12 | | | |
| ... | | | | | |
| 4Ch | ORCONF12 | transferred upon startup | | | |
| 50h | ORSPCT0 | Default states of MRSPCT0 – MRSPCT10 | | | |
| ... | | | | | |
| 5Ah | ORSPCT10 | transferred upon startup | | | |
| 60h | ORACS | Default states of MRACS | | | |

MOTOR CONFIGURATION REGISTER OVERVIEW

| ADDR[6:0] | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|---------------|-------------------|-----------|-------------|-----------|-------------|-----------|--------|---------|
| 00h | MRCONF0 | FRMD | FRREN | SCEN | PWMF | REGSEL | VCEN | LINSLP | LINIO |
| 01h | MRCONF1 | FLSEL[1:0] | | ZPSEL[1:0] | | PWMFL | PWMZP | PDTC | PWMON |
| 02h | MRCONF2 | SSTEN | FGOF[1:0] | | FDTI[4:0] | | | | |
| 03h | MRCONF3 | PDTSEL[1:0] | | SSTT[5:0] | | | | | |
| 04h | MRCONF4 | STOSC[7:0] | | | | | | | |
| 05h | MRCONF5 | CLMASK[3:0] | | | | OCMASK[3:0] | | | |
| 06h | MRCONF6 | Internal Use Only | | | | | | | |
| 07h | MRCONF7 | SYNCEN | PPDOSEL | FSCDT[1:0] | | FSCDL[3:0] | | | |
| 08h | MRCONF8 | SSCG | CPTM[3:0] | | | | THTH[1:0] | | TSTS |
| 09h | MRCONF9 | WDTEN | WDTP | WDT[5:0] | | | | | |
| 0Ah | MRCONF10 | VCLVPEN | CPEN | THWEN | THPEN | FSPEN | OVPEN | OCPEN | DIAGSEL |
| 0Bh | MRCONF11 | DWNSET[1:0] | | WDTSEL[1:0] | | CPLT | FSPLT | OCPLT | DLTO |
| 0Ch | MRCONF12 | STEPSEL[2:0] | | | SLMD | LASET[3:0] | | | |

MRCONF0

| Address = 00h | | | | Standby Mode: Read/Write | | | |
|---------------|-------|------|------|--------------------------|------|--------|-------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| FRMD | FRREN | SCEN | PWMF | REGSEL | VCEN | LINSLP | LINIO |

FRMD: Forward / Reverse MoDe

The physical motor rotation direction depends on the wiring of the three phases.

FRMD = 1 reverses the motor direction.

FRREN: FFree Running Enable

Decides if the LV8907 does a BEMF detection before attempting to start the motor open-loop excitation and

commutation.

FRREN = 0 Motor will start with a BEMF detection.

FRREN = 1 Motor will start open-loop with startup parameters.

SCEN: external Speed Control Enable

This bit selects the LV8907 internal speed feedback control or PWM pass-through. Speed feedback control is

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active when SCEN = 0. RPM is selected from input duty cycle as shown in Figure 11.

SCEN = 1: External speed control, the internal closed-loop speed control is inactivated.

PWMF: PWM input frequency selection

Decides the PWM input frequency range and PWM translation configuration.

PWMF = 0: Indirect PWM translation or closed-loop speed control. Valid PWM input frequency from 5.3 Hz to 1 kHz.
 PWMF = 1: Direct PWM pass-through. Valid PWM input frequency up to 18.5 kHz. In this mode the PWM frequency is directly fed to the power stage. Internal closed-loop speed control cannot be used.

The following table shows the configuration summary based on the combination of SCEN and PWMF.

| SCEN | PWMF | Speed Control | Input PWM Frequency Range [Hz] | Output PWM Frequency |
|------|------|---------------------|--------------------------------|----------------------|
| 0 | 0 | closed-loop | 5.3 to 1000 | 19.5 [kHz] |
| 1 | 0 | indirect translated | 5.3 to 1000 | 19.5 [kHz] |
| 0 | 1 | direct pass-through | up to 18500 | same as input |
| 1 | 1 | direct pass-through | up to 18500 | same as input |

MRCONF1

| | | | | | | | |
|---------------|---|------------|---|--------------------------|-------|------|-------|
| Address = 01h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| FLSEL[1,0] | | ZPSEL[1,0] | | PWMFL | PWMZP | PDTC | PWMON |

FLSEL: Full Load fallback level SElection

If 100% PWM input duty cycle was detected (no PWM frequency) and PWMFL is set, the motor is driven with the duty cycle programmed into FLSEL as shown in the following table.

| FLSEL[1] | FLSEL[0] | Motor Duty Cycle[%] |
|----------|----------|---------------------|
| 0 | 0 | 25 |
| 0 | 1 | 50 |
| 1 | 0 | 75 |
| 1 | 1 | 100 |

ZPSEL: Zero Power fallback level SElection

If 0% PWM input duty cycle is detected (no PWM frequency) and PWMZP is set, the motor is driven with the

REGSEL: VCC REGulator SElection (5 V / 3.3 V)

REGSEL = 0 VCC output set to 3.3 V.

REGSEL = 1 VCC output set to 5 V.

VCEN: VCC Regulator Enable

VCEN = 0 VCC is off.

VCEN = 1 VCC is active.

LINSLP: LIN Slope Mode Setup

To improve EMI performance the LIN switching slope can be reduced.

LINSLP = 0 Normal LIN rise time.

LINSLP = 1 Rise time increased by 1/3.

LINIO: LIN Input/Output selection

LV8907 has an embedded LIN physical layer which can also be used as a PWM input channel.

LINIO = 0 LIN_PWMIN is in PWM input mode.

LINIO = 1 The LIN transceiver is active and the PWM signal is taken from PWMIN.

duty cycle programmed into ZPSEL as shown in the following table.

| ZPSEL[1] | ZPSEL[0] | Motor Duty Cycle[%] |
|----------|----------|---------------------|
| 0 | 0 | 25 |
| 0 | 1 | 50 |
| 1 | 0 | 75 |
| 1 | 1 | 100 |

PWMFL: PWM Full Load fallback enable

If 100% PWM input duty cycle was detected the motor will be

PWMFL = 0: turned off.

PWMFL = 1: driven with the duty cycle defined by FLSEL.

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PWMZP: PWM Zero Power fallback enable

If 0% PWM input duty cycle is detected the motor will be.
 PWMZP = 0: turned off.
 PWMZP = 1: driven with the duty cycle defined by ZPSEL.

PDTC: Pending Detection of a Transition Control

During the first 200 ms after EN high, while the PWM signal is still being measured, the motor can be either
 PDTC = 0: turned off.

PDTC = 1: driven with the duty cycle defined by PDTSEL (MRCONF3[7,6])

PWMON: PWM ON polarity

Decides whether the PWM input signal is active low, or active high.

PWMON = 0: PWM input signal is active high.

PWMON = 1: PWM input signal is active low.

MRCONF2

| | | | | | | | |
|---------------|-----------|----------|-----------|--------------------------|----------|----------|--------------|
| Address = 02h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| SSTEN | FGOF[1,0] | | FDTI[4:0] | | | | |

SSTEN: Soft Start ENable

Soft start (current ramp) allows slow startup of motors with higher inertia. The soft start algorithm ramps the current limit from 0 to max current in 16 steps during soft start time t_{SST} which is programmed in register MRCONF3.

SSTEN = 0 Soft start is OFF.

SSTEN = 1 Soft start is active.

Note that soft start typically begins after duty cycle detection. If no duty cycle operation is selected (PDTC = 1) soft start will begin after reset.

FGOF: Frequency Generator Output Frequency

The FG signal is a representation of a successfully detected BEMF transition which occurs three times during every electrical revolution. It is possible to divide that frequency as described in the following table.

| FGOF[1] | FGOF[0] | FG output mode |
|---------|---------|---------------------------------------|
| 0 | 0 | One transition per BEMF detection |
| 0 | 1 | One pulse per electrical revolution |
| 1 | 0 | One transition every two BEMF det |
| 1 | 1 | One pulse every two elec. Revolutions |

FDTI: Fet Dead Time

During phase switching between supply and GND it is possible for both low- and high-side drivers to be

temporarily on at the same time causing large current spikes. Register FDTI defines a dead time during which both drivers will be kept off during these transitions.

| FDTI[4] | FDTI[3] | FDTI[2] | FDTI[1] | FDTI[0] | Dead time[μ s] |
|---------|---------|---------|---------|---------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 3.2 |
| 0 | 0 | 0 | 0 | 1 | 3.1 |
| FDTI | | | | | 3.2 - FDTI/10 |
| 1 | 1 | 1 | 1 | 0 | 0.2 |
| 1 | 1 | 1 | 1 | 1 | 0.1 |

MRCONF3

| | | | | | | | |
|---------------|----------|-----------|----------|--------------------------|----------|----------|--------------|
| Address = 03h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| PDTSEL[1,0] | | SSTT[5:0] | | | | | |

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PDTSEL: Pending Detection of a Transition SElection

If bit PDTC is set the motor is driven with the duty cycle programmed into PDTSEL as shown in the following table,

as soon as EN is high. This feature is bridging the initial 200 ms of operation until a valid PWM duty cycle can be decoded.

| PDTSEL[1] | PDTSEL[0] | Motor Duty Cycle[%] |
|-----------|-----------|---------------------|
| 0 | 0 | 25 |
| 0 | 1 | 50 |
| 1 | 0 | 75 |
| 1 | 1 | 100 |

SSTT: Soft Start Time

Soft start allows startup of motors with higher inertia by ramping the current. The soft start algorithm divides the current limit voltage 100 mV (Typ.) into 16 sections and

increases the value from 6.25 mV to 100 mV to switch over the current limit value. The soft start can be set from 0.1 s < t_{SSTT} < 6.72 s as shown in the table below:

| SSTT[5] | SSTT[4] | SSTT[3] | SSTT[2] | SSTT[1] | SSTT[0] | Soft Start time[s] |
|---------|---------|---------|---------|---------|---------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0.105 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0.21 |
| SSTT | | | | | | $0.105 \times (1 + SSTT)$ |
| 1 | 1 | 1 | 1 | 1 | 0 | 6.615 |
| 1 | 1 | 1 | 1 | 1 | 1 | 6.72 |

MRCONF4

| Address = 04h | | | | | | | | Standby Mode: Read/Write |
|---------------|---|---|---|---|---|---|-------|---------------------------------|
| | | | | | | | | Normal Mode: Read Only |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
| STOSC[7:0] | | | | | | | | Startup commutation period [ms] |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.82 |
| STOSC | | | | | | | | $0.82 \times (1 + STOSC)$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 209.92 |

This register defines the rotation frequency f_{STOSC} at which the motor should be turned during open-loop startup. If a BEMF signal can be detected the IC will commutate to the next energization pattern by using the zero-crossing as its reference. If no BEMF can be detected the IC will

commutate to the next energization pattern with the frequency programmed into STOSC. Open-loop startup continues for the time programmed into CPTM (MRCONF8[6:3]) If no BEMF is detected during that time a locked rotor error is indicated.

MRCONF5

| Address = 05h | | | | | | | | Standby Mode: Read/Write |
|---------------|---|---|---|-------------|---|---|-------|--------------------------|
| | | | | | | | | Normal Mode: Read Only |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
| CLMASK[4:0] | | | | OCMASK[4:0] | | | | |

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CLMASK: Current Limit MASKing time

In order to prevent noise and glitches from causing false current limiting, a mask time can be programmed.

| CLMASK[3] | CLMASK [2] | CLMASK [1] | CLMASK [0] | Mask Time[us] |
|-----------|------------|------------|------------|-----------------|
| 0 | 0 | 0 | 0 | 0.1 |
| 0 | 0 | 0 | 1 | 0.2 |
| CLMASK | | | | 0.1 + CLMASK/10 |
| 1 | 1 | 1 | 0 | 1.5 |
| 1 | 1 | 1 | 1 | 1.6 |

OCMASK: Over Current MASKing time

The time to detect overcurrent can be programmed with OCMASK.

| OCMASK[3] | OCMASK [2] | OCMASK [1] | OCMASK [0] | Mask Time[us] |
|-----------|------------|------------|------------|----------------------------------|
| 0 | 0 | 0 | 0 | 0.2 |
| 0 | 0 | 0 | 1 | 0.4 |
| OCMASK | | | | $0.2 \times (1 + \text{OCMASK})$ |
| 1 | 1 | 1 | 0 | 3.0 |
| 1 | 1 | 1 | 1 | 3.2 |

MRCONF6

| | | | | | | | |
|---------------|---|---|---|--------------------------|---|---|-------|
| Address = 06h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| SROFFT[3-0] | | | | CRMASK[3-0] | | | |

7. Internal use only.

MRCONF7

| | | | | | | | |
|---------------|---------|------------|---|--------------------------|---|---|-------|
| Address = 07h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| SYNCEN | PPDOSEL | FSCDT[1:0] | | FSCDL[3:0] | | | |

SYNCEN: Synchronous Rectification Enable

Defines synchronous rectification mode for the output stage. In synchronous rectification the high- and low-side switches are always switched in complementary mode = if one switch is on, the other one is off. In a-synchronous rectification both complementary switches may be off and the motor current is circling through the body diodes.

SYNCEN = 0 Synchronous rectification is ON.

SYNCEN = 1 Synchronous rectification is OFF.

PPDOSEL: Pwm Problem Diagnostics Output SElection

D6 of the main register MRCONF7 can be used to reflect abnormal detection result to DIAG pin at the time of PWM input abnormal detection (0% or 100% detection).

PPDOSEL = 0 PWM abnormal input detection result is reflected on DIAG pin.

PPDOSEL = 1 the result is not reflected on DIAG pin.

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FSCDT: Fet Short–Circuit Detection Time

By monitoring FET Vds, the time from FET's ON signal output until detecting Shorted status can be set with D5 and

D4 of MRCONF7. Please refer to the table below for settable time:

| FSCDT[1] | FSCDT [0] | Detection Time[us] |
|----------|-----------|--------------------|
| 0 | 0 | 3.2 |
| 0 | 1 | 6.4 |
| 1 | 0 | 9.6 |
| 1 | 1 | 12.8 |

FSCDL: Fet Short–Circuit Detection Level

Vds voltage to detect FET Short status can be set with D3~D0 of MRCONF7. Please refer to the table below for available voltages:

| FSCDL [3] | FSCDL[2] | FSCDL [1] | FSCDL [0] | Vth[V] |
|-----------|----------|-----------|-----------|----------------|
| 0 | 0 | 0 | 0 | 0.1 |
| 0 | 0 | 0 | 1 | 0.2 |
| FSCDL | | | | 0.1 + FSCDL/10 |
| 1 | 1 | 1 | 0 | 1.5 |
| 1 | 1 | 1 | 1 | 1.6 |

MRCONF8

| Address = 08h | | | | Standby Mode: Read/Write | | | |
|---------------|-----------|---|---|--------------------------|---|------|-------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| SSCG | CPTM[3-0] | | | THTH[1,0] | | TSTS | |

SSCG: Spread Spectrum Chp Generation

The Charge pump may have radiation noise issues due to switching at 52.1 kHz(typ.). By activating SSCG it is possible to disperse frequency components of the charge pump switching frequency. The frequency will vary 20%.

SSCG = 0: Spread spectrum OFF.

SSCG = 1: Spread spectrum ON.

A locked rotor is detected by counting the time the IC is in Startup mode (without BEMF detection) If no BEMF is detected for the time programmed into CPTM register the motor is turned off and a locked rotor is flagged.

In Auto recovery mode the motor will remain off for eight times the Open–Loop Startup Timeout before another startup is attempted.

CPTM: Constrained movement Protection TiMe

A locked rotor protection circuit is embedded in order to protect IC and Motor during locked rotor conditions.

| CPTM [3]s | CPTM [2] | CPTM [1] | CPTM [0] | Detection/Restart time[s] |
|-----------|----------|----------|----------|-----------------------------------|
| 0 | 0 | 0 | 0 | 0.42 / 3.36 |
| 0 | 0 | 0 | 1 | 0.84 / 6.72 |
| CPTM | | | | 0.42 × (1+CPTM) / 3.36 × (1+CPTM) |
| 1 | 1 | 1 | 0 | 6.3 / 50.4 |
| 1 | 1 | 1 | 1 | 6.72 / 53.76 |

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THTH: THreshold of THERmometer

LV8907 has an embedded comparator to monitor the external power FET's temperature using an external thermistor. If the voltage at TH drops below the threshold

level (shown in the table), the external overtemperature protection is activated, the output gate driver stage is turned off and the THPO error flag is set.

| THTH[1] | THTH [0] | V _{TH} [V] |
|---------|----------|---------------------|
| 0 | 0 | 0.35 |
| 0 | 1 | 0.30 |
| 1 | 0 | 0.25 |
| 1 | 1 | 0.20 |

TSTS: Thermal Shutdown Temperature Setting

The LV8907 monitors its own junction temperature to protect against overtemperature damage. Two different warning and shutoff levels can be selected:

TSTS = 0: Overtemperature warning occurs at 125°C(typ.), shutdown at 150°C(typ.).

TSTS = 1: Overtemperature warning occurs at 150°C(typ.), shutdown at 175°C(typ.).

MRCONF9

| Address = 09h | | | | Standby Mode: Read/Write | | | |
|---------------|------|----------|---|--------------------------|---|---|-------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| WDTEN | WDTP | WDT[5:0] | | | | | |

WDTEN: Watchdog Timeout ENable

This bit can enable or disable the watchdog. For increased system robustness it is possible to permanently lock access to this bit. See OTP section for more details.

WDTEN = 1 Watchdog is active.

WDTEN = 0 Watchdog is disabled.

WDTP = 0 Motor off.

WDTP = 1 Motor is driven with the PWM duty cycle as defined by WDTSEL (MRCONF11[5,4]).

WDT: Watchdog Timer Setting

The end time of the watchdog timer is defined by register WDT.

WDTP: Watchdog Timeout Protection mode selection

Operation mode following watchdog timeout can be selected.

| WDT [5] | WDT [4] | WDT [3] | WDT [2] | WDT [1] | WDT [0] | Detection Time[ms] |
|---------|---------|---------|---------|---------|---------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1.64 |
| 0 | 0 | 0 | 0 | 0 | 1 | 3.28 |
| WDT | | | | | | 1.64 × (1 + WDT) |
| 1 | 1 | 1 | 1 | 1 | 0 | 103.32 |
| 1 | 1 | 1 | 1 | 1 | 1 | 104.96 |

MRCONF10

| Address = 0Ah | | | | Standby Mode: Read/Write | | | |
|---------------|------|-------|-------|--------------------------|-------|-------|---------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| VCLVPEN | CPEN | THWEN | THPEN | FSPEN | OVPEN | OCPEN | DIAGSEL |

xEN: Error and Warning Mask

The higher seven bit in this register allows enabling and disabling of various errors and warnings. A one in the register masks the error, a zero activates the protection. The following errors and warnings can be masked:

- VCLVPEN = 0: VCC Low voltage protection enabled
- CPEN = 0: Constrained movement Protection ENable
- THWEN = 0: Thermal warning output enabled
- THPEN = 0: Thermal protection enabled

- FSPEN = 0: FET short protection enabled
- OVPEN = 0: Overvoltage protection enabled
- OCPEN = 0: Overcurrent protection enabled

DIAGSEL: Diagnosis Output Polarity Selection

This bit selects the polarity of the DIAG signal
 DIAGSEL = 0 The DIAG pin is active low.
 DIAGSEL = 1 The DIAG pin is active high and draws pull-down current when off.

MRCONF11

| | | | | | | | |
|---------------|----------|-------------|----------|--------------------------|----------|----------|--------------|
| Address = 0Bh | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| DWNSET[1,0] | | WDTSEL[1,0] | | CPLT | FSPLT | OCPLT | DLTO |

DWNSET: slowDoWN SETting

During speed control mode, motor deceleration can lead to energy recuperation and temporary voltage spikes. DWNSET allows for various degrees of energy recuperation:

- Normal Mode
Results in a tightest control and maximum energy recuperation. The application circuit has to be able to absorb the energy generated
- Sync OFF Mode
The motor is essentially not driven until it has reached the target speed. This does not feed any energy back into the supply, but may take a long time if motor inertia is high and losses are low
- Slow Response Mode
This mode is essentially imposing a slow deceleration ramp on the control speed. The energy recuperated is similar to Normal Mode but spread over a longer period of time reducing the voltage overshoot

| DWNSET[1] | DWNSET [0] | Mode |
|-----------|------------|------------------------------|
| 0 | 0 | Normal Mode |
| 0 | 1 | Sync OFF Mode |
| 1 | 0 | Slow Response Mode (PROT/32) |
| 1 | 1 | Normal Mode |

WDTSEL: Watchdog Target–duty Selection

Bit WDTP (MRCONF9[6]) defines if a Watchdog timeout causes Halt mode (0% drive) or Drive mode. When Drive mode is selected the motor duty cycle is defined by WDTSEL as shown in the table below.

| WDTSEL[1] | WDTSEL[0] | Duty[%] |
|-----------|-----------|---------|
| 0 | 0 | 25 |
| 0 | 1 | 50 |
| 1 | 0 | 75 |
| 1 | 1 | 100 |

xPLT: Protection Latch Selection

The faults of the motor block, FET Short and overcurrent can cause intolerable large-current. To prevent repeated current flow during re-try attempts, it is possible to latch these errors. The LV8907 will remain disabled until the latch is cleared by the register MRRST.

- CPLT = 0 Auto recover after a motor block.
- CPLT = 1 Latch the IC off after a motor block.

- FSPLT = 0 Auto recover after a FET short.
- FSPLT = 1 Latch the IC off after a FET short.

- OCPLT = 0 Auto recover after overcurrent.
- OCPLT = 1 Latch the IC off after overcurrent.

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DLTO: Diagnostic output Latched Transitions Only

Selects which errors/warnings will actually trigger a DIAG transition.

DLTO = 0: Trigger DIAG for any non-masked error or

warning.

DLTO = 1: Trigger DIAG only for latched errors as defined by xPLT above.

MRCONF12

| | | | | | | | |
|---------------|---|---|------|--------------------------|---|---|-------|
| Address = 0Ch | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| STEPSEL[2-0] | | | SLMD | LASET[3-0] | | | |

8. This register is writeable in Normal mode.

STEPSEL: Speed Transition stEP SELECTION

In speed control mode, large steps in motor target speed can cause excessive current spikes, noise and wear on the mechanical components. The LV8907 allows to impose a limit on the difference between target speed and actual speed such that every electrical revolution only a fraction of the previous rotational (PROT) speed is allowed to change. This limit is defined by STEPSEL in register MRCONF12[7-5].

NOTE: Note: During closed-loop speed control optimization and/or evaluation, it might be useful to turn off this ramp imposing (STEPSEL[2:0]= 0b000).

Figure 17 shows the RPM ramping response to an input step for six different ramp settings for instance.

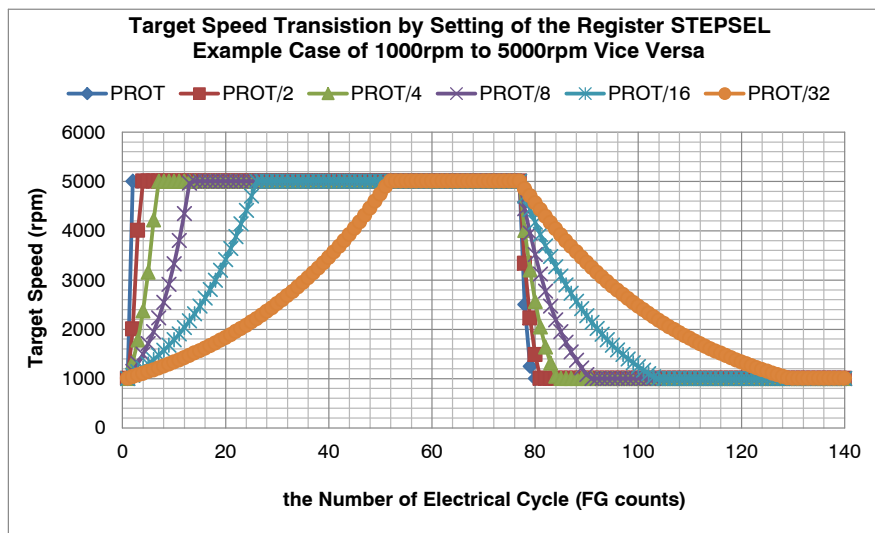


Figure 17. Speed Control Input Ramp of Different STEPSEL Settings

| STEPSEL[2] | STEPSEL[1] | STEPSEL[0] | Step Mode |
|------------|------------|------------|---------------------------------------|
| 0 | 0 | 0 | PROT (Current electrical speed at FG) |
| 0 | 0 | 1 | PROT/2 |
| 0 | 1 | 0 | PROT/4 |
| 0 | 1 | 1 | PROT/8 |
| 1 | 0 | 0 | PROT/16 |
| 1 | 0 | 1 | PROT/32 |
| 1 | 1 | 0 | PROT |
| 1 | 1 | 1 | PROT |

SLMD: Sinusoidal Mode Driving

This bit selects whether the motor phases are driven with a trapezoidal or pseudo-sinusoidal signal.

SLMD = 0 Trapezoidal drive with 120 degrees energization.

SLMD = 1 Sinusoidal drive with 150 degrees energization.

LASET: Lead Angle Setting

In trapezoidal drive mode it is possible to advance the commutation point towards zero-crossing of the BEMF signal. This helps to achieve BEMF field-weakening for higher rotational speeds and to compensate for delays in high speed operation.

| LASET [3] | LASET [2] | LASET [1] | LASET [0] | Lead Angle[deg] |
|-----------|-----------|-----------|-----------|-----------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1.875 |
| LASET | | | | LASET × 1.875 |
| 1 | 1 | 1 | 0 | 26.25 |
| 1 | 1 | 1 | 1 | 28.125 |

SPEED CONTROL REGISTER OVERVIEW

| ADDR[6:0] | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----------|---------------|----|-----------|----|----|---------|----|----|----|--|
| 10h | MRSPCT0 | - | PX[2:0] | | - | PG[2:0] | | | | |
| 11h | MRSPCT1 | - | IX[2:0] | | - | IG[2:0] | | | | |
| 12h | MRSPCT2 | - | FGT0[6:0] | | | | | | | |
| 13h | MRSPCT3 | - | FGT1[6:0] | | | | | | | |
| 14h | MRSPCT4 | - | FGT2[6:0] | | | | | | | |
| 15h | MRSPCT5 | - | FGT3[6:0] | | | | | | | |
| 16h | MRSPCT6 | - | FGT4[6:0] | | | | | | | |
| 17h | MRSPCT7 | - | FGT5[6:0] | | | | | | | |
| 18h | MRSPCT8 | - | FGT6[6:0] | | | | | | | |
| 19h | MRSPCT9 | - | FGT7[6:0] | | | | | | | |
| 1Ah | MRSPCT10 | - | FGT8[6:0] | | | | | | | |

Speed Control Loop Gain Setting

Closed-loop motor rotation speed controller (PI) is provided. The block diagram is shown in Figure 18.

Where,

TAG: target speed (period)

PROT: previous speed feedback (period)

Int: previous sum

K: scaling factor

$$K = \frac{VS}{128 \times 512}$$

Proportional Gain can be set with PX and PG of MRSPCT0 where the total gain is the product of both components PG and PX. Integral Gain can be set with IX, and IG of MRSPCT1 respectively. These P and I parameters can be changed while a motor is running (i.e. EN = HIGH). MRSPCT0 must be written, followed by writing MRSPCT1 through SPI. To update the P and I parameters of the control logic block simultaneously, MRSPCT0 code is suspended until MRSPCT1 is written. The calculation operates every FG cycle. The period is measured by 104 kHz clock.

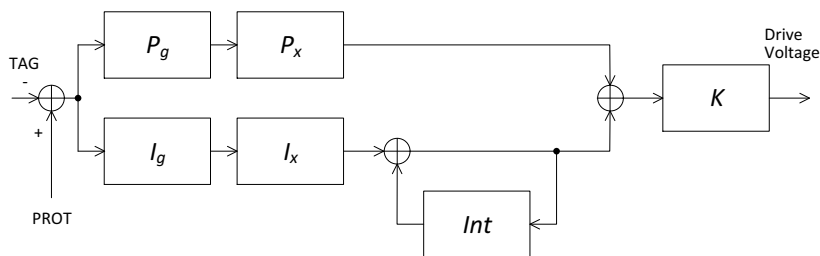


Figure 18. PI Speed Controller Block Diagram

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| PX, IX [2] | PX, IX [1] | PX, IX [0] | Gain |
|------------|------------|------------|------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 32 |
| 1 | 1 | 0 | 64 |
| 1 | 1 | 1 | 0 |

| PG, IG [2] | PG, IG [1] | PG, IG [0] | Gain |
|------------|------------|------------|------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 7/8 |
| 0 | 1 | 0 | 6/8 |
| 0 | 1 | 1 | 5/8 |
| 1 | 0 | 0 | 4/8 |
| 1 | 0 | 1 | 3/8 |
| 1 | 1 | 0 | 2/8 |
| 1 | 1 | 1 | 1/8 |

The proportional gain is a product of PX and PG, and the integrator gain is a product of IX and IG.

| Value | Px Ix | | Pg Ig | |
|-------|--------|---------|--------|---------|
| | Factor | Setting | Factor | Setting |
| 0.125 | x1 | 0 | x1/8 | 7 |
| 0.250 | x1 | 0 | x2/8 | 6 |
| 0.250 | x2 | 1 | x1/8 | 7 |
| 0.375 | x1 | 0 | x3/8 | 5 |
| 0.500 | x1 | 0 | x4/8 | 4 |
| 0.500 | x2 | 1 | x2/8 | 6 |
| 0.500 | x4 | 2 | x1/8 | 7 |
| 0.625 | x1 | 0 | x5/8 | 3 |
| 0.750 | x1 | 0 | x6/8 | 2 |
| 0.750 | x2 | 1 | x3/8 | 5 |
| 0.875 | x1 | 0 | x7/8 | 1 |
| 1.000 | x1 | 0 | x1 | 0 |
| 1.000 | x2 | 1 | x4/8 | 4 |
| 1.000 | x4 | 2 | x2/8 | 6 |
| 1.000 | x8 | 3 | x1/8 | 7 |
| 1.250 | x2 | 1 | x5/8 | 3 |
| 1.500 | x2 | 1 | x6/8 | 2 |
| 1.500 | x4 | 2 | x3/8 | 5 |
| 1.750 | x2 | 1 | x7/8 | 1 |
| 2.000 | x16 | 4 | x1/8 | 7 |
| 2.000 | x2 | 1 | x1 | 0 |
| 2.000 | x4 | 2 | x4/8 | 4 |
| 2.000 | x8 | 3 | x2/8 | 6 |
| 2.500 | x4 | 2 | x5/8 | 3 |
| 3.000 | x4 | 2 | x6/8 | 2 |
| 3.000 | x8 | 3 | x3/8 | 5 |
| 3.500 | x4 | 2 | x7/8 | 1 |
| 4.000 | x16 | 4 | x2/8 | 6 |
| 4.000 | x32 | 5 | x1/8 | 7 |
| 4.000 | x4 | 2 | x1 | 0 |
| 4.000 | x8 | 3 | x4/8 | 4 |
| 5.000 | x8 | 3 | x5/8 | 3 |
| 6.000 | x16 | 4 | x3/8 | 5 |
| 6.000 | x8 | 3 | x6/8 | 2 |

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| Value | Px lx | | Pg lg | |
|--------|--------|---------|--------|---------|
| | Factor | Setting | Factor | Setting |
| 7.000 | x8 | 3 | x7/8 | 1 |
| 8.000 | x16 | 4 | x4/8 | 4 |
| 8.000 | x32 | 5 | x2/8 | 6 |
| 8.000 | x64 | 6 | x1/8 | 7 |
| 8.000 | x8 | 3 | x1 | 0 |
| 10.000 | x16 | 4 | x5/8 | 3 |
| 12.000 | x16 | 4 | x6/8 | 2 |
| 12.000 | x32 | 5 | x3/8 | 5 |
| 14.000 | x16 | 4 | x7/8 | 1 |
| 16.000 | x16 | 4 | x1 | 0 |
| 16.000 | x32 | 5 | x4/8 | 4 |
| 16.000 | x64 | 6 | x2/8 | 6 |
| 20.000 | x32 | 5 | x5/8 | 3 |
| 24.000 | x32 | 5 | x6/8 | 2 |
| 24.000 | x64 | 6 | x3/8 | 5 |
| 28.000 | x32 | 5 | x7/8 | 1 |
| 32.000 | x32 | 5 | x1 | 0 |
| 32.000 | x64 | 6 | x4/8 | 4 |
| 40.000 | x64 | 6 | x5/8 | 3 |
| 48.000 | x64 | 6 | x6/8 | 2 |
| 56.000 | x64 | 6 | x7/8 | 1 |
| 64.000 | x64 | 6 | x1 | 0 |

Thus, there are some duplication with responding to the combination of X and G.

Target Speed Setting

There are two ways of setting a target speed with speed control active (SCEN = 0):

1. By using a companion microprocessor to write the speed value directly into the Speed Control Register via SPI
2. By applying a low frequency PWM input which selects a target speed from the Speed Control Register

SPI Speed Control

For SPI speed control the companion microprocessor should apply a fixed duty cycle PWM signal to the LV8907 PWMIN pin. An input duty cycle of 12.5% would then select speed register MRSPCT3 as shown in the table below. By writing RPM values to register MRSPCT3 via SPI, the speed can be controlled directly.

PWM Speed Control

PWM input frequency must be in Low frequency mode (PWMF = 0). In this mode the PWM input duty cycle is measured and used to select a target speed from the Speed Control Registers MRSPCT2..10. Note that 0% and 100% input duty cycle will be flagged as a “PWM Input Fault”.

| Input Duty Cycle(%) (Center Value of the Range) | Register |
|--|----------------------|
| 0 | 0% Duty Operation* |
| (3.125) | MRSPCT2 |
| 12.5 | MRSPCT3 |
| 25 | MRSPCT4 |
| 37.5 | MRSPCT5 |
| 50 | MRSPCT6 |
| 62.5 | MRSPCT7 |
| 75 | MRSPCT8 |
| 87.5 | MRSPCT9 |
| (96.875) | MRSPCT10 |
| 100 | 100% Duty Operation* |

*See Abnormal Duty Cycle Operation (100% or 0%)

There is a hysteresis of 6.25% duty cycle around each typical value resulting in the duty cycle thresholds depicted in Figure 11.

The motor speed is defined as ERPM (Electrical Revolutions Per Minute). To calculate the physical rotational speed RPM of the motor divide ERPM by the number of pole pairs of the motor. Each of the nine registers (FGT0[6:0] to FGT8[6:0]) selected by the input PWM above has 7 bits to program ERPM in a piecewise exponential function.

| Preset Target Speed RPM in Electrical Cycle | Register FGTx[6:0] Speed Index Code |
|---|-------------------------------------|
| 400 | 4 (0x04) |
| ...one step 200... | ...one step 1... |
| 13,200 | 68 (0x44) |
| ...one step 400... | ...one step 1... |
| 17,600 | 79 (0x4F) |
| ...one step 800... | ...one step 1... |
| 24,000 | 87 (0x57) |
| ...one step 2,000... | ...one step 1... |
| 40,000 | 95 (0x5F) |

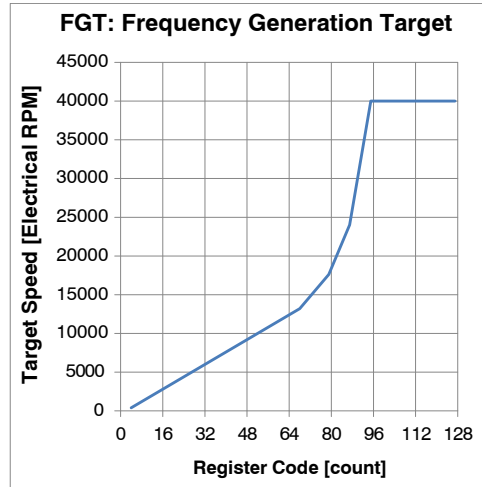


Figure 19. Speed Register Contents vs. Electrical RPM

MRACS

| Address = 20h | | | | Standby Mode: Read/Write | | | |
|---------------|---|---|---|--------------------------|---|--------|--------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | OSAENB | MSAENB |

This read-only register controls SPI access to the Main Registers and OTP Registers. Its contents are transferred from OTP Register ORACS at device startup.

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OSAENB: OTP registers SPI Access ENB

Controls write access to the OTP registers.
 OSAENB = 0: Write access permitted.
 OSAENB = 1: Write access denied.

MSAENB: Main registers SPI Access ENB

Controls write access to the Main registers.
 MSAENB = 0: Write access permitted.
 MSAENB = 1: Write access denied.

MRACK

| | | | | | | | |
|---------------|----------|----------|----------|-------------------------|----------|----------|--------------|
| Address = 30h | | | | Standby Mode: Read Only | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

This read only register is used to check IC and SPI interface. 55h is read from this register in standby and normal mode, FFh during sleep mode.

MRODL

| | | | | | | | |
|---------------|----------|----------|----------|--------------------------|----------|----------|--------------|
| Address = 31h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| MRODL[7:0] | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | OTP download |

A write access of 00h to this register initiates a copy operation of OTP data to the Main Register. This register is blocked if OBSY is high.

MRRST

| | | | | | | | |
|---------------|----------|----------|----------|--------------------------|----------|----------|----------------------|
| Address = 32h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read/Write | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| MRRST[7:0] | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | Reset Watchdog Timer |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | | | | Reset Error Latch |

This register is used to reset the watchdog timer or the error latch.

- Writing 00h to this register will reset the watchdog timer

- Writing FFh will reset the protection latch

MRORB

| | | | | | | | |
|---------------|----------|----------|----------|--------------------------|----------|----------|--------------|
| Address = 33h | | | | Standby Mode: Read/Write | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | ORBEN | ORBLV |

This register modifies the OTP readout threshold. After programming the OTP registers should be verified by reading them with the readout thresholds set low and high to detect false zeros and ones. See “OTP Programming”.

ORBEN: Otp Read Bias check ENable
 ORBEN = 0: Normal mode.
 ORBEN = 1: Margin read mode.

ORBLV: Otp Read Bias check LeVel.

- ORBLV = 0: Low level margin check
- ORBLV = 1: High level margin check

MRDIAG0

| | | | | | | | |
|---------------|----------|----------|----------|-------------------------|----------|----------|--------------|
| Address = 34h | | | | Standby Mode: Read Only | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| CPO | THPO | FSPO | VGLLVPO | CHPLVPO | VSOVPO | VSLVPO | OCPO |

Registers MRDIAG0 and MRDIAG1 indicate the system errors and/or warnings.

CPO: Constrained movement Protection Output

No BEMF was detected during the entire open-loop startup time as programmed in CPTM. Either the rotor is blocked, or startup parameters are not correct. The drivers are disabled.

THPO: Thermal Protection Output

The external temperature sensor input TH threshold was triggered. If the voltage at pin TH is lower than programmed in THTH the drivers will shut down. Tie TH to V3RO to disable this function.

FSPO: FET Short Protection Output

The drain-source voltage threshold across one of the external power FETs has been exceeded during operation. The threshold voltage is programmed in register FSCDL. Errors are suppressed for a blanking time as programmed in register FSCDT.

For the high-side FETs this voltage is measured between pin VS and the corresponding phase connection UOUT, VOUT, WOUT. For the low-side FETs it is measured between the phase connection and the pins SUL, SVL and SWL. Make sure to minimize potential voltage drops in the sense paths.

VGLLVPO: VGL Low Voltage Protection Output

The voltage at VGL has dropped below 5.5 V(max). The drivers are disabled to protect against low gate enhancement.

CHPLVPO: CHP Low Voltage Protection Output

The voltage between VS and VCP has dropped below 5.5 V(max). The drivers are disabled to protect against low gate enhancement.

VSOVPO: VS Overvoltage Protection Output

The voltage at VS has exceeded 20 V(min). The driver stage and the charge pump are disabled to protect against overvoltage at the charge pump.

VSLVPO: VS Low Voltage Protection Output

The voltage at VS has fallen below 5.1 V(max). The driver stage is disabled to protect against internal threshold issues.

OCPO: Overcurrent Protection Output

The voltage between current sense pins RFSENS and RF has exceeded 200 mV for longer than the overcurrent limit mask time programmed in OCMASK in register MRCONF5. The driver stage is disabled to protect against damage.

MRDIAG1

| | | | | | | | |
|---------------|----------|----------|----------|-------------------------|----------|----------|--------------|
| Address = 35h | | | | Standby Mode: Read Only | | | |
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| PWMPO | VCLVPO | - | SPCO | STUPO | WDTPO | THSPO | THWPO |

Registers MRDIAG0 and MRDIAG1 indicate the system errors and/or warnings.

PWMPO: PWM Input Abnormal Protection Output

The PWM input does not oscillate with the appropriate frequency or is steady high (100%) or low (0%). Depending on the settings in register MRCONF1 the driver stage will

turn off, or operate at a predefined duty cycle (emergency mode).

VCLVPO: VCC Low Voltage Protection Output

VCC undervoltage error. Depending on the setting of MRCONF0 on page MRCONF0 VCC is either 5 V(typ.) or 3.3 V(typ.). Undervoltage is flagged if VCC falls below 4.2 V(max.) or 2.7 V(max.) respectively.

SPCO: Speed Control issue Output

SPCO = 0, when the absolute value of the speed error is equal to or less than target × 1/16.

SPCO = 1, when the absolute value of the speed error is greater than target × 1/16.

STUPO: bemf-less StartUp Period Output

This flag indicates open-loop startup operation. No BEMF has been detected, yet.

WDTPO: WatchDog Timeout Protection Output

The watchdog has timed out. This flag will be high if the watchdog was not re-set during the time defined by MRCONF9. If the watchdog is enabled the driver stage will either be off or run in emergency mode with the settings defined by MRCONF11.

Flag WDTPO is high even if the watchdog is disabled.

THSPO: Thermal Shutdown Protection Output

The IC temperature is too high and the drivers are shutoff. The overtemperature shutoff level is defined by MRCONF8 to be either 150°C(min.) or 175°C(min.).

THWPO: Thermal Warning Protection Output

The IC temperature has exceeded the warning level. The overtemperature warning level is defined by MRCONF8 to be either 125°C(min.) or 150°C(min.).

OTP Registers

The OTP Registers contain the default values of the system registers. These registers are always readable via SPI in either Standby or Normal modes. During device startup these default values are copied from the OTP bank (SPI addresses 40 h to 60 h) to the Main register bank (SPI addresses 00 h to 20 h). The OTP registers should only be programmed once during IC initialization, during normal operation only the Main Registers are accessed and modified. It is possible to block programming of the OTP section by setting the OSAENB bit in the ORACS Register of the OTP.

For detailed information on the content of the OTP see the corresponding Main Register descriptions in the previous section. Main registers from 30h to 35h shown below are autonomous and have no equivalent position in the OTP as they report various internal data and status information.

| ADDR[6:0] | Bank | OTP Register | Function | Main Register | ADDR[6:0] |
|-----------|-------|--------------|------------------------|---------------|-----------|
| 40h | 0d[0] | ORCONF0 | ...corresponds to... | MRCONF0 | 00h |
| 41h | 0d[1] | ORCONF1 | | MRCONF1 | 01h |
| 42h | 0d[2] | ORCONF2 | | MRCONF2 | 02h |
| 43h | 0d[3] | ORCONF3 | | MRCONF3 | 03h |
| 44h | 0d[4] | ORCONF4 | | MRCONF4 | 04h |
| 45h | 1d[0] | ORCONF5 | | MRCONF5 | 05h |
| 47h | 1d[2] | ORCONF7 | | MRCONF7 | 07h |
| 48h | 1d[3] | ORCONF8 | | MRCONF8 | 08h |
| 49h | 1d[4] | ORCONF9 | | MRCONF9 | 09h |
| 4Ah | 2d[0] | ORCONF10 | | MRCONF10 | 0Ah |
| 4Bh | 2d[1] | ORCONF11 | | MRCONF11 | 0Bh |
| 4Ch | 2d[2] | ORCONF12 | | MRCONF12 | 0Ch |
| 50h | 2d[3] | ORSPCT0 | | MRSPCT0 | 10h |
| 51h | 2d[4] | ORSPCT1 | | MRSPCT1 | 11h |
| 52h | 3d[0] | ORSPCT2 | | MRSPCT2 | 12h |
| 53h | 3d[1] | ORSPCT3 | | MRSPCT3 | 13h |
| 54h | 3d[2] | ORSPCT4 | | MRSPCT4 | 14h |
| 55h | 3d[3] | ORSPCT5 | | MRSPCT5 | 15h |
| 56h | 3d[4] | ORSPCT6 | | MRSPCT6 | 16h |
| 57h | 4d[0] | ORSPCT7 | | MRSPCT7 | 17h |
| 58h | 4d[1] | ORSPCT8 | MRSPCT8 | 18h | |
| 59h | 4d[2] | ORSPCT9 | MRSPCT9 | 19h | |
| 5Ah | 4d[3] | ORSPCT10 | MRSPCT10 | 1Ah | |
| 60h | 4d[4] | ORACS | WRITE protection | MRACS | 20h |
| - | - | - | SPI Status Register | MRACK | 30h |
| - | - | - | Initiates OTP download | MRODL | 31h |

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| ADDR[6:0] | Bank | OTP Register | Function | Main Register | ADDR[6:0] |
|-----------|------|--------------|--------------------|---------------|-----------|
| - | - | - | Watchdog Reset | MRRST | 32h |
| - | - | - | Margin read checks | MRORB | 33h |
| - | - | - | Diagnostic Flags | MRDIAG0 | 34h |
| - | - | - | Diagnostic Flags | MRDIAG1 | 35h |

OTP Data Download

The OTP register data is typically transferred into the main registers at device startup (From sleep to standby

transition). This operation takes up to 110 μ s. A high OBSY flag in the first returned byte during a SPI transaction indicates this.

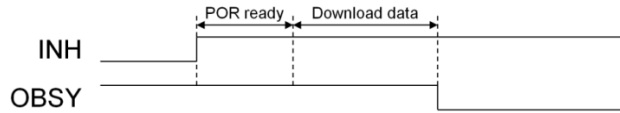


Figure 20. OTP Data Download Timing at Startup

An OTP download can also actively be initiated by writing 00h to register MRODL. This command requires monitoring the OBSY flag. Don't perform specific register

access (MRCONF, MRSPCT, ORCONF, ORSPCT, ORACS) until the OBSY flag is cleared.

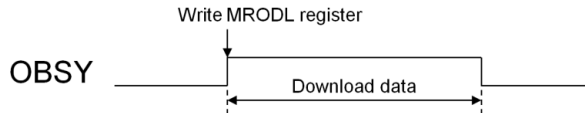


Figure 21. OTP Data Download Timing after an MRODL Command

OTP Programming Overall

Figure 20 shows overall of the OTP memory write and verify flow. It consists of preparation, write and three times of data integrity verification.

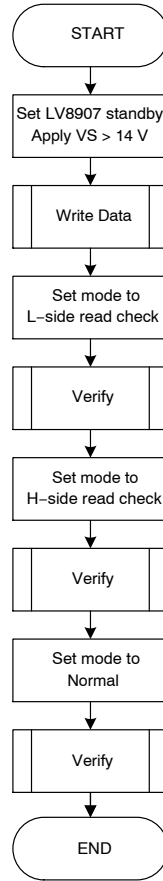


Figure 22. OTP Memory Write and Verify Flow

OTP Programming

The OTP registers can be programmed in Standby mode only while the write lock bit OSAENB is set 0. And, the supply voltage at pin VS must be more than 14 V. The actual write operation to the OTP memory will be done, when the state change from 0 to 1 is commanded. Once the bit state is changed to 1, it cannot be change back to 0. The number of writing is limited to one per bit.

The OTP memory consists of five memory banks. The bank contains five register bytes. The bank is filled by five

SPI write transactions. When the last address register in each bank is received, the busy-flag OBSY will be set and those five bytes will be programmed permanently into the corresponding OTP bank. The OBSY flag will be reset at the end of the write cycle. OBSY is in GSDAT register. To get GSDAT, SPI accesses to the register MRACK is recommended. MRACK doesn't interfere with the programming operation.

MRCONF, MRSPCT, ORCONF, ORSPCT, ORACS registers cannot be accessed during an OTP write cycle.

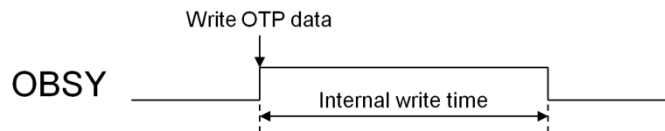


Figure 23. OTP Programming Timing

The programming takes 25 ms maximum. To simplify operation, a waiting for 25 ms plus margin can be applicable instead of a polling of the flag OBSY. (Figure 24)

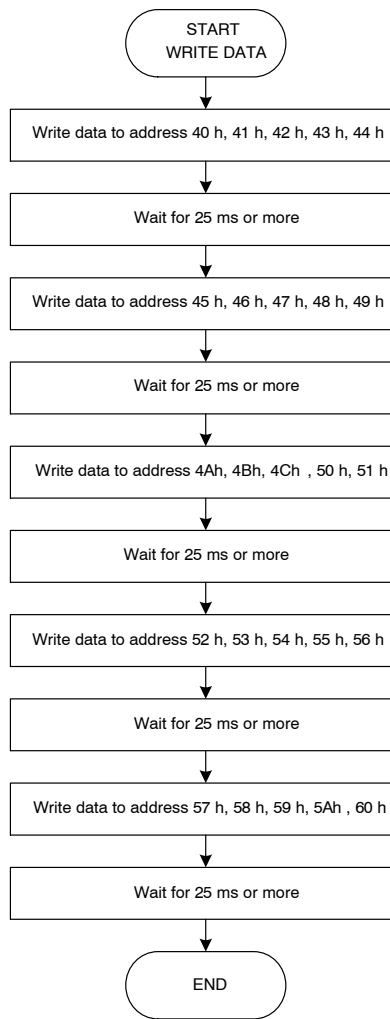


Figure 24. OTP Memory Write Operation

OTP Data Integrity Verification

In order to verify that the OTP programming operation was successful. It is strongly recommended to do an OTP margin check: To do this, the OTP registers are downloaded into the main register bank with minimum and maximum readout thresholds. This OTP download is forced by writing 00h to register MRODL. The readout threshold is set in register MRORB.

OTP Margin read check sequence after programmed:

1. Set OTP readout threshold “low” by setting ORBEN = 1 and ORBLV = 0 in register MRORB
2. Execute OTP download command by writing 00h to MRODL
3. Verify that the main register contents are consistent with the programmed OTP data
4. Set OTP readout threshold “high” by setting ORBEN = 1 and ORBLV = 1 in register MRORB
5. Execute OTP download command by writing 00h to MRODL

6. Verify that the main register contents are consistent with the programmed OTP data
7. Return OTP threshold to normal by setting ORBEN = 0 and ORBLV = 0
8. Execute OTP download command
9. Verify that the main register contents are consistent with the programmed OTP data

Locking OTP Register Contents

MSAENB bit and OSAENB bit of ORACS register are used in order to prevent write-access of main- and OTP registers respectively.

CAUTION: Inadvertent writing of these bits will permanently lock the corresponding register blocks from any further write access. Should only be set at end of development cycles.

LV8907UW

ORACS

| Address = 60h | | | | Standby Mode: Read Only | | | |
|---------------|---|---|---|-------------------------|---|--------|--------|
| | | | | Normal Mode: Read Only | | | |
| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | OSAENB | MSAENB |

This register is used in order to permanently prevent write access to the OTP and/or main registers. This register data is transferred into MRACS register.

OSAENB: Controls write access to the OTP registers.

OSAENB = 0: Write access permitted.

OSAENB = 1: Write access denied.

MSAENB: This bit is used in order to prevent write access to the main registers.

MSAENB = 0: Write access permitted.

MSAENB = 1: Write access denied.

Notice:

Generally, there is the risk of physical damage caused by unexpected overcurrent in some case of loss of commutation synchronization with a sensorless motor application. Its detail and mitigation are described in the application note, "[Lessons Learned from using LV8907UW in a BLDC Motor Application](#)".

APPENDIX

Table 3 shows Symbol name list.

The list expresses the genesis of name of the symbol in LV8907 datasheet.

Table 3. SYMBOL NAME LIST

| No. | Symbol | Symbol name Explanation |
|-----|---------|---|
| 1 | CHPLVPO | CH arge P ump L ow V oltage P rotection O utput |
| 2 | CLMASK | C urrent L imit M ASKing time |
| 3 | CPEN | C onstrained movement P rotection E Nable |
| 4 | CPLT | C onstrained movement P rotection L a T ch selection |
| 5 | CPO | C onstrained movement P rotection O utput |
| 6 | CPTM | C onstrained movement P rotection T IME |
| 7 | DIAGS | DI AG Status |
| 8 | DIAGSEL | DI AG polarity S ELECTION |
| 9 | DLTO | Di ag-output L atched T ransitions O nly |
| 10 | DWNSET | slow D o W N S ETting |
| 11 | FDTI | F et D ead T ime |
| 12 | FGOF | F requency G enerator O utput F requency (= rotation speed) |
| 13 | FGT | F requency G eneration T arget |
| 14 | FLSEL | F ull L oad fallback level S ELECTION (PWM input 100% duty mode) |
| 15 | FRMD | F orward/ R everse M o D e |
| 16 | FRREN | F ree R unning E Nable |
| 17 | FSCDL | F et S hort- C ircuit D etection L evel |
| 18 | FSCDT | F et S hort- C ircuit D etection T ime |
| 19 | FSPEN | F et S hort P rotection E Nable |
| 20 | FSPLT | F et S hort P rotection L a T ch selection |
| 21 | FSPO | F et S hort P rotection O utput |
| 22 | GSDAT | G eneral S tatus D A T a |
| 23 | LASET | L ead A ngle S ETting |
| 24 | LATCH | L A T C H ed shutdown status |
| 25 | LINIO | L IN I nput/ O utput selection |
| 26 | LINSLP | L IN S L O P e Mode setup |
| 27 | MRACK | M ain R egister A ccess C heck |
| 28 | MRACS | M ain R egister A C C ess S etting |
| 29 | MRCONF | M ain R egister C ON F iguration |
| 30 | MRDIAG | M ain R egister D IAG N ostics |
| 31 | MRODL | M ain R egister O tp D own L oad |
| 32 | MRORB | M ain R egister O tp R ead B ias check |
| 33 | MRRST | M ain R egister R e S e T |
| 34 | MRSPCT | M ain R egister S P E ed C on T rol |
| 35 | MSAENB | M ain registers S pi A ccess E Nable B ar (Disable) |
| 36 | OBSY | O tp B u S Y |
| 37 | OCMASK | O ver C urrent M ASKing time |
| 38 | OCPEN | O ver C urrent P rotection E Nable |
| 39 | OCPLT | O ver C urrent P rotection L a T ch selection |
| 40 | OCPO | O ver C urrent P rotection O utput |
| 41 | ORBEN | O tp R ead B ias check E Nable |

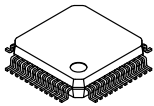
Table 3. SYMBOL NAME LIST (continued)

| | | |
|----|---------|--|
| 42 | ORBLV | Otp Read Bias check LeVel |
| 43 | OSAENB | Otp registers Spi Access ENable Bar (Disable) |
| 44 | OVPEN | OverVoltage Protection ENable |
| 45 | PDTC | Pending Detection of a Transition Control |
| 46 | PDTSEL | Pending Detection of a Transition SElection |
| 47 | PPDOSEL | Pwm Problem Diagnostics Output SElection |
| 48 | PWMF | PWM input Frequency selection |
| 49 | PWMFL | PWM Full Load fallback enable (PWM input 100% duty mode) |
| 50 | PWMON | PWM ON polarity |
| 51 | PWMPO | PWM input abnormal Protection Output |
| 52 | PWMZP | PWM Zero Power fallback enable (PWM input 0% duty mode) |
| 53 | REGSEL | Vcc REGulator SElection |
| 54 | SACF | Spi ACcess Failed |
| 55 | SCEN | external Speed Control ENable |
| 56 | SLMD | SinusoidaL Mode Driving |
| 57 | SMOD | Status MODe |
| 58 | SPCO | SPeed Control issue Output |
| 59 | SSCG | Spread Spectrum Chp Generation |
| 60 | SSTEN | Soft STart ENable |
| 61 | SSTT | Soft STart Time |
| 62 | STEPSEL | Speed Transition stEP SElection |
| 63 | STOSC | STartup OSCillator |
| 64 | STUPO | bemf-less STartUp Period Output |
| 65 | SYNCEN | SYNChronous rectification ENable (active low) |
| 66 | THPEN | THermal Protection ENable |
| 67 | THPO | THermal Protection Output |
| 68 | THSPO | THermal Shutdown Protection Output |
| 69 | THTH | THreshold of THermometer |
| 70 | THWEN | THermal Warning ENable |
| 71 | THWPO | THermal Warning Protection Output |
| 72 | TSTS | Thermal Shutdown Temperature Setting |
| 73 | VCEN | VCc Regulator ENable |
| 74 | VCLVPEN | VCc Low Voltage Protection ENable |
| 75 | VCLVPO | VCc Low Voltage Protection Output |
| 76 | VGLLVPO | VGL Low Voltage Protection Output |
| 77 | VSLVPO | VS Low Voltage Protection Output |
| 78 | VSOVPO | VS OverVoltage Protection Output |
| 79 | WDT | WatchDog Timeout duration setting |
| 80 | WDTEN | WatchDog Timeout Enable |
| 81 | WDTP | WatchDog Timeout Protection mode selection |
| 82 | WDTPO | WatchDog Timer Protection Output |
| 83 | WDTSEL | WatchDog Target-duty SElection |
| 84 | ZPSEL | Zero Power fallback level SElection (PWM input 0% duty mode) |

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

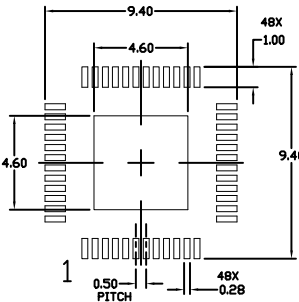
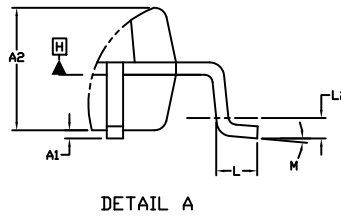
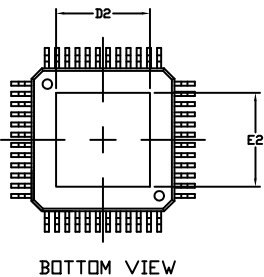
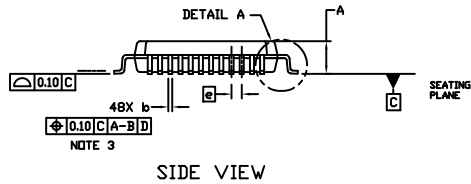
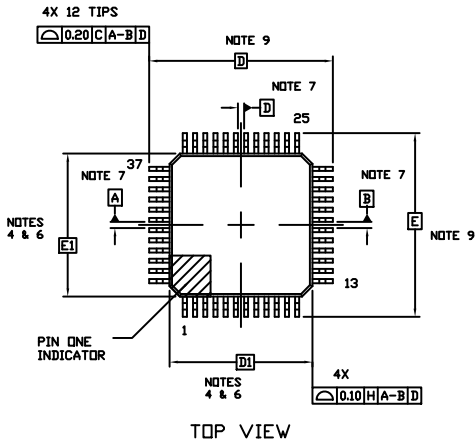


SPQFP48 7x7 / SQFP48K

CASE 131AN

ISSUE A

DATE 08 NOV 2013



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN. | MAX. |
| A | --- | 1.70 |
| A1 | 0.00 | 0.15 |
| A2 | 1.50 | REF |
| b | 0.15 | 0.26 |
| D | 9.00 | BSC |
| D1 | 7.00 | BSC |
| D2 | 4.60 | REF |
| E | 9.00 | BSC |
| E1 | 7.00 | BSC |
| E2 | 4.60 | REF |
| e | 0.50 | BSC |
| L | 0.30 | 0.70 |
| L2 | 0.25 | BSC |
| M | 0* | 10* |

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