CY25402/CY25422/CY25482

Two-PLL Programmable Clock Generator with Spread Spectrum

Features

- Two fully integrated phase-locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz
  - External reference: 8 to 166 MHz clock
- Reference clock input voltage range
  - 2.5 V, 3.0 V, and 3.3 V for CY25482
  - 1.8 V for CY25402 and CY25422
- Wide operating output frequency range
  - 3 to 166 MHz
- Programmable[1] spread spectrum with center and down spread option and lexmark and linear modulation profiles
- V_{DD} supply voltage options:
  - 2.5 V, 3.0 V, and 3.3 V for CY25402 and CY25482
  - 1.8 V for CY25422
- Frequency select feature with option to select four different frequencies
- Power-down, Output Enable, and SS ON/OFF controls
- Low jitter, high-accuracy outputs
- Ability to synthesize nonstandard frequencies with fractional-N capability
- Three clock outputs with programmable drive strength
- Glitch-free outputs while frequency switching
- 8-pin small outline integrated circuit (SOIC) package
- Commercial and industrial temperature ranges
- One-time programmability
  For programming support, contact Cypress technical support or send an e-mail to clocks@cypress.com

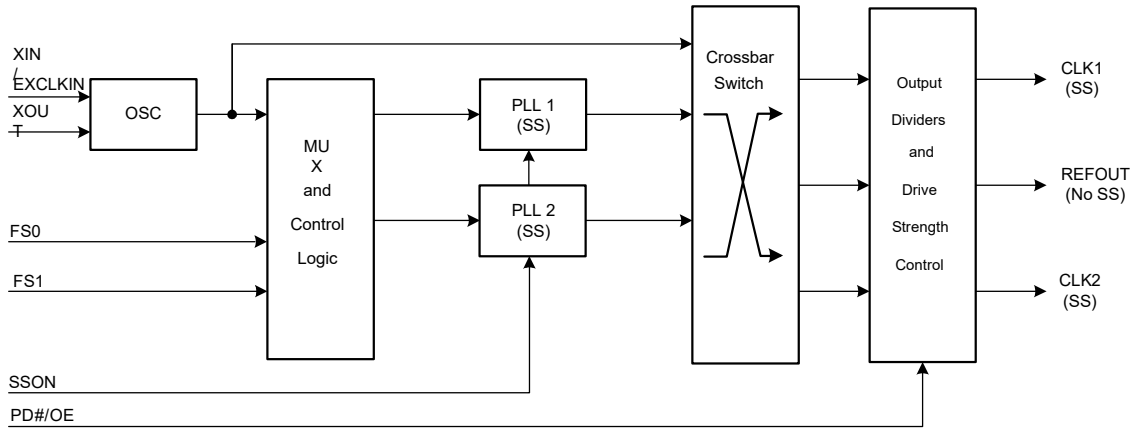
Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using spread spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of zero parts per million (PPM) frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low-power systems

Functional Description

For a complete list of related documentation, click here.

Block Diagram



Note
1. The devices mentioned in this datasheet are available as factory-programmable parts and not as field-programmable parts, since the associated programming software is currently not available. Visit www.cypress.com to create a Technical Support case, so Cypress can provide a programming file (.jed file) that matches your requirements.

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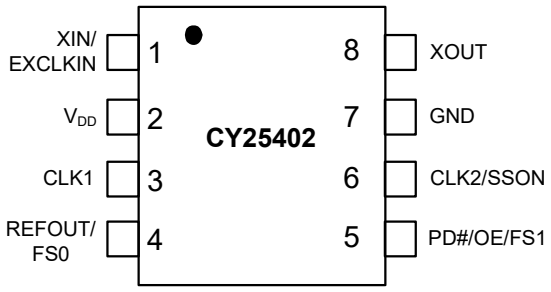
Device Selector Guide

Device	Crystal Input	EXCKLKIN Input	V_{DD}
CY25402	Yes	1.8 V LVCMOS	2.5 V, 3.0 V, 3.3 V
CY25482	No	2.5 V, 3.0 V, 3.3 V LVCMOS	2.5 V, 3.0 V, 3.3 V
CY25422	Yes	1.8 V LVCMOS	1.8 V

Pin Configuration

Figure 1. 8-pin SOIC Pinout

CY25402



Pin Definitions

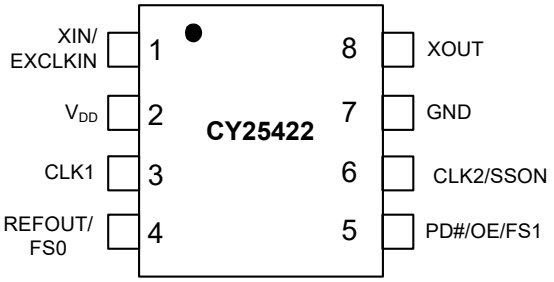
CY25402 (2.5 V, 3.0 V, or 3.3 V Supply)

Pin Number	Name	I/O	Description
1	XIN/EXCLKIN	Input	Crystal input or 1.8 V external clock input
2	V_{DD}	Power	Power supply: 2.5 V, 3.0 V, or 3.3 V
3	CLK1	Output	Programmable clock output with spread spectrum
4	REFOUT/FS0	Output/Input	Multifunction programmable pin: reference clock output with no spread spectrum or frequency select pin
5	PD#/OE/FS1	Input	Multifunction programmable pin: power-down, output enable or frequency select pin
6	CLK2/SSON	Output/Input	Multifunction programmable pin: programmable clock output with spread spectrum or spread spectrum ON/OFF control pin
7	GND	Power	Power supply ground
8	XOUT	Output	Crystal output

Pin Configuration

Figure 2. 8-pin SOIC Pinout

CY25422



Pin Definitions

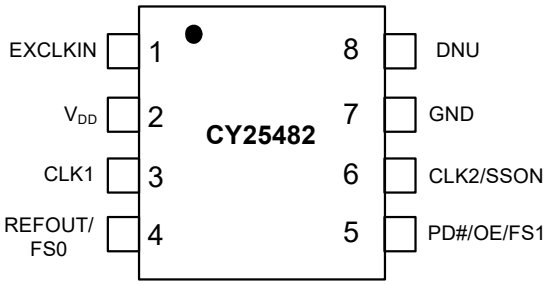
CY25422 (1.8 V Supply)

Pin Number	Name	I/O	Description
1	XIN/EXCLKIN	Input	Crystal input or 1.8 V external clock input
2	V_{DD}	Power	Power supply: 1.8 V
3	CLK1	Output	Programmable clock output with spread spectrum
4	REFOUT/FS0	Output/Input	Multifunction programmable pin: reference clock output with no spread spectrum or frequency select pin
5	PD#/OE/FS1	Input	Multifunction programmable pin: power-down, output enable or frequency select pin
6	CLK2/SSON	Output/Input	Multifunction programmable pin: programmable clock output with spread spectrum or spread spectrum ON/OFF control pin
7	GND	Power	Power supply ground
8	XOUT	Output	Crystal output

Pin Configuration

Figure 3. 8-pin SOIC Pinout

CY25482



Pin Definitions

CY25482 (2.5 V, 3.0 V, or 3.3 V Supply)

Pin Number	Name	I/O	Description
1	EXCLKIN	Input	2.5 V, 3.0 V, or 3.3 V external clock input
2	V_{DD}	Power	Power supply: 2.5 V, 3.0 V, or 3.3 V
3	CLK1	Output	Programmable clock output with spread spectrum
4	REFOUT/FS0	Output/Input	Multifunction programmable pin: reference clock output with no spread spectrum or frequency select pin
5	PD#/OE/FS1	Input	Multifunction programmable pin: power-down, output enable, or frequency select pin
6	CLK2/SSON	Output/Input	Multifunction Programmable pin: programmable clock output with spread spectrum or spread spectrum ON/OFF control pin
7	GND	Power	Power supply ground
8	DNU	Output	Do not use this pin

Functional Overview

Two Configurable PLLs

The CY25402, CY25422, and CY25482 have two programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having two PLLs is that a single device generates two independent frequencies from a single crystal.

Input Reference Clocks

The input reference clock can be either a crystal or a clock signal, for CY25402 and CY25422 while just a clock signal for CY25482. The input frequency range for crystal (XIN) is 8 MHz to 48 MHz and that for external reference clock (EXCLKIN) is 8 MHz to 166 MHz. The voltage range of the reference clock input for CY25482 is 2.5 V/3.0 V/3.3 V while that for CY25402 and CY25422 is 1.8 V. This gives user an option for this device to be compatible for different input clock voltage levels in the system.

V_{DD} Power Supply Options

These devices have programmable power supply options. The CY25402/CY25482 is a high voltage part that can be programmed to operate at any voltage 2.5 V, 3.0 V, or 3.3 V while CY25422 is a low voltage part that can operate at 1.8 V.

Output Source Selection

These devices have programmable input sources for each of its clock outputs. There are three available clock sources and these clock sources are: XIN/EXCLKIN, PLL1, and PLL2. Output clock source selection is done by using three out of three crossbar switch. Thus, any one of these three available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have two independent clock outputs.

Spread Spectrum Control

Both PLLs (PLL1 and PLL2) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK2/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with lexmark or linear profile.

Frequency Select

Each PLL can be programmed for up to four different frequencies. There are two multifunction programmable pins, REFOUT/FS0 and PD#/OE/FS1 which if programmed as frequency select inputs, can be used to select among these arbitrarily programmed frequency settings. Each output has programmable output divider options.

Glitch-Free Frequency Switch

When the frequency select pin, FS(1:0) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

PD#/OE Mode

Multifunction pin PD#/OE/FS1 (Pin 5) can be programmed to operate as either frequency select (FS1), power down (PD#) or output enable (OE) mode. PD# is a low-true input. If activated it shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings.

When this pin is programmed as Output Enable (OE), clock outputs can be enabled or disabled using OE (pin 5). Individual clock outputs can be programmed to be sensitive to this OE pin.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Pin Definitions on page 4 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The devices, CY25402, CY25422, and CY25482 can be custom programmed to any desired frequencies and listed features. For customer specific programming, contact your local Cypress field application engineer (FAE) or sales representative.

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage for CY25402/CY25482	–	–0.5	4.5	V
V_{DD}	Supply voltage for CY25422	–	–0.5	2.6	V
V_{IN}	Input voltage for CY25402/CY25482	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
V_{IN}	Input voltage for CY25422	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature, storage	Non Functional	–65	+150	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability rating	V-0 at1/8 in.	–	10	ppm
MSL	Moisture sensitivity level	SOIC package	3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	V_{DD} Operating voltage for CY25402/CY25482	2.25	–	3.60	V
V_{DD}	V_{DD} Operating voltage for CY25422	1.65	1.8	1.95	V
T_{AC}	Commercial ambient temperature	0	–	+70	°C
T_{AI}	Industrial ambient temperature	–40	--	+85	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low voltage	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output high voltage	I_{OH} = –2 mA, drive strength = [00]	V_{DD} – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{IL1}	Input low voltage of PD#/OE, FS0, FS1 and SSON	–	–	–	0.2 × V_{DD}	V
V_{IL2}	Input low voltage of EXCLKIN for CY25402/CY25422	–	–	–	0.3	V
V_{IL3}	Input low voltage of EXCLKIN for CY25482	–	–	–	0.2 × V_{DD}	V
V_{IH1}	Input High Voltage of PD#/OE, FS0, FS1 and SSON	–	0.8 × V_{DD}	–	–	V
V_{IH2}	Input high voltage of EXCLKIN for CY25402/CY25422	–	1.62	–	2.2	V
V_{IH3}	Input high voltage of EXCLKIN for CY25482	–	0.8 × V_{DD}	–	–	V
I_{IL}	Input low current, PD#/OE/FS1	V_{IN} = 0 V	–	–	10	µA
I_{IH}	Input high current, PD#/OE/FS1	V_{IN} = V_{DD}	–	–	10	µA
I_{ILDN}	Input low current, SSON and FS0 pins	V_{IN} = 0 V (Internal pull down resistor = 160k typ.)	–	–	10	µA
I_{IHDN}	Input high current, SSON and FS0 pins	V_{IN} = V_{DD} (Internal pull down resistor = 160k typ.)	14	–	36	µA
R_{DN}	Pull-down resistor of CLK1, REFOUT/FS0 and CLK2/SSON pins	Output clocks in off state by setting PD# = Low	100	160	250	kΩ
I_{DD}[2, 3]	Supply current for CY25422	PD# = High, No load	–	12	–	mA
	Supply current for CY25402/CY25482	PD# = High, No load	–	14	–	mA
I_{DDS}[2]	Standby current	PD# = Low	–	3	–	µA
C_{IN}[3]	Input capacitance	SSON, PD#/OE/FS1 and FS0 pins	–	–	7	pF

Notes
2. Guaranteed by design but not 100% tested.
3. Configuration dependent.

AC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{IN} (crystal)	Crystal frequency, XIN		8	–	48	MHz
F_{IN} (clock)	Input clock frequency (EXCLKIN)		8	–	166	MHz
F_{CLK}	Output clock frequency		3	–	166	MHz
DC	Output duty cycle, all clocks except Ref Out	Duty Ccycle is defined in Figure 5 on page 11; t_1/t_2, measured at 50% of V_{DD}	45	50	55	%
DC	Ref Out duty cycle	Ref In minimum 45%, maximum 55%	40	–	60	%
T_{RF1}[4]	Output rise/fall time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 11, C_{LOAD} = 15 pF, drive strength [00]	–	6.8	–	ns
T_{RF2}[4]	Output rise/fall time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 11, C_{LOAD} = 15 pF, drive strength [01]	–	3.4	–	ns
T_{RF3}[4]	Output rise/fall time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 11, C_{LOAD} = 15 pF, drive strength [10]	–	2.0	–	ns
T_{RF4}[4]	Output rise/fall time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 11, C_{LOAD} = 15 pF, drive strength [11]	–	1.0	–	ns
T_{CCJ}[4, 5]	Cycle-to-cycle jitter (peak)	Configuration dependent. See Configuration Example	–	100	–	ps
T_{LOCK}[5]	PLL lock time	Measured from 90% of the applied power supply level	–	1	3	ms

Configuration Example

For C-C Jitter

Ref. Frequency (MHz)	CLK1 Output		CLK2 Output	
	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)
14.3181	8.0	134	48	92
19.2	74.25	99	8	91
27	48	67	166	103
48	48	93	166	137

Notes
4. Guaranteed by design but not 100% tested.
5. Configuration dependent.

Recommended Crystal Specification

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	28	MHz
Fmax	Maximum frequency	14	28	48	MHz
R1	Motional resistance (ESR)	135	50	30	Ω
C0	Shunt capacitance	4	4	2	pF
CL	Parallel load capacitance	18	14	12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

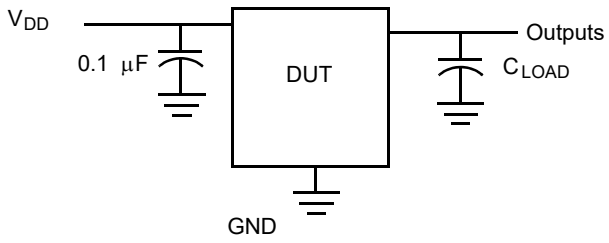
Recommended Crystal Specification

For Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum frequency	8	14	24	MHz
Fmax	Maximum frequency	14	24	32	MHz
R1	Motional resistance (ESR)	90	50	30	Ω
C0	Shunt capacitance	7	7	7	pF
CL	Parallel load capacitance	18	12	12	pF
DL(max)	Maximum crystal drive level	1000	1000	1000	µW

Test and Measurement Setup

Figure 4. Test and Measurement Setup



Voltage and Timing Definitions

Figure 5. Duty Cycle Definition

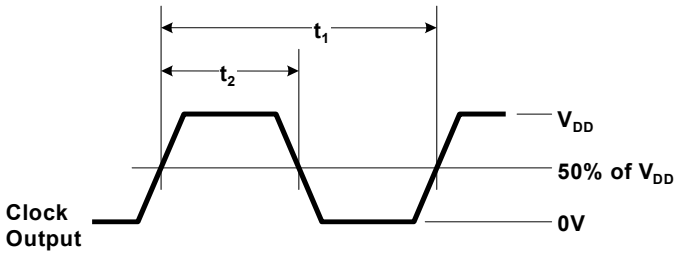
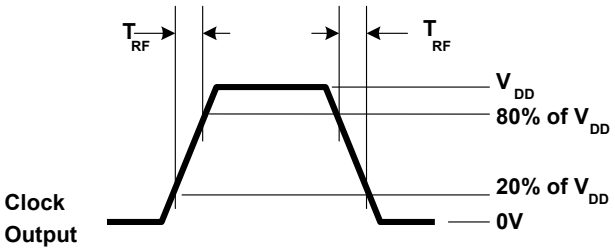


Figure 6. Rise Time = T_{RF}, Fall Time = T_{RF}



Ordering Information

Part Number	Type[6]	Package	Supply Voltage	Production Flow
Pb-free				
CY25402SXI	Field Programmable	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25402SXIT	Field Programmable	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25422FSXI	Field Programmable	8-pin SOIC	1.8 V	Industrial, –40 °C to +85 °C
CY25422FSXIT	Field Programmable	8-pin SOIC – Tape and Reel	1.8 V	Industrial, –40 °C to +85 °C
CY25482FSXI	Field Programmable	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25482FSXIT	Field Programmable	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
Programmer				
CY3675-CLKMAKER1		Programming kit		
CY3675-SOIC8A		Socket adapter board for programming CY25402, CY25403, CY25422, CY25423, CY25482, and CY25483		

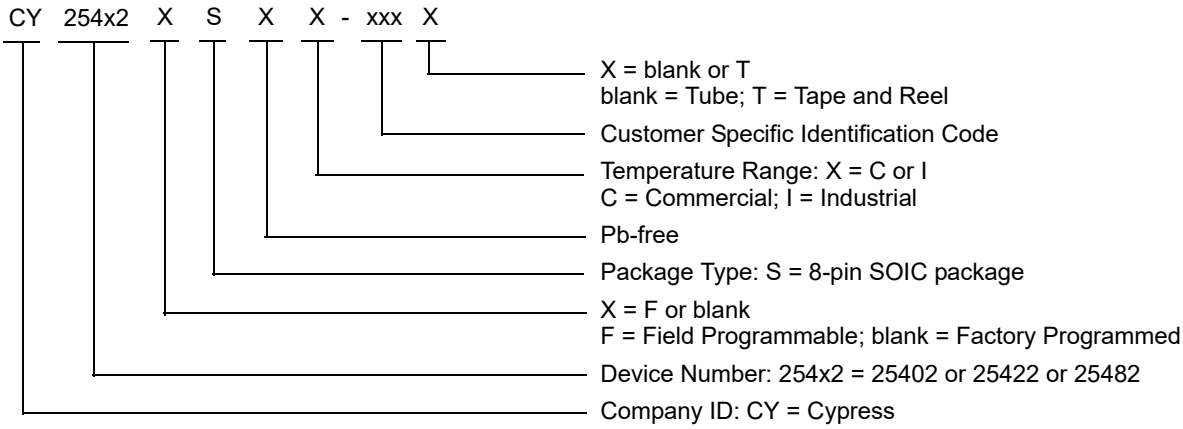
Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

Part Number[7]	Type	Package	Supply Voltage	Production Flow
Pb-free				
CY25402SXC-xxx	Factory Programmed	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Commercial, 0 °C to 70 °C
CY25402SXC-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Commercial, 0 °C to 70 °C
CY25422SXC-xxx	Factory Programmed	8-pin SOIC	1.8 V	Commercial, 0 °C to 70 °C
CY25422SXC-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	1.8 V	Commercial, 0 °C to 70 °C
CY25482SXC-xxx	Factory Programmed	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Commercial, 0 °C to 70 °C
CY25482SXC-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Commercial, 0 °C to 70 °C
CY25402SXI-xxx	Factory Programmed	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25402SXI-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25422SXI-xxx	Factory Programmed	8-pin SOIC	1.8 V	Industrial, –40 °C to +85 °C
CY25422SXI-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	1.8 V	Industrial, –40 °C to +85 °C
CY25482SXI-xxx	Factory Programmed	8-pin SOIC	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C
CY25482SXI-xxxT	Factory Programmed	8-pin SOIC – Tape and Reel	2.5 V, 3.0 V, or 3.3 V	Industrial, –40 °C to +85 °C

Notes
6. The devices mentioned in this datasheet are available as factory-programmable parts and not as field-programmable parts, since the associated programming software is currently not available. Visit www.cypress.com to create a Technical Support case, so Cypress can provide a programming file (.jed file) that matches your requirements.
7. xxx indicates Factory Programmable and are factory programmed configurations. For more details, contact your local Cypress FAE or sales representative.

Ordering Code Definitions

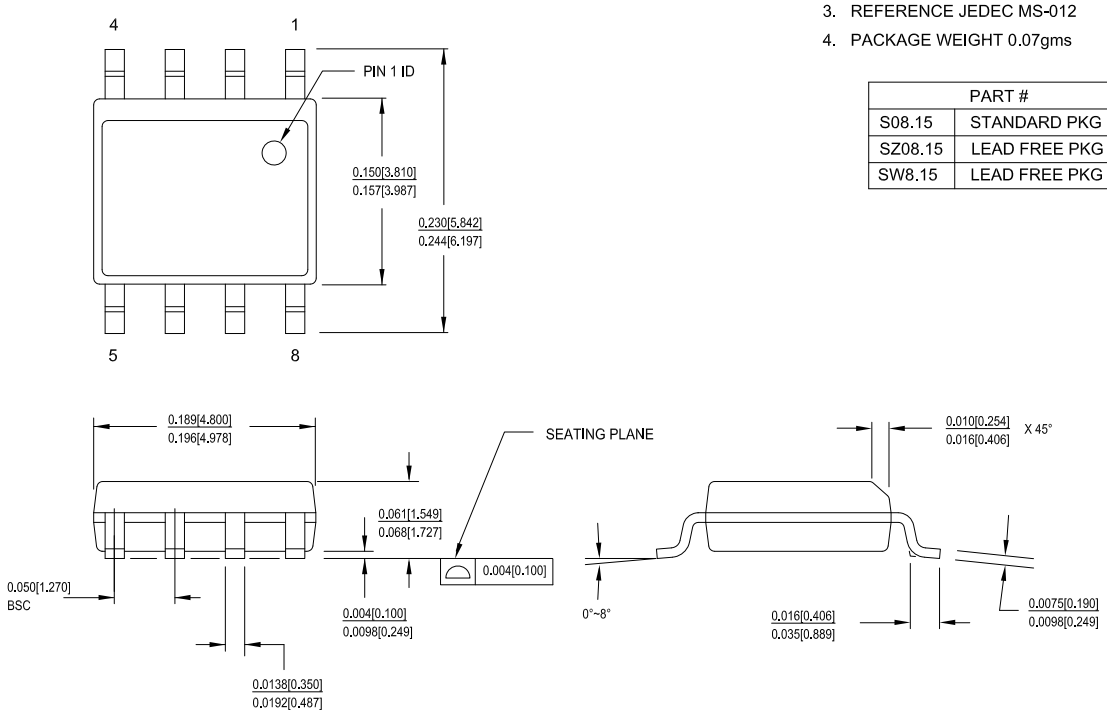


Package Drawing and Dimensions

Figure 7. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *I

Acronyms

Acronym	Description
DL	Drive Level
DNU	Do Not Use
DUT	Device Under Test
EIA	Electronic Industries Alliance
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FAE	Field Application Engineer
FS	Frequency Select
JEDEC	Joint Electron Devices Engineering Council
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
OE	Output Enable
OSC	Oscillator
PD	Power Down
PLL	Phase-Locked Loop
PPM	Parts Per Million
SS	Spread Spectrum
SSC	Spread Spectrum Clock
SSON	Spread Spectrum On

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
fF	femtofarad
MHz	megahertz
µs	microsecond
µW	microwatt
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY25402/CY25422/CY25482, Two-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12565				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	690296	RGL	01/17/2007	New data sheet.
*A	815788	RGL	03/02/2007	Minor Change: To post on web.
*B	1428744	RGL / AESA	08/30/2007	Updated Document Title to read as “CY25402/CY25422/CY25482 Two PLL Programmable Clock Generator with Spread Spectrum”. Changed status from Preliminary to Final. Added CY25482 part related information in all instances across the document. Updated Block Diagram. Updated Pin Definitions: Updated details in “Description” column. Updated Functional Overview: Updated description and added sub-sections. Updated Absolute Maximum Conditions: Updated details corresponding to V_{DD} and V_{IN} parameters. Updated Recommended Operating Conditions: Updated details corresponding to V_{DD} parameter. Updated DC Electrical Specifications: Updated almost entire table. Updated Ordering Information: Updated part numbers. Updated to new template.
*C	2748211	TSAI	08/10/2009	Post to external web.
*D	2898568	KVM	06/02/2010	Updated Ordering Information: Updated part numbers. Added Possible Configurations. Moved ‘xxx’ parts under Possible Configurations. Added Ordering Code Definitions. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *C to *D. Added Acronyms. Updated to new template.
*E	3110175	BASH	12/14/2010	Added Units of Measure. Updated to new template.
*F	3235621	CXQ	04/20/2011	Updated Ordering Information: Updated part numbers.
*G	4219507	CINM	12/13/2013	Updated Ordering Information: Updated part numbers. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*H	4473684	TAVA	08/25/2014	Updated Features: Added Note 1 and referred the same note next to “Programmable”. Updated Ordering Information: No change in part numbers. Added Note 6 and referred the same note in “Type” column.
*I	4586478	AJU	12/03/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.

Document History Page (continued)

Document Title: CY25402/CY25422/CY25482, Two-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12565				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	5590046	TAVA	01/17/2017	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*K	5726617	BPIN	05/18/2017	Updated Ordering Information: Updated part numbers. Updated to new template.
*L	5778002	PSR	06/19/2017	Updated Features: Added one-time programmability. Updated Pin Definitions: Updated details in “Description” column corresponding to pin number 4. Updated Pin Definitions: Updated details in “Description” column corresponding to pin number 4.
*M	5952857	XHT	10/31/2017	Updated DC Electrical Specifications: Updated details in “Description” and “Max” columns corresponding to V_{IL2} parameter. Added V_{IL3} parameter and its details. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *H to *I. Completing Sunset Review.

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