TEXAS INSTRUMENTS

SN74CB3Q16211 24-Bit Switch 2.5-V/3.3-V Low-Voltage FET Bus Switch

1 Features

- Member of the Texas Instruments Widebus® family
- High-bandwidth data path (up to 500 MHz[(1)])
- 5-V tolerant I/Os with device powered up or powered down
- Low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 5 Ω typical)
- Rail-to-rail switching on data I/O ports
  - 0-V to 5-V switching with 3.3-V V_{CC}
  - 0-V to 3.3-V switching with 2.5-V V_{CC}
- Bidirectional data flow, with near-zero propagation delay
- Low input or output capacitance minimizes loading and signal distortion ($C_{io(OFF)}$ = 4 pF typical)
- Fast switching frequency ($f_{\overline{OE}}$ = 20 MHz maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 1 mA typical)
- V_{CC} operating range from 2.3 V to 3.6 V
- Data I/Os support 0-V to 5-V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V)
- Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs
- I_{off} supports partial-power-down mode operation
- Latch-up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports both digital and analog applications: PCI interface, differential signal interface, memory interleaving, bus isolation, low-distortion signal gating [1]
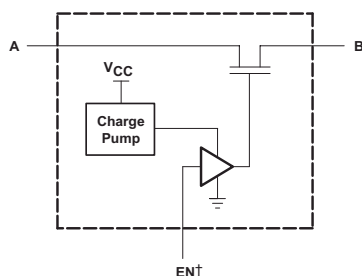
† EN is the internal enable signal applied to the switch.

Simplified Schematic, Each FET Switch (SW)

2 Applications

- AV receiver
- Blu-ray recorder and player
- Embedded PC
- Portable audio dock
- DLP front projection system

3 Description

The SN74CB3Q16211 device is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16211 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE
SN74CB3Q16211	TSSOP (56)	14.00 mm × 6.10 mm
	TVSOP (56)	11.30 mm × 4.40 mm
	SSOP (56)	18.40 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
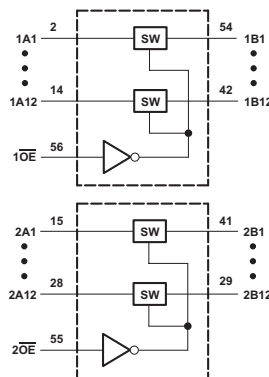
Terminal numbers shown are for the DGG, DGV, and DL packages.

Logic Diagram (Positive Logic)

[1] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

5 Description (continued)

The SN74CB3Q16211 device is organized as two 12-bit bus switches with separate output-enable (1 $\overline{OE}$, 2 $\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Table 5-1. Function Table
(Each 12-Bit Bus Switch)**

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

6 Pin Configuration and Functions

NC	1	56	1$\overline{OE}$
1A1	2	55	2$\overline{OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
V_{CC}	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12
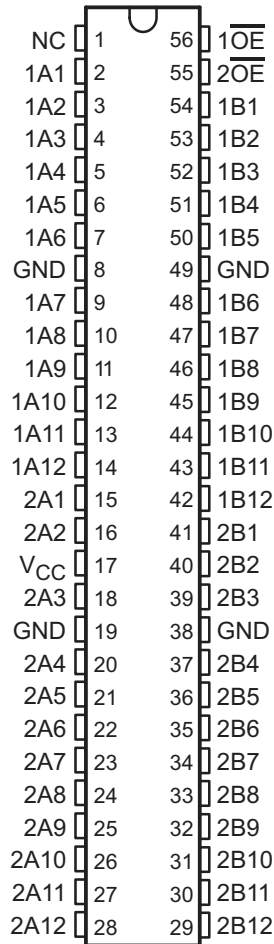
NC − No internal connection

Figure 6-1. DGG, DGV, or DL Package, 56-Pin TSSOP and TVSOP (Top View)
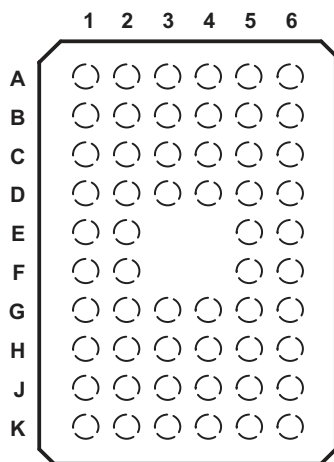
Figure 6-2. ZQL Package, 56-Pin BGA (Top View)

	1	2	3	4	5	6
A	1A2	1A1	NC	1$\overline{OE}$	2$\overline{OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V_{CC}	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

NC − No internal connection

Figure 6-3. Functions Table

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		−0.5	4.6	V
V_{IN}	Control input voltage range[2] [3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±64	mA
	Continuous current through V_{CC} or GND terminals			±100	mA
θ_{JA}	Package thermal impedance[6]	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
		GQL package		42	

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   All voltages are with respect to ground unless otherwise specified.
(3)   The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6)   The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	−65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

(1)   All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF, V_{IN} = V_{CC} or GND		1	3	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle			0.15	0.25	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			3.5	5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	V_{IN} = V_{CC} or GND,	Switch OFF, $V_{I/O}$ = 5.5 V, 3.3 V, or 0		4	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	V_{IN} = V_{CC} or GND,	Switch ON, $V_{I/O}$ = 5.5 V, 3.3 V, or 0		10	12.5	pF
r_{on} [6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		5	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		5	6.5	
			V_I = 2.4 V,	I_O = −15 mA		5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 7-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

7.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ [1]	$\overline{OE}$	A or B		10		20	MHz
t_{pd} [2]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	8	1.5	8	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	7.5	ns

(1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
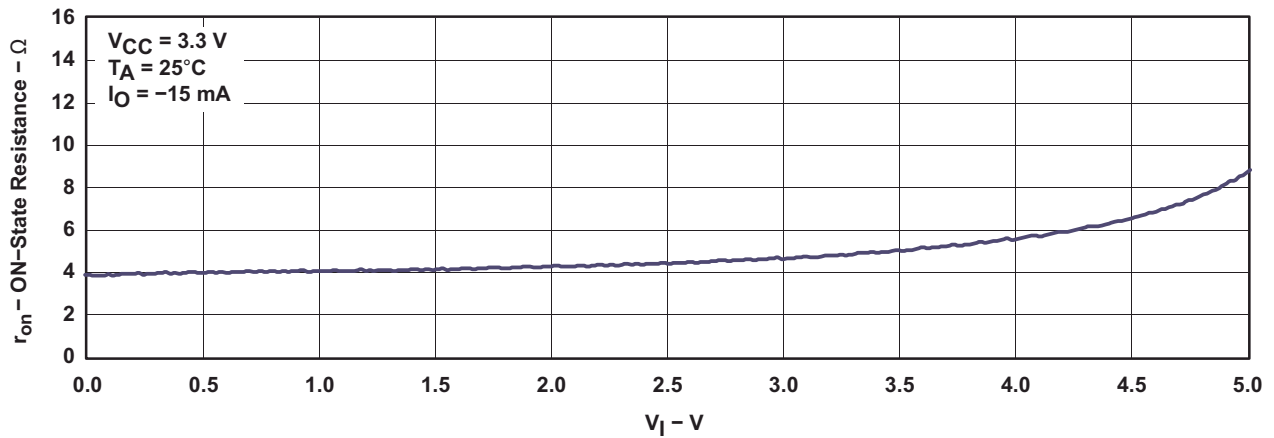
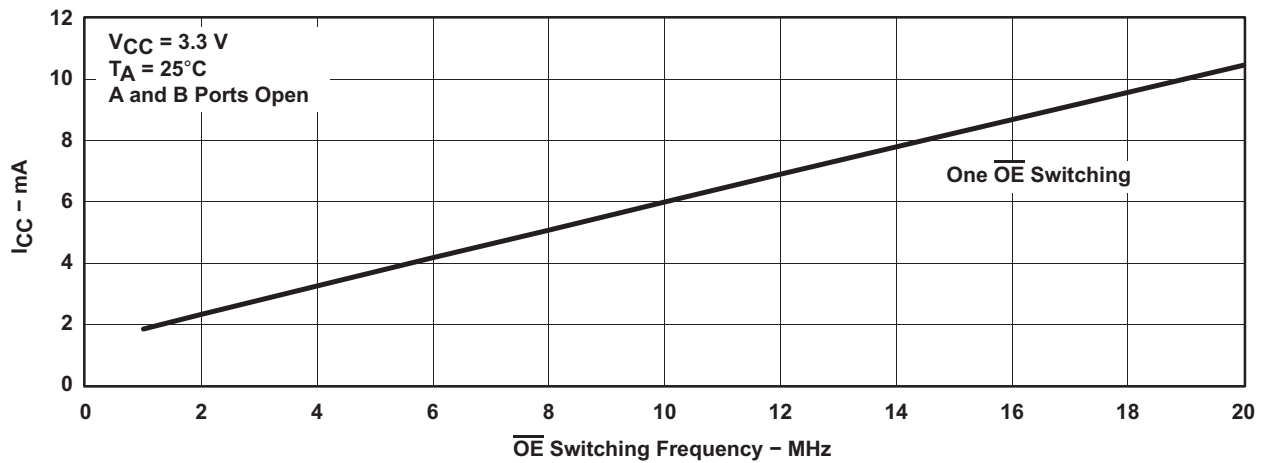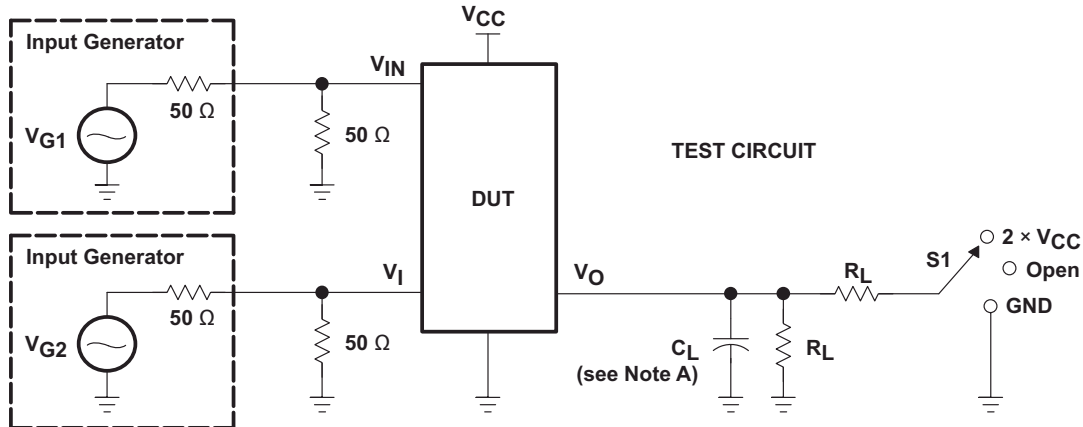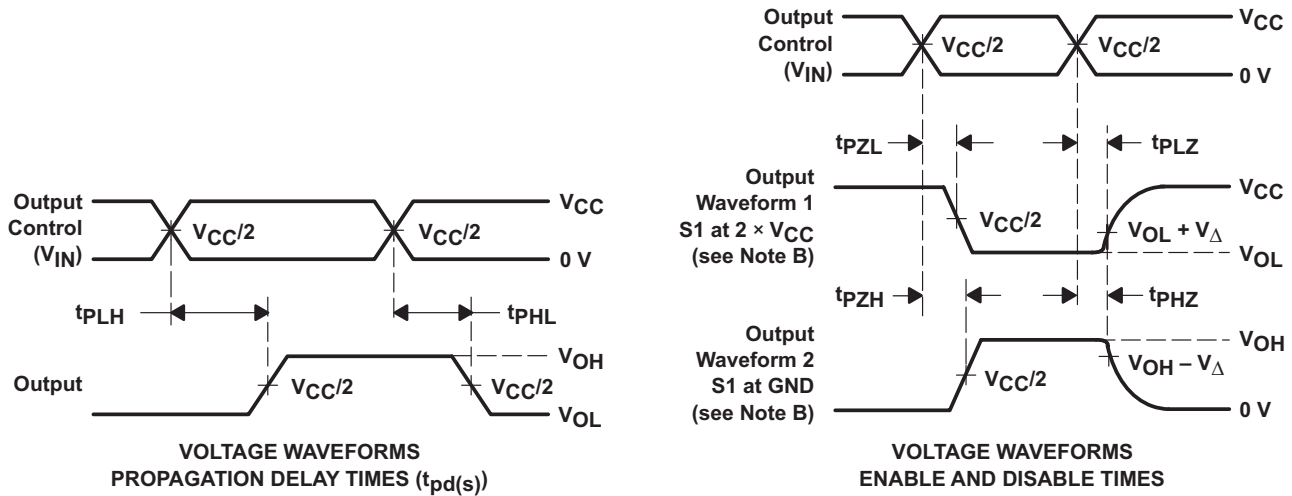## 7.6 Typical Characteristics

Figure 7-1. Typical r_{on} vs V_I

Figure 7-2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency

Product Folder Links: *SN74CB3Q16211*

8 Parameter Measurement Information

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V	Open	500 Ω	V_{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V	2 × V_{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V_{CC}	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V_{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V_{CC}	50 pF	0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤2.5 ns, t_f ≤2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 8-1. Test Circuit and Voltage Waveforms

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

* Texas Instruments, *CBT-C, CB3T, and CB3Q Signal-Switch Families* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3Q16211DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DGVR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BW211	Samples
SN74CB3Q16211DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 Q2 Q3 Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CB3Q16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CB3Q16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0

A

6.6
6.2 TYP

PIN 1 INDEX
AREA

54X 0.4

56

C

0.08 C

SEATING
PLANE

1

11.4
11.2
NOTE 3

2X
10.8

28

29

B

4.5
4.3
NOTE 4

56X 0.23
0.13

⊕ 0.1 Ⓜ C A B

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° -8°

0.75
0.50

1.2
1.1

0.15
0.05

DETAIL A
TYPICAL
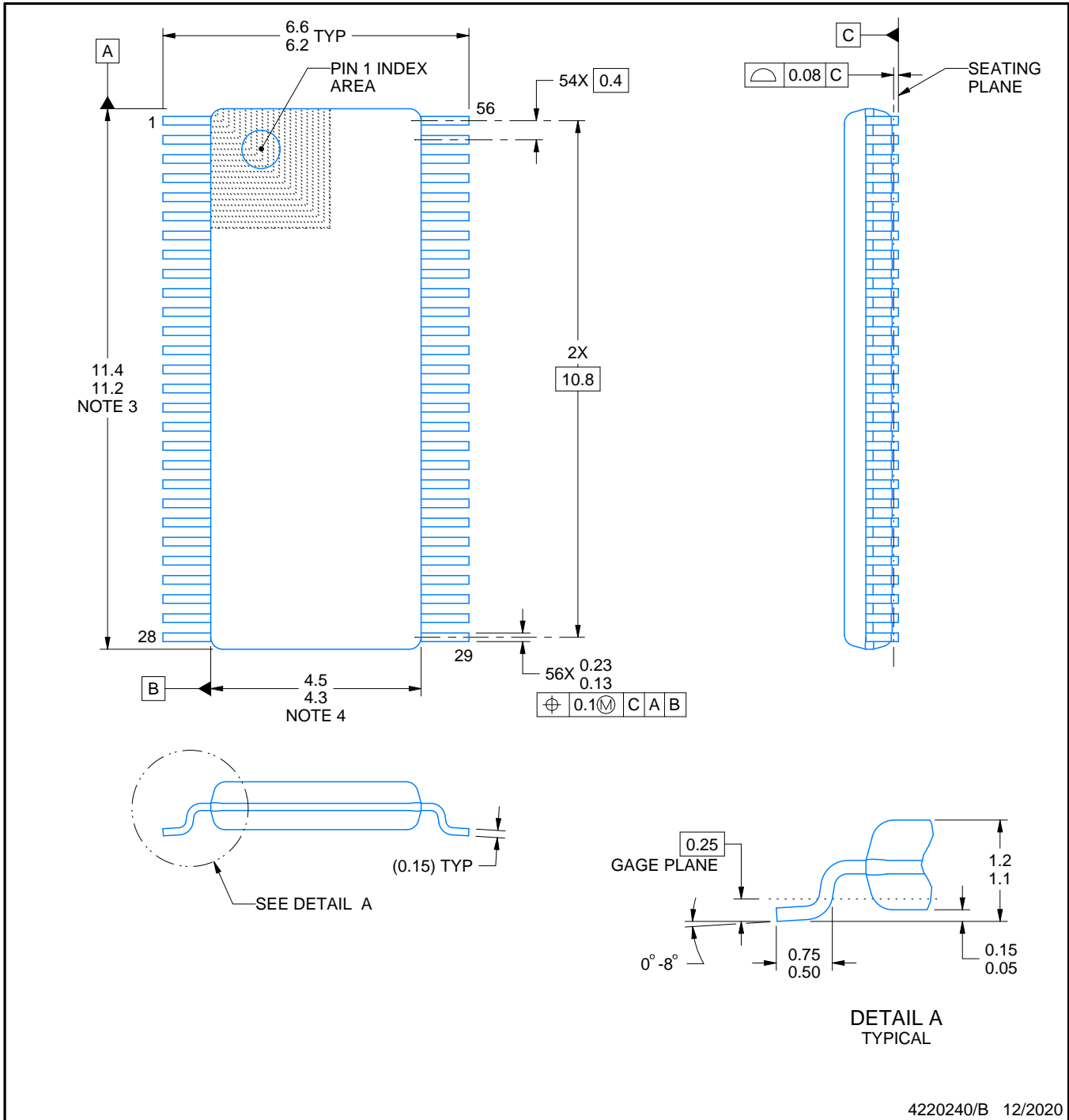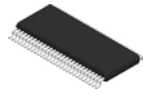
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

DGV0056A

TVSOP - 1.2 mm max height

56X
(1.4)

56X (0.2)

1

SYMM

(R0.05) TYP

56

54X (0.4)

SYMM

28

29

(5.9)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK
OPENING

METAL EDGE

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220240/B   12/2020
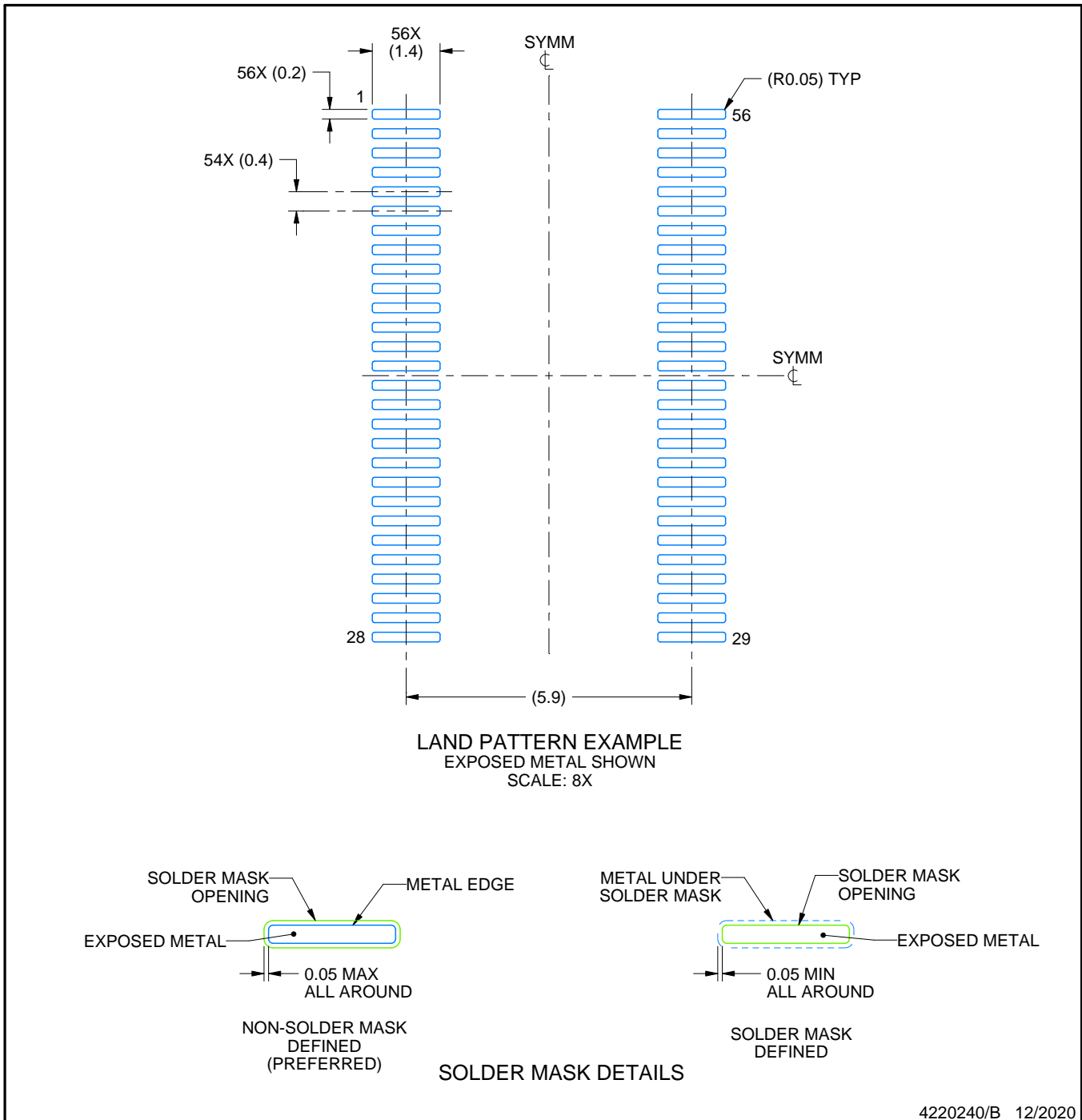
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220240/B   12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)   0.0135 (0,343)   ⊕ 0.005 (0,13) Ⓜ
                           0.008 (0,203)

56   29

                                                      0.420 (10,67)   0.010 (0,25)
                                                      0.395 (10,03)   0.005 (0,13)

                                            0.299 (7,59)
                                            0.291 (7,39)
                                                                        Gage Plane

                                                                        0.010 (0,25)
1   28
                                                              0°−8°
      0.730 (18,54)   0.040 (1,02)
      0.720 (18,29)   0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN   Seating Plane

                                                     ◁ 0.004 (0,10)

4040048−4/F 05/13
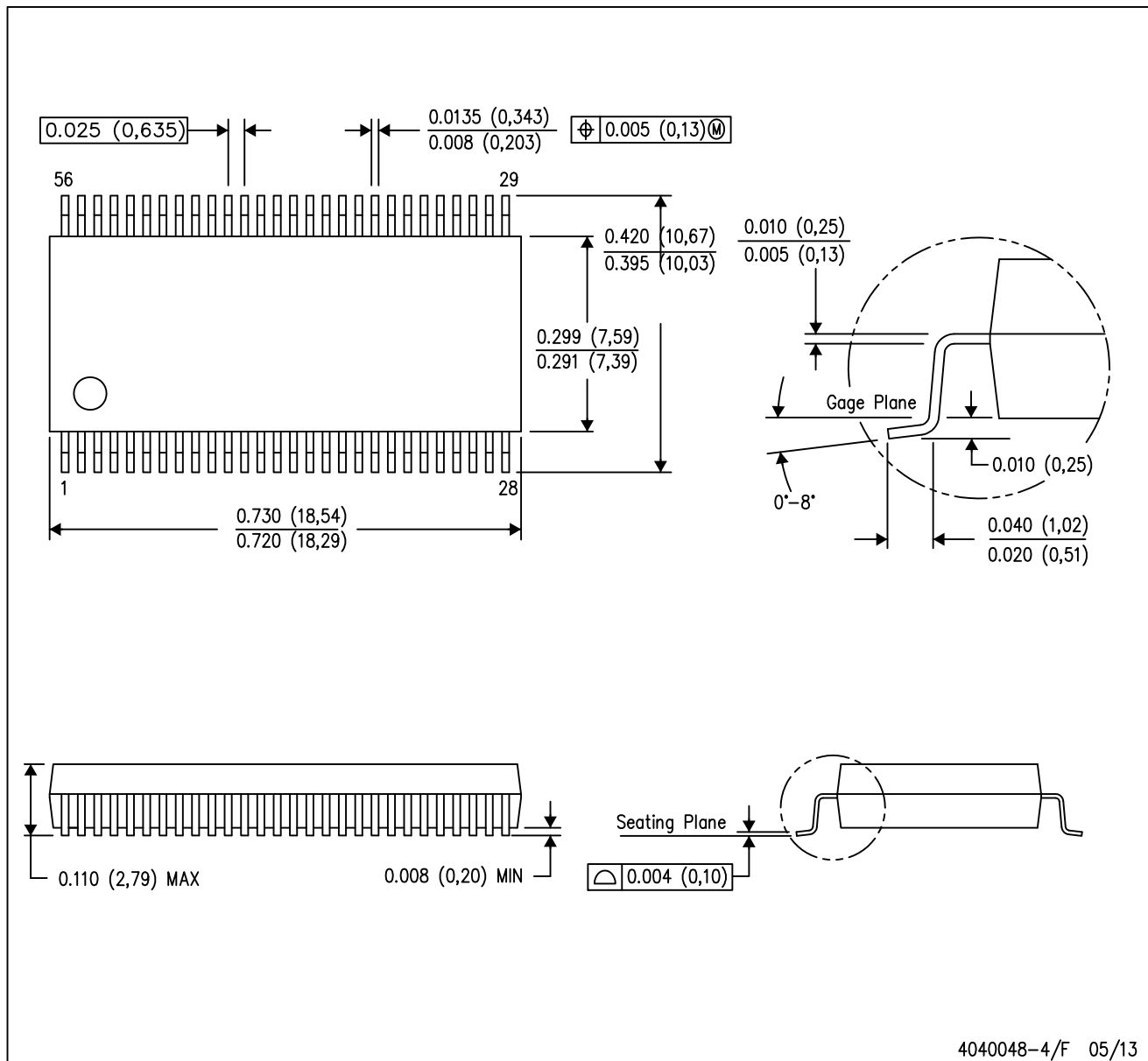
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

8.3
7.9 TYP

A

PIN 1 ID
AREA

1

54X 0.5

56

14.1
13.9
NOTE 3

2X
13.5

28

B

29

6.2
6.0

56X 0.27
0.17

⊕ 0.08 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

⌒ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL
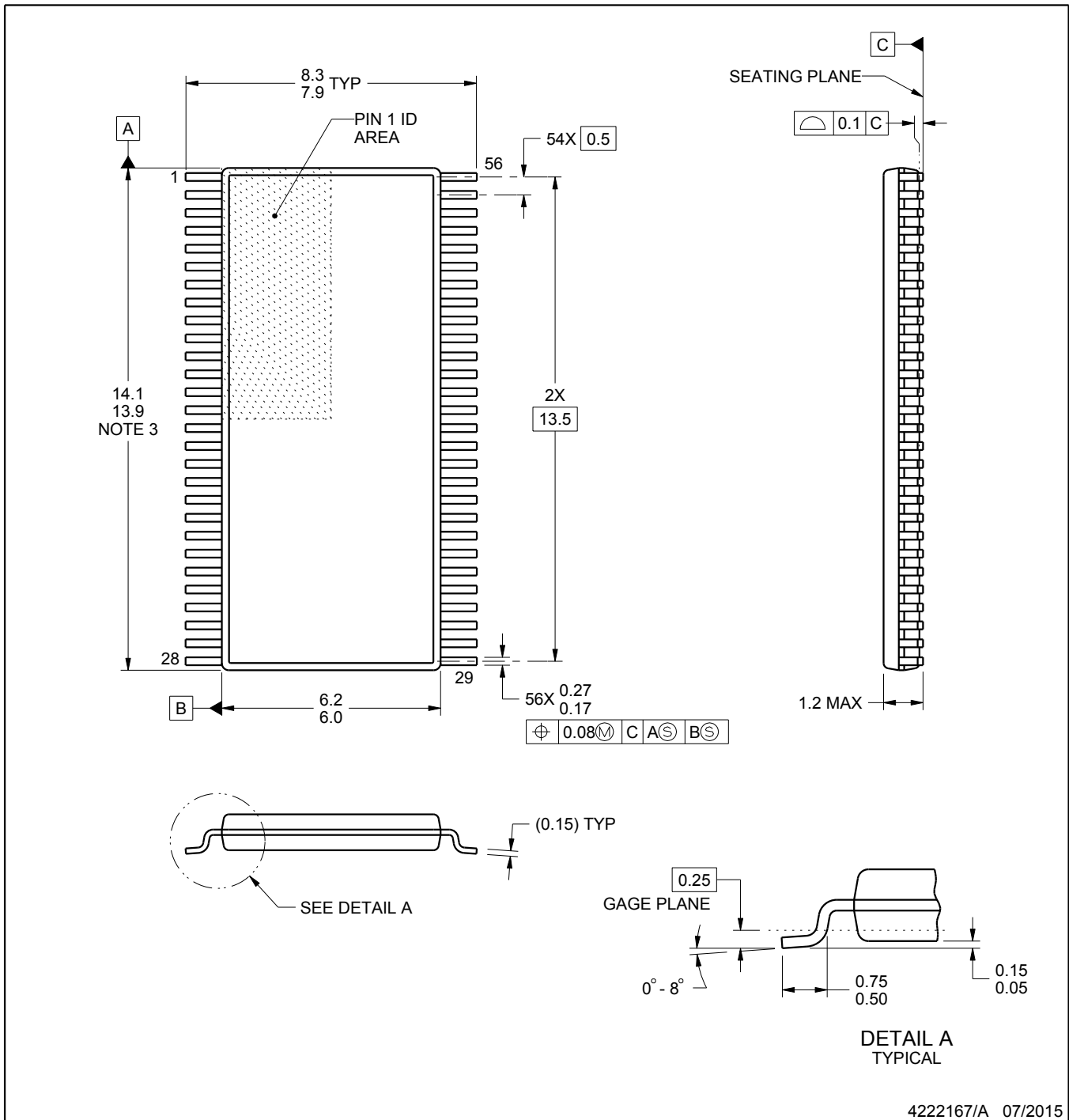
4222167/A   07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

DGG0056A

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

56

SYMM

28

29

(7.5)
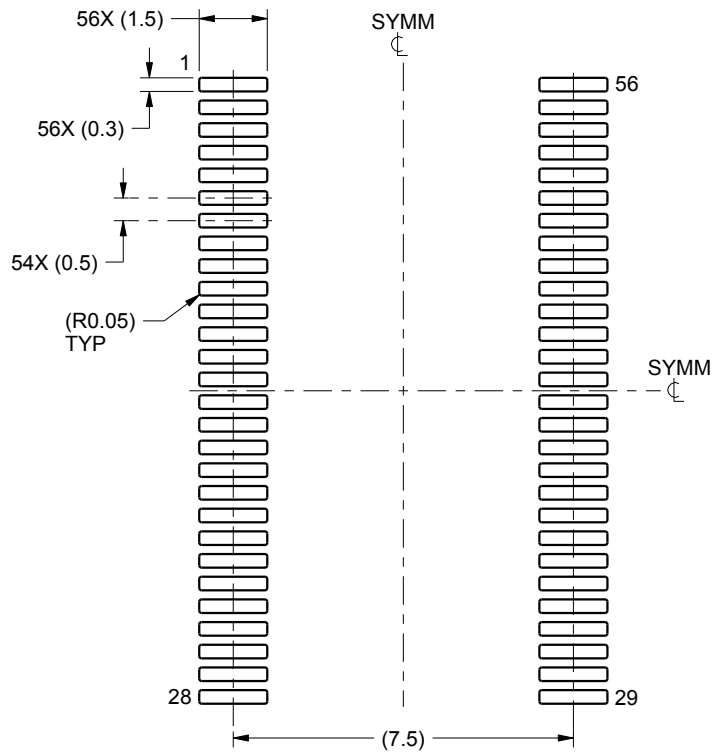
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
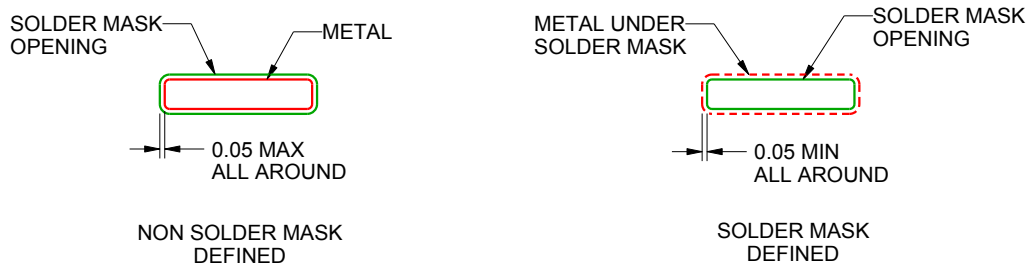
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05) TYP

SYMM
ℂ

56

SYMM
ℂ

28

29

(7.5)
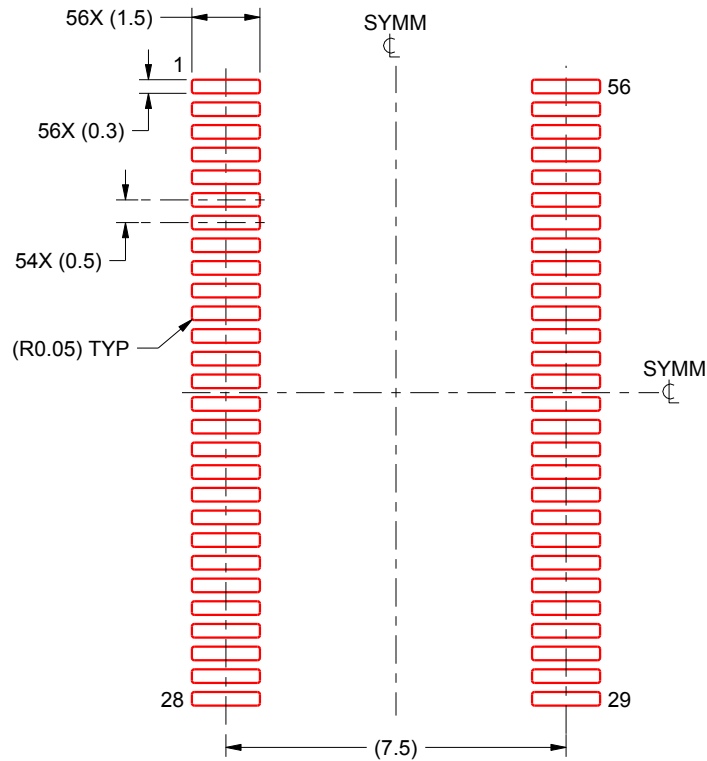
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A   07/2015

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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