AK4564

16bit CODEC with built-in ALC and MIC/HP/SPK-Amp

GENERAL DESCRIPTION

The AK4564 is a 16bit stereo CODEC with a built-in Microphone-Amp, Headphone-Amp and Speaker-Amp. AK4564 has new recording features, a digital equalizer for microphone inputs and a digital ALC (Automatic Level Control). The playback features also include LINEOUT-Amp, digital volume, Headphone-Amp and Speaker-Amp. The AK4564 suits a portable application with a built-in LCD and etc. The AK4564 is housed in a space-saving 48pin LQFP package.

FEATURE

1. **Resolution: 16bits**
2. **Recording Function:**
   - · **4-Input Selector (Internal MIC, External MIC, LINE x 2)**
   - · **Pre-Amp**
   - · **Digital EQ/HPF/LPF**
   - · **Digital ALC (Automatic Level Control) circuit**
   - · **FADEIN / FADEOUT**
   - · **Digital HPF for offset cancellation (fc=3.7Hz@fs=48kHz)**
   - · **Enable mixing of BEEP signal**
3. **Playback Function**
   - · **Digital De-emphasis Filter (tc = 50/15μs, fs = 32kHz, 44.1kHz and 48kHz)**
   - · **LINEOUT-Amp**
   - · **Digital Volume: 0dB ~ - 65.25dB, Mute**
   - · **Headphone-Amp**
     - **Po: 5.3mW @ 16Ω (AVDD = 2.8V)**
   - · **Speaker-Amp with built-in ALC**
     - **BTL Output**
     - **Po: 80mW @ 8Ω**
   - · **Enable mixing of BEEP signal**
4. **Power Management**
5. **ADC characteristics (LIN ® ADC)**
   - · **S/(N+D): 87dB, DR=S/N: 90dB**
6. **DAC characteristics (DAC ® LINEOUT-Amp)**
   - · **S/(N+D): 82dB, DR=S/N: 88dB**
7. **Master Clock: 256fs/384fs**
8. **Sampling Rate: 8kHz ~50kHz**
9. **Audio Data Interface Format: MSB-First, 2's compliment**
   - · **ADC, DAC: 16bit MSB justified, 16bit LSB justified, I^2S**
10. **Ta = -20 ~ 85 °C**
11. **Power Supply Voltage**
    - · **CODEC, Speaker-Amp: 2.6 ~ 3.6V**
    - · **MIC/Headphone/LINEOUT-Amp: 2.6 ~ 5.5V**
12. **Power Supply Current**
    - · **All Power On: 30.5mA**
13. **Package: 48pin LQFP, 0.5mm Pitch**

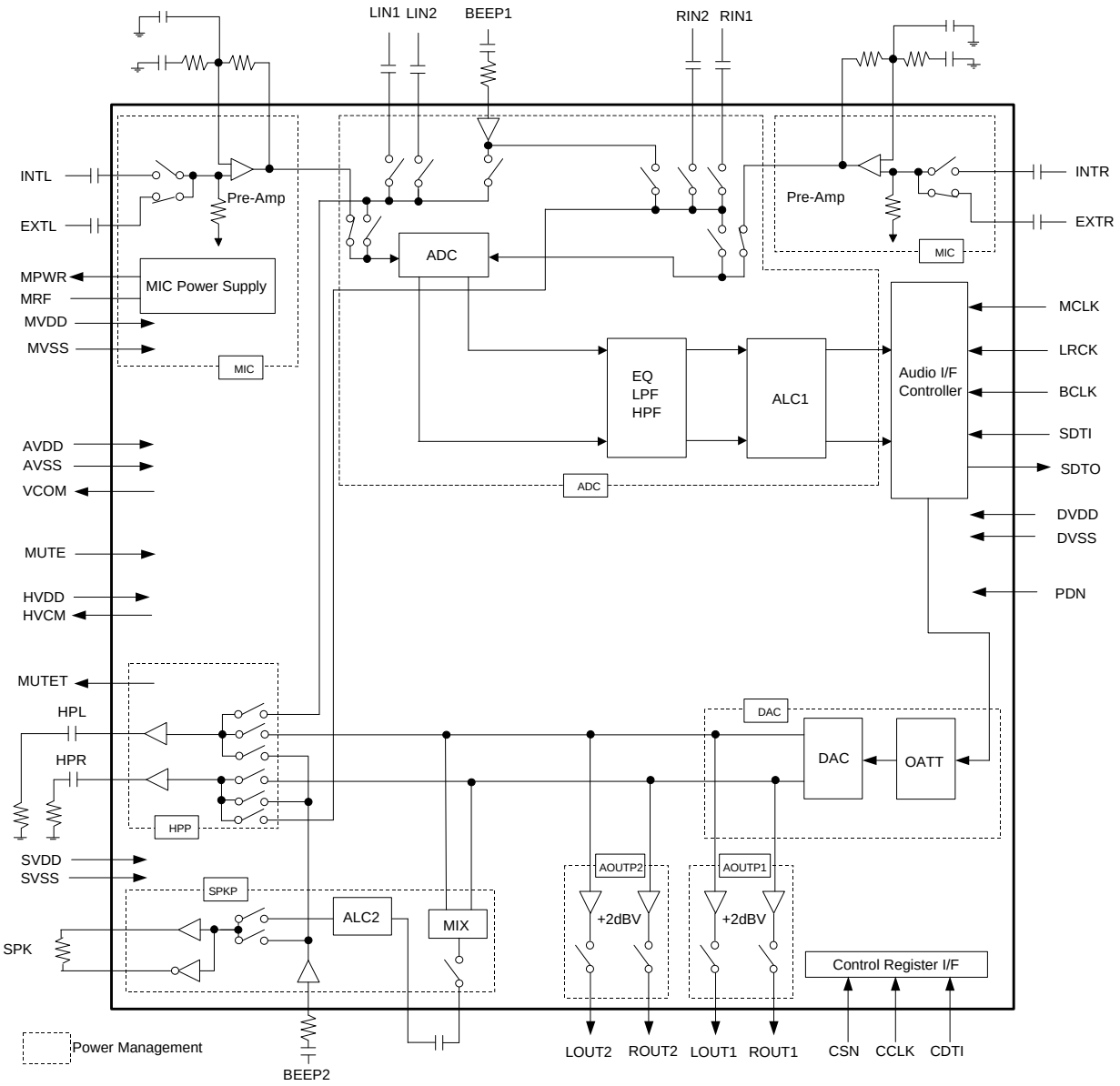


Figure 1. AK4564 block diagram

PIN/FUNCTION

No.	Pin Name	I/O	FUNCTION
Power Supply			
5	SVDD	-	Speaker Amp Power Supply Pin, +3.0V
6	SVSS	-	Speaker Amp Ground Pin
15	DVDD	-	Digital Power Supply Pin, +2.8V
16	DVSS	-	Digital Ground Pin
28	HVDD	-	Headphone-Amp, LINEOUT Power Supply Pin, +4.5V
30	HVCM	O	Headphone-Amp, LINEOUT Common Voltage Output Pin, 0.5 x HVDD
31	AVSS	-	Analog Ground Pin
32	AVDD	-	Analog Power Supply Pin, +2.8V
33	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD
41	MVSS	-	MIC Amp Ground Pin
42	MVDD	-	MIC Amp Power Supply Pin, +2.8V
43	MPWR	O	MIC Power Supply Pin, 1.6V@MVDD=2.8V, Idd=3mA(max)
44	MRF	O	MIC Power Supply Ripple Filter Pin
Operation Clock			
7	BCLK	I	Audio Serial Data Clock Pin
8	MCLK	I	Master Clock Input Pin
9	LRCK	I	Input/Output Channel Clock Pin
13	SDTI	I	Audio Serial Data Input Pin
14	SDTO	O	Audio Serial Data Output Pin
MIC Block			
37	PREOR	O	Rch Pre-Amp Output Pin
38	PRENR	I	Rch Pre-Amp Negative Input Pin
39	EXTR	I	Lch External MIC Input Pin
40	INTR	I	Rch Internal MIC Input Pin
45	INTL	I	Lch Internal MIC Input Pin
46	EXTL	I	Rch External MIC Input Pin
47	PRENL	I	Lch Pre-Amp Negative Input Pin
48	PREOL	O	Lch Pre-Amp Output Pin
Control Data Interface			
10	CDTI	I	Control Data Input Pin
11	CSN	I	Chip Select Pin
12	CCLK	I	Control Clock Input Pin
ADC Block			
17	LIN1	I	Lch Line #1 Input Pin
19	RIN1	I	Rch Line #1 Input Pin
21	LIN2	I	Lch Line #2 Input Pin
23	RIN2	I	Rch Line #2 Input Pin
DAC Block			
18	LOUT1	O	Lch Line #1 Output Pin
20	ROUT1	O	Rch Line #1 Output Pin
22	LOUT2	O	Lch Line #2 Output Pin
24	ROUT2	O	Rch Line #2 Output Pin

NOTE: All digital input pins must not be left floating.

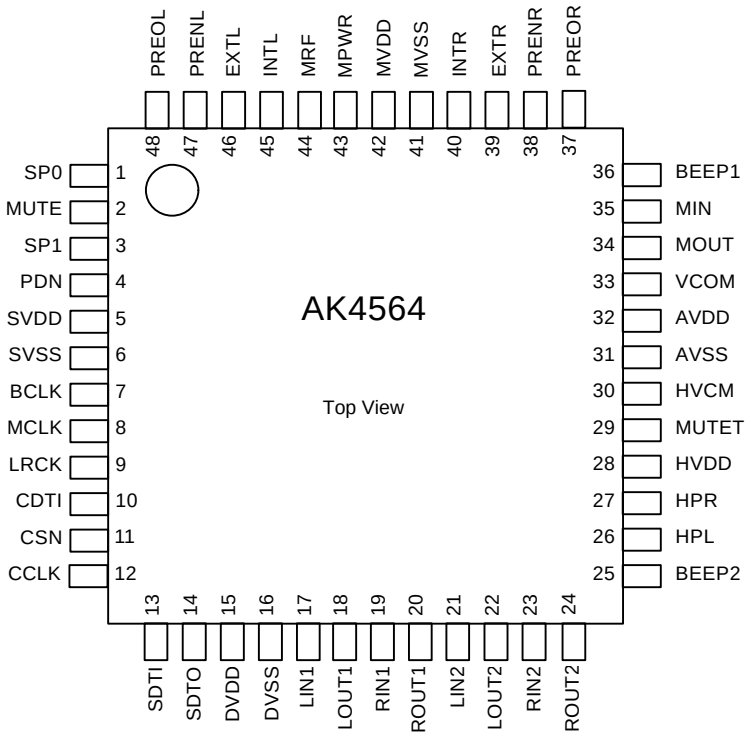
No.	Pin Name	I/O	FUNCTION
Headphone Amp			
26	HPL	O	Lch Headphone Amp Output Pin
27	HPR	O	Rch Headphone Amp Output Pin
29	MUTET	O	Headphone Amp MUTE Capacitor Pin
Speaker Amp Block			
1	SP0	O	Speaker Amp positive Output Pin
3	SP1	O	Speaker Amp negative Output Pin
34	MOUT	O	Analog Mixing Output Pin
35	MIN	I	ALC2 Input Pin
Other Functions			
2	MUTE	I	Mute Pin "L": Normal Operation, "H" MUTE
4	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
25	BEEP2	I	Beep Signal #2 Input Pin
36	BEEP1	I	Beep Signal #1 Input Pin

NOTE: All digital input pins must not be left floating.

■ Ordering Guide

AK4564VQ	-20 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD4564	Evaluation board for AK4564	

■ Pin layout



ABSOLUTE MAXIMUM RATING

(AVSS, DVSS, MVSS, SVSS=0V;Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog 1	AVDD	-0.3	6.0	V
	Analog 2	HVDD	-0.3	6.0	V
	MIC	MVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	Speaker	SVDD	-0.3	6.0	V
	| DVSS – AVSS | (Note 2)	ΔGND1	-	0.3	V
	| MVSS – AVSS | (Note 2)	ΔGND2	-	0.3	V
	| SVSS – AVSS | (Note 2)	ΔGND3	-	0.3	V
Input Current (Any pins except supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA1	-0.3	AVDD+0.3	V
(Note 4)		VINA2	-0.3	MVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	-0.3	DVDD+0.3	V
Ambient Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C
Maximum Power Dissipation	Ta=85°C (Note 7)	Pd1	-	500	mW
(Note 6)	Ta=70°C (Note 8)	Pd2	-	700	mW

Note 1. All voltage with respect to ground.
Note 2. AVSS, DVSS, MVSS and SVSS must be connected to the same analog ground plane.
Note 3. LIN1, RIN1, LIN2, RIN2, BEEP1, BEEP2 and MIN pins
Note 4. EXTL, EXTR, INTL, INTR, PRENL and PRENR pins
Note 5. MCLK, LRCK, BICK, SDTI, PDN, CSN, CCLK, CDTI and MUTE pins
Note 6. Wiring density is 50% or more.
Note 7. **Headphone-Amp and Speaker-Amp shouldn't be powered up at the same time. The maximum power supply voltage of SVDD is 3.3V.**
Note 8. **Headphone-Amp and Speaker-Amp can be powered up at the same time.**

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, MVSS, SVSS=0V;Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog 1	AVDD	2.6	2.8	3.6	V
	Analog 2	HVDD	2.6	4.5	5.5	V
	MIC (Note 9)	MVDD	2.6 or "AVDD – 0.1"	2.8	5.5	V
	Digital	DVDD	2.6	2.8	AVDD	V
	Speaker (Note 10)	SVDD	2.6	3.0	3.3 or 3.6	V

Note 1. All voltage with respect to ground.
Note 9. Minimum value is higher value between 2.6V and "AVDD – 0.1"V.
Note 10. When Ta (max) is 85°C, SVDD (max) is 3.3V. Then Headphone-Amp and Speaker-Amp shouldn't be powered up at the same time.
When Ta (max) is 70°C, SVDD (max) is 3.6V. Then Headphone-Amp and Speaker-Amp can be powered-up at the same time.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, MVDD=2.8V, SVDD=3.0V, HVDD=4.5V; AVSS, DVSS, MVSS, SVSS=0V; fs=48kHz; Input Frequency =1kHz; Measurement width=20Hz ~ 20kHz, unless otherwise specified)

Parameter	min	typ	Max	Units
Pre-Amp Characteristics:				
Input Resistance (INTL, INTR, EXTL, EXTR pins)	70	100	130	kΩ
Maximum Output Voltage (Note 11)			-4.5	dBV
Gain	+18	+24	+30	dB
Load Resistance (Note 12)	3		30	kΩ
Load Capacitance (Note 13)			10	pF
MIC Power Supply Voltage Characteristics: MPWR pin				
Output Voltage (Output current = 0mA) (Note 14)	1.4	1.6	1.8	V
Maximum Output Current			3	mA
ADC Analog Input Characteristics: ALC1 = OFF				
Resolution			16	bits
Input Resistance (LIN1, RIN1, LIN2, RIN2 pins)	70	100	130	kΩ
Input Voltage (Note 15) (Note 16)	-5.1	-4.3	-3.5	dBV
(Note 15) (Note 17)	-58.5	-57.7	-56.9	dBV
S/(N+D) (-0.5dBFS) (Note 16)	78	88		dB
(Note 18)	75	85		dB
DR (-60dBFS, A-Weighted) (Note 16)	84	90		dB
(Note 17)	57	61		dB
S/N (A-Weighted) (Note 16)	84	90		dB
(Note 17)	57	61		dB
Interchannel Isolation (Note 16)	80	100		dB
(Note 17)	50	70		dB
Interchannel Gain Mismatch (Note 16)			0.5	dB
(Note 17)			0.5	dB

Note 11. Maximum output voltage is (0.6 x AVDD) Vpp.
Note 12. Load resistance is the value of "Rf + Ri". (Refer to Figure 12)
Note 13. When the output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.
Note 14. When the output current is 0mA, the output voltage of MPWR pin is typically (MVDD – 1.2) V at MVDD=2.8V and typically (MVDD-1.4) V at MVDD=4.5V.
When the output current is 3mA, the output voltage of MPWR pin is typically (MVDD – 1.5) V at MVDD=2.8V and typically (MVDD-1.7) V at MVDD=4.5V.
Note 15. Input voltages are proportional to AVDD voltage.
LIN1, RIN1, LIN2, RIN2 = (0.62 x AVDD) Vpp
INTL, INTR, EXTL, EXTR = (0.0013 x AVDD) Vpp
Note 16. Input from LIN1, RIN1, LIN2 or RIN2 pins. IVOL=0dB.
Note 17. Input from INTL, INTR, EXTL or EXTR pins. Pre-Amp Gain = + 23.9dB, PRE = "1", IVOL = +29.625dB
External resistor of Pre-Amp is "Rf = 10kΩ, Ri = 680Ω". (Refer to Figure 12)
Note 18. Input from INTL, INTR, EXTL or EXTR pins. Pre-Amp Gain = + 23.9dB, PRE = "1", IVOL = +0dB
External resistor of Pre-Amp is "Rf = 10kΩ, Ri = 680Ω". (Refer to Figure 12)

*** 0dBV = 1Vrms = 2.83Vpp**

(Continue)

Parameter	min	typ	max	Units
DAC Analog Output characteristics: Measured via LOUT1/ROUT1, LOUT2/ROUT2, VOL=+6.5dB				
Resolution			16	bits
S/(N+D) (0dBFS)	76	82		dB
DR (-60dBFS, A-Weighted)	82	88		dB
S/N (A-Weighted)	82	88		dB
Output Voltage (Note 19)	+1.2	+2	+2.8	dBV
Interchannel Isolation	80	100		dB
Interchannel Gain Mismatch			0.5	dB
Load Resistance	10			kΩ
Load Capacitance (Note 13)			30	pF
Headphone-Amp Characteristics: DAC → HPL/HPR pin				
Output Voltage (Note 20) HVDD = 3V	-5.5	-4.7	-3.9	dBV
(Note 21) HVDD = 4.5V	-1.1	-0.3	+0.5	dBV
S/(N+D) (Note 20) HVDD = 3V	50	70		dB
(Note 21) HVDD = 4.5V	50	66		dB
Output Noise Voltage (A-Weighted);				
HPG="0", HVDD=3V, R_L=32Ω		-92	-86	dBV
HPG="1", HVDD=4.5V, R_L=100Ω		-77	-71	dBV
Interchannel Isolation; HPG="0", HVDD=3V, R_L=32Ω	60	80		dB
HPG="1", HVDD=4.5V, R_L=100Ω	60	80		dB
Interchannel Gain Mismatch; HPG="0", HVDD=3V, R_L=32Ω			0.5	dB
HPG="1", HVDD=4.5V, R_L=100Ω			0.5	dB
Load Resistance; HVDD=2.6~3.6V, HPG = "0"	22			Ω
HVDD=4.0~5.5V, HPG = "1"	100			Ω
Load Capacitance (C1 in Figure 2)			30	pF
(C2 in Figure 2)			6.8	nF
Speaker-Amp Characteristics: R_L = 8Ω, BTL, MIN → SP0/SP1, ALC2 = OFF				
Output Voltage (-6.5dBV Input)	-4	-2	0	dBV
S/(N+D) (-2dBV Output)	30	60		dB
S/N (A-Weighted)	81	89		dB
Load Resistance	8			Ω
Load Capacitance			10	pF

Note 19. Output voltages are proportional to AVDD voltage.
LOUT1, ROUT1, LOUT2, ROUT2 = (1.27 x AVDD) Vpp @VOL = +6.5dB

Note 20. When DAC = 0dBFS Output, OATT = 0dB, HPG = "0", R_L = 32Ω, the output voltage is (0.59 x AVDD) Vpp.

Note 21. When DAC = -12dBFS Output, OATT = 0dB, HPG = "1", R_L = 100Ω, the output voltage is (0.98 x AVDD) Vpp.

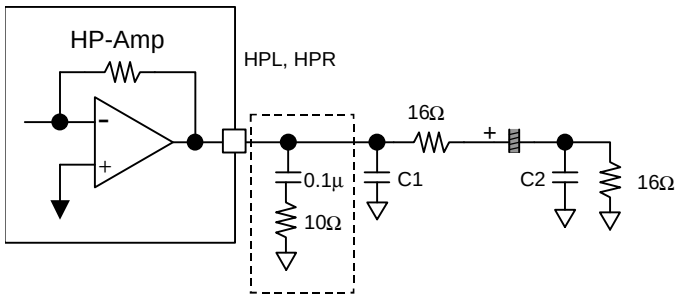


Figure 2. Headphone-Amp Output Circuit

*** 0dBV = 1Vrms = 2.83Vpp**

(Continue)

Parameter	min	typ	max	Units
Monaural Input: (MIN pin)				
Maximum Input Voltage (Note 22)			-4.5	dBV
Input Resistance	14	23	33	kΩ
Monaural Output: DAC → MIX → MOUT pin				
Output Voltage (Note 23)	-5.3	-4.5	-3.7	dBV
Load Resistance	10			kΩ
Load Capacitance (Note 13)			30	pF
BEEP1 Input: BEEP1 pin				
Maximum Output Voltage of Internal Amplifier (Note 24)			-4.5	dBV
Feed-back Resistance	14	20	26	kΩ
BEEP2 Input: BEEP2 pin				
Maximum Output Voltage of Internal Amplifier (Note 24)			-4.5	dBV
Feed-back Resistance	14	20	26	kΩ
Power Supply Current				
Power Up (PDN = "H")				
All Circuit Power-Up: (MIC=ADC=DAC=VCOM=HPP=SPKP=AOUTP1=AOUTP2= "1")				
AVDD+DVDD		13	19.5	mA
MVDD (Note 25)		4.5	6.8	mA
HVDD: HP-Amp Normal operation (AOUTP2,1 = "1", HP-Amp No output)		6.5	9.8	mA
SVDD: SPK-Amp Normal operation (SPPS= "1", SPK-Amp No output)		6.5	9.8	mA
ADC: (ADC=VCOM= "1") (Note 26)				
AVDD+DVDD		7.5	-	mA
DAC+LINEOUT: (DAC=AOUTP1=AOUTP2=VCOM= "1")				
AVDD+DVDD		5.5	-	mA
HVDD: LINEOUT Normal operation, HP-Amp Power OFF (AOUT1,2= "1", HPP = "0")		2.5	-	mA
Power Down (PDN= "L")				
AVDD+DVDD+HVDD+MVDD+SVDD (Note 27)			200	μA

Note 22. Maximum input voltage is proportional to AVDD voltage. (0.6 x AVDD) Vpp
Note 23. DAC 0dBFS Output (Both L/R channels and the same phase) and OATT = 0dB.
Note 24. Maximum output voltage is proportional to AVDD voltage. (0.6 x AVDD) Vpp
Note 25. MPWR pin supplies 0mA.
Note 26. As VCOM bit = "1", power supply current of HVDD is 0.8mA (typ.).
Note 27. In power-down, all digital input pins including clock (MCLK, BCLK and LRCK) pins are held at "DVDD" or "DVSS". PDN pin is held at "DVSS".

*** 0dBV = 1Vrms = 2.83Vpp**

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V; fs=48kHz; De-emphasis = OFF, Digital EQ/HPF/LPF = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 28)	±0.1dB	PB	0		18.9	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 28)		SB	29.4			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 29)		GD	-	19.0	-	1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 28)	-3.0dB	FR	-	3.7	-	Hz
	-0.56dB		-	10	-	Hz
	-0.15dB		-	20	-	Hz
DAC Digital Filter:						
Passband (Note 28)	±0.1dB	PB	0		21.7	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 28)		SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 29)		GD	-	15.8	-	1/fs
DAC Digital Filter + Analog Filter: (Note 30)						
Frequency Response	0 ~ 20.0kHz	FR		±0.5		dB

Note 28. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.1dB).

Note 29. The calculated delay time caused by digital filtering. This time is from the input of an analog signal to setting the 16bit data of both channels to the output register of the ADC and includes the group delay of the HPF.
For DAC, this time is from setting the 16bit data of both channels on input register to the output of analog signal.

Note 30. DAC → LOUT1/ROUT1, LOUT2/ROUT2

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	1.5	-	-	V
Low-Level Input Voltage	VIL	-	-	0.6	V
High-Level Output Voltage Iout=-200μA	VOH	DVDD-0.2	-	-	V
Low-Level Output Voltage Iout=200μA	VOL	-	-	0.2	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHRACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=2.6 ~ 3.6V, MVDD, HVDD=2.6~ 5.5V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (MCLK)					
256fs: Frequency	fCLK	2.048	12.288	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	18.432	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Timing					
Frequency	fs	8	48	50	kHz
Duty Cycle	Duty	45	50	55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
LRCK Edge to BCLK "↑" (Note 31)	tLRB	50			ns
BCLK "↑" to LRCK Edge (Note 31)	tBLR	50			ns
LRCK to SDTO (MSB) Delay Time	tLRM			80	ns
BCLK "↓" to SDTO Delay Time	tBSD			80	ns
SDTI Latch Hold Time	tSDH	50			ns
SDTI Latch Set up Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Latch Set up Time	tCDS	50			ns
CDTI Latch Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width	tPDW	150			ns
PDN "↑" to SDTO Delay Time	tPDV		4128		1/fs

Note 31. BCLK rising edge must not occur at the same time as LRCK edge.

■ **Timing Diagram**

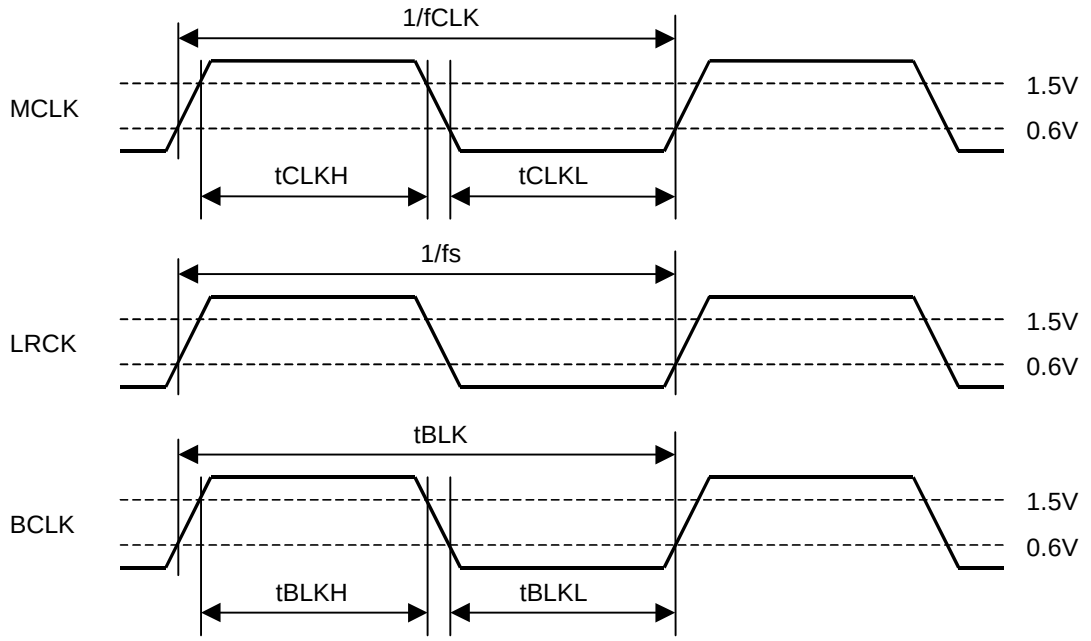


Figure 3. Clock Timing

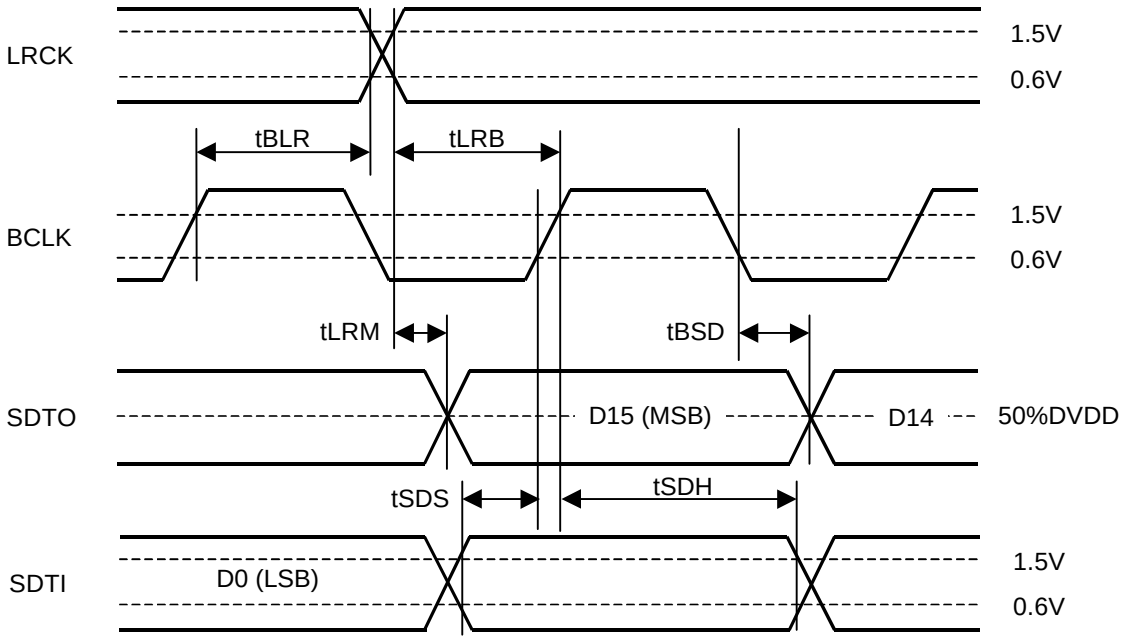


Figure 4. Audio Data Input/Output Timing (Audio I/F format: No. 0)

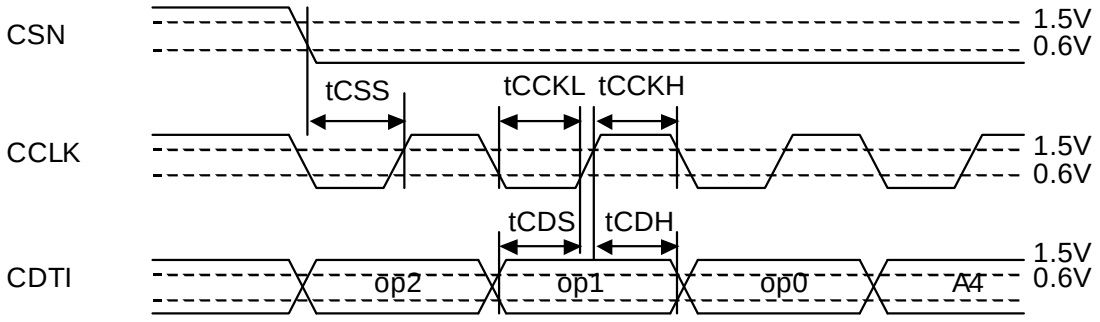


Figure 5. WRITE Command Input Timing

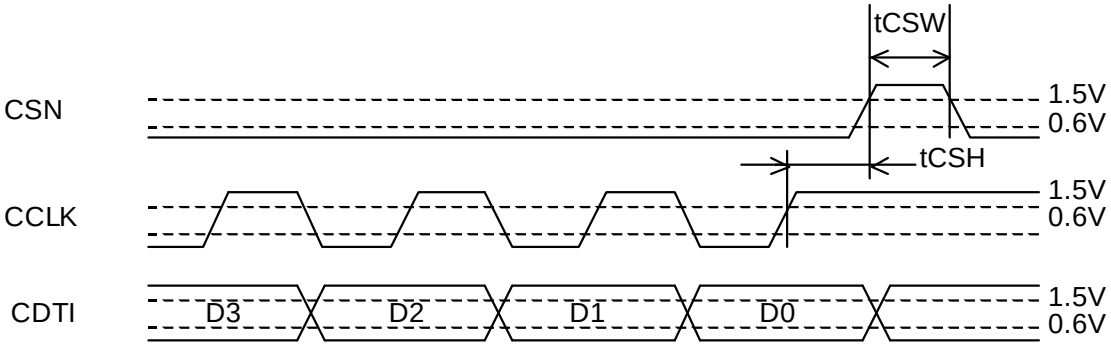


Figure 6. WRITE Data Input Timing

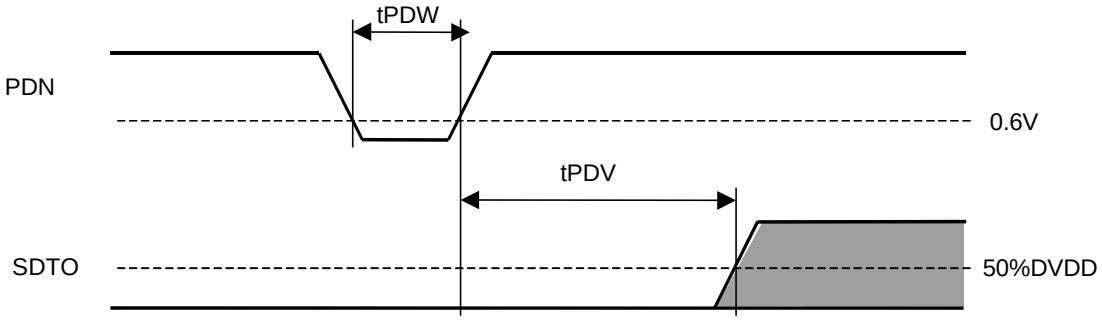


Figure 7. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter. The frequency of MCLK can be input as 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically.
*fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4564 may occur click noise. DAC input data should be “0” to avoid click noise.

All external clocks (MCLK, BCLK and LRCK) should always be present except MIC = ADC = DAC = VCOM = HPP = SPKP = AOUT1P = AOUT2P = “0” or PDN = “L”. If these clocks are not provided, the AK4564 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4564 should be placed in MIC = ADC = DAC = VCOM = HPP = SPKP = AOUT1P = AOUT2P = “0” or PDN = “L”. However, ADC, DAC and ALC2 are in power-down mode until MCLK, BCLK and LRCK is input, even if they release a power-down mode by PDN pin or control register. (Refer to the “Power Management Mode”.)

■ System Reset

AK4564 should be reset once by bringing PDN pin “L” upon power-up. After the system reset operation, the all internal registers become initial value.

Initializing cycle is 4128/fs=86ms@fs=48kHz. During initializing cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, “0”. Output data of ADC settles data equivalent for analog input signal after initializing cycle. This cycle is not for DAC.

■ Digital High Pass Filter

The AK4564 has a Digital High Pass Filter (HPF) to cancel DC-offset in ADC. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and it is attenuated to –0.15dB at 20Hz. This cut-off frequency scales with the sampling frequency (fs).

■ Audio Serial Interface Format

The SDTI, SDTO, BCLK and LRCK pins are connected to an external controller. The audio data format has four modes, MSB-first and 2's compliment. The data format is set by the DIF1-0 bits. SDTI is latched by "↑" of BCLK. SDTO is latched by "↓".

When DIF1= "0" and DIF0="1", only BCLK=64fs is acceptable.

No.	DIF1 bit	DIF0 bit	SDTO(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 8	RESET
1	0	1	LSB justified	LSB justified	= 64fs	Figure 9	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 10	
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 11	

Table 1. Audio Data Format

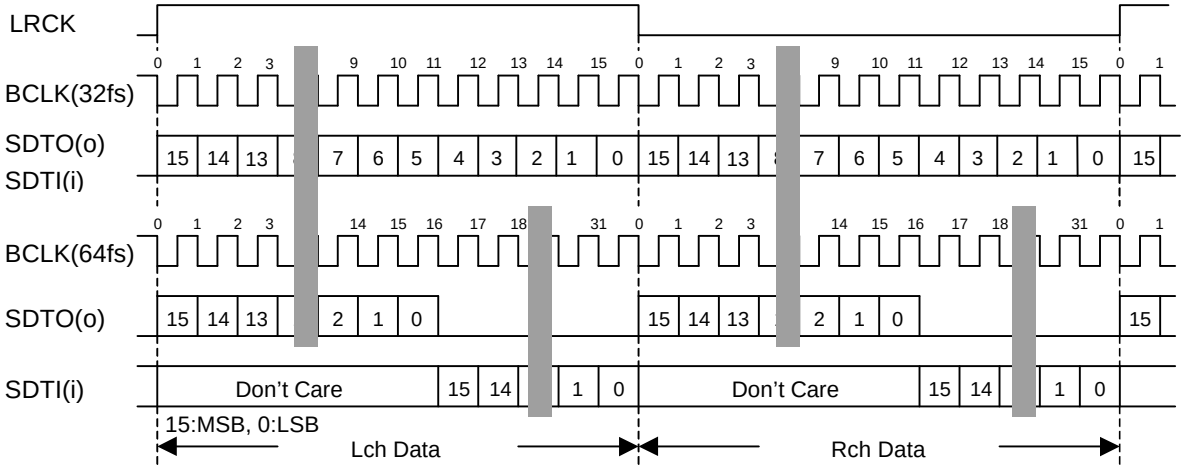


Figure 8. Audio Data Timing (No.0)

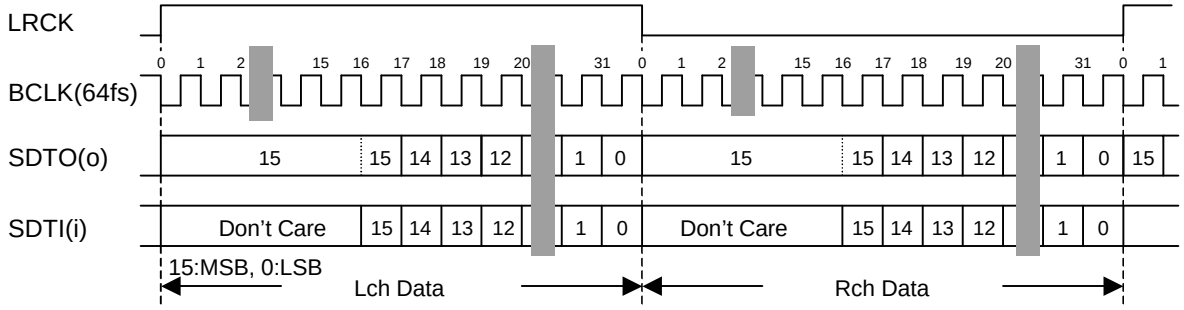


Figure 9. Audio Data Timing (No.1)

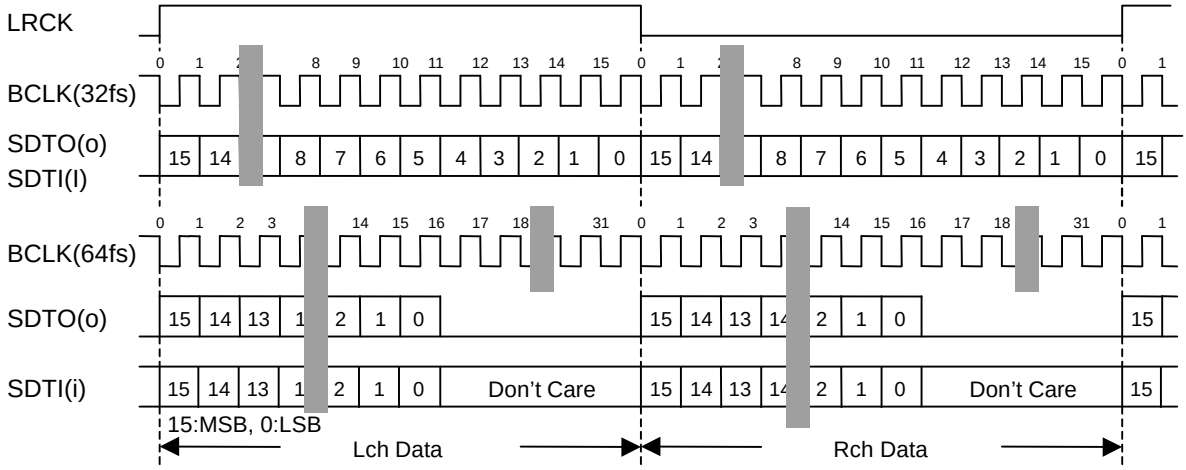


Figure 10. Audio Data Timing (No.2)

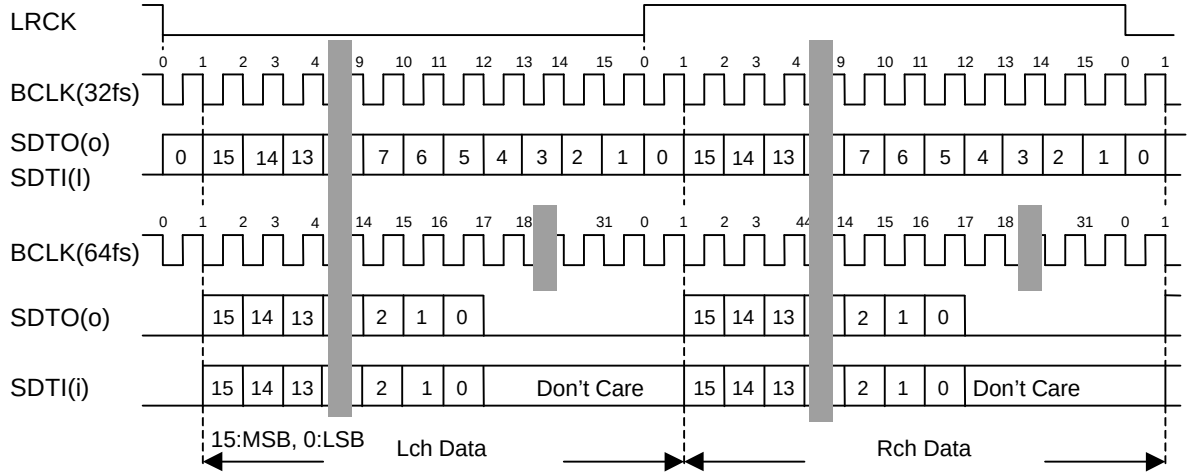


Figure 11. Audio Data Timing (No.3)

■ MIC BLOCK

1. Pre- Amp

Pre-Amp includes selector, Internal MIC or External MIC Mode can be selected by INT/EXT bit. The Pre-Amp is non-inverting amplifier and internally biased to VCOM voltage with 100kΩ (typ.). Gain (1+Rf/Ri) of the Pre-Amp is adjusted by external resistors and should be a range of +18 ~ +30dB.

An external capacitor is needed to cancel DC gain. The Cut-off frequency is determined by an external resistor (Ri) and a capacitor (C1).

A capacitor of 100pF (C2) should be connected to prevent oscillation of Pre-Amp.

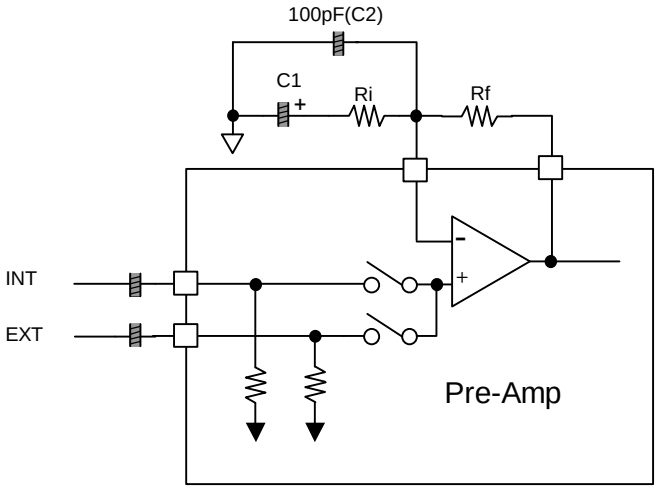


Figure 12. Pre-Amp

2. Power Supply for MIC

The Power Supply for microphone device is supplied from MPWR pin. MPWR pin can supply the current up to 3mA. When the output current is 0mA, the output voltage is typically (MVDD – 1.2) V at MVDD=2.8V and typically (MVDD – 1.4) V at MVDD=4.5V. When the output current is 3mA, the output voltage is typically (MVDD – 1.5) V at MVDD=2.8V and typically (MVDD – 1.7) V at MVDD=4.5V. When MIC bit is “0”, the output current is not supplied.

■ Analog Mixing Circuit for Recording Block

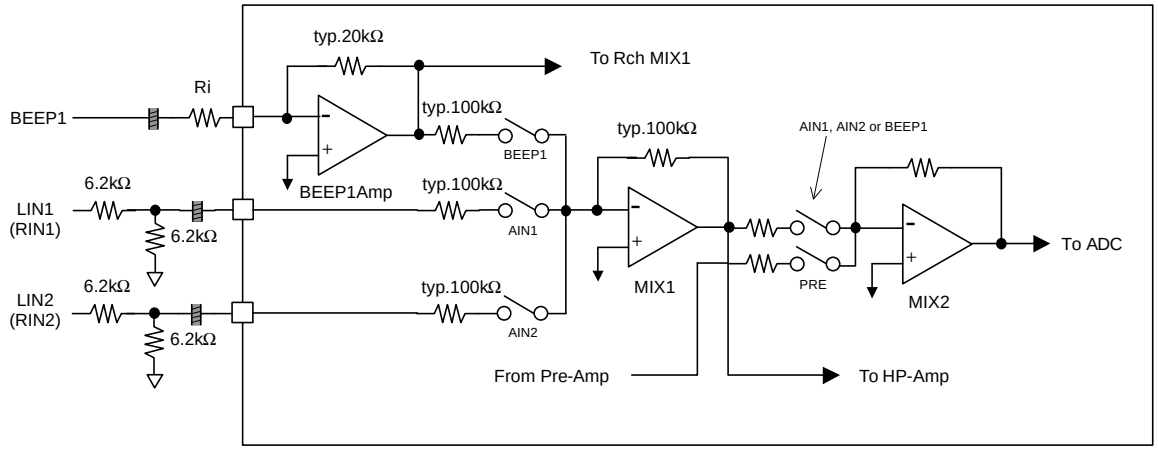


Figure 13. Analog Mixing Circuit for Recording Block

1. BEEP1 Input

When BEEP1 bit is "1", the input signal via BEEP1 pin can be applied to ADC. This signal level can be adjusted by an external resistor (Ri). Feed-back resistor of BEEP1-Amp is 20k ± 30% Ω. (Refer to Figure 13)

2. LINE Input

Input resistance of LIN1, RIN1, LIN2 and RIN2 are typically 100kΩ and centered around the VCOM voltage. When the input voltage exceeds +2dBV, the input signals should be attenuated down to –4.3dBV at VA=2.8V by external resistor divider.

When AIN1 bit is "1", LIN1 and RIN1 pins are selected. When AIN2 bit is "1", LIN2 and RIN2 pins are selected. If AIN1 and AIN2 bits are selected at the both input signals are mixed by the ratio of "1:1"

3. MIX1-Amp

MIX1-Amp is powered-up when ADC bit = "1" or MIX1P bit = "0".

4. MIX2-Amp

MIX2-Amp mixes Pre-Amp output and MIX1-Amp output at the ratio of "1:1".

5. Polarity

Input signals from INTL/INTR, EXTL/EXTR and BEEP1 pins are inverted and are output from ADC. Input signals from LIN1/RIN1 and LIN2/RIN2 pins are non-inverted and output from ADC.

Signal Path	Polarity
INTL/INTR → ADC	Inverted
EXTL/EXTR → ADC	Inverted
BEEP1 → ADC	Inverted
LIN1/RIN1 → ADC	Non-inverted
LIN2/RIN2 → ADC	Non-inverted

Table 2. Polarity of Recording Block

6. MONO Mode

When MONO bit is "1", the recording blocks in the AK4564 becomes MONO mode. The Pre-Amp, MIX1-Amp, MIX2-Amp and ADC analog block of the right channel are powered-down. And the right channel data of ADC is the same as the left channel data of ADC. When changing MONO mode, the ADC should be powered-up by changing ADC bit = "1" after MONO bit is changed to "1". Because click noise may occur when MONO bit is changed during ADC normal operation.

■ BEEP2 Input

When BEEP2H bit is "1", the input signal from BEEP2 pin is output to Headphone-Amp. When BEEP2S bit is "1", the input signal from BEEP2 pin is output to Speaker-Amp.

This signal level can be adjusted by an external resistor (Ri). An internal resistor value (Rf) is 20k ± 30% Ω. In Speaker-Amp, the signal level is gained to +4.6dB internally.

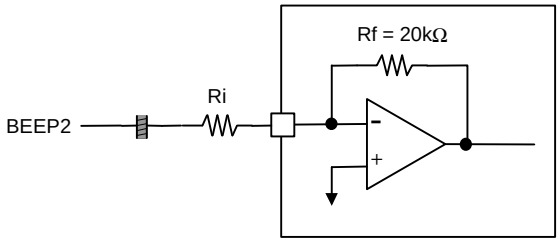


Figure 14. Block diagram of BEEP2 inputs

■ MUTE Function

When MUTE pin is "H", the output signals of LINEOUT, Headphone and Speaker-Amp are muted, and become VCOM or HVCM voltage. The switches of AOUT1, AOUT2, HPDAC, HPMIX, BEEP2H, ALCS and BEEP2S become "OFF" at the same time.

■ Output Digital Volume (OATT)

Attenuation range of the output digital volume is 0dB to -65.25dB with MUTE, and the step width is 0.75dB. When ZEC bit is “1”, the attenuation level is changed by zero crossing detection or zero crossing timeout operation. Zero crossing timeout period is set by TM1-0 bits and FSTM bit. When ZCE is “0”, it is changed immediately without zero crossing detection.

Channel independent zero crossing detection is used. If new value is written to the OATT register before OATT changes by zero crossing or timeout, the previous value becomes invalid. When the OATT register is written continually, it should take an interval of zero crossing timeout and over.

■ LINEOUT

LINEOUT signals are output from LOUT1/ROUT1 and LOUT2/ROUT2 pins. The output gain is set by VOL1 and VOL2 bits. The common voltage of these outputs is HVCM voltage and load resistance is min. 10kΩ. The Power supply voltage for LINEOUT-Amp is supplied from HVDD pin. The output level of LINEOUT is constant regardless of HVDD voltage. When the voltage of HVDD pin is low, the distortion of LINEOUT degrades.

When LINEOUTs are muted by AOUT1 or AOUT2 bit, the outputs become HVCM voltage and the amps go to Power-Save-Mode. When AOUTP1 (AOUTP2) bit is “0”, LINEOUT-Amps become Power-Down-Mode and the output signal goes to Hi-Z.

When PDN pin changes from “L” to “H” after power-up, LINEOUT-Amps become Power-Save-Mode. In Power-Save-Mode, LOUT1/ROUT1 (LOUT2/ROUT2) pins gradually become HVCM voltage via an internal resistor (typ.200kΩ) from Hi-Z to decrease a pop noise. When Power OFF, the pop noise can be decreased by using Power-Save-Mode.

■ Headphone-Amps

The Power supply voltage for Headphone-Amp is supplied from HVDD pin and centered around HVCM voltage. The load resistance and output voltage are specified by HVDD voltage. The output voltage can be changed by supplying AVDD voltage and HPG bit. (Refer to Table 3)

HVDD	2.6 ~ 3.6V	4.0 ~ 5.5V
HPG bit	0	1
Output Voltage	(0.59 x AVDD) Vpp	(0.98 x AVDD) Vpp
Load Resistance (min)	22Ω	100Ω

Table 3. Load resistance and output voltage of Headphone-Amp

When HPG bit is "0", the signals from MIX1, DAC and BEEP2 are output from Headphone-Amps with 0dB gain. When HPG is "1", the signals from MIX1, DAC and BEEP2 output from Headphone-Amps with +16.5dB gain. (Refer to Figure 15)

When HPDAC, HPMIX and BEEP2H bits are "0", the input signals to Headphone-Amp are disabled and HPL/HPR pins output HVCM voltage.

HPMIX, HPDAC and BEEP2H bits control ON/OFF of each input signal. When these bits are "1" at the same time, all input signals are mixed by the ration of "1:1". (Refer to Figure 13 and Figure 16)

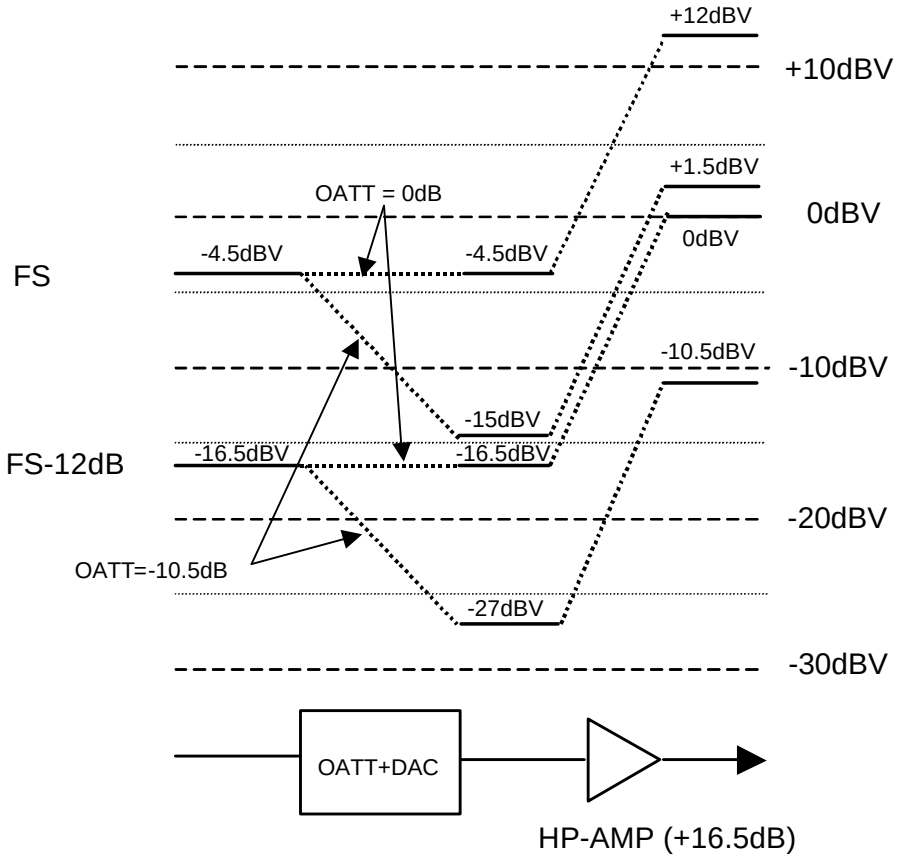


Figure 15. Headphone-Amp Level Diagram (AVDD=2.8V, HVDD=4.5V, HPG = "1", OATT = 0dB& -10.5dB)
* FS = Full Scale

Headphone-Amps are powered-up/down by HPP bit. When HPP bit is "0", Headphone-Amps are powered-down and HPL and HPR pins are fixed to "L" (AVSS). At power-up/down, the common voltage of HPL/HPR pin is settled by a constant which determined by the internal resistor and the external capacitors. The internal resistor is 50kΩ(typ) at power-up, and 1kΩ(typ) at power-down. (Refer to Figure 16)

Rising Time of Headphone-Amp: τ1 = 50kΩ x C1
Falling Time of Headphone-Amp: τ2= 1kΩ x (C1 + 2 x C2)

For example; C1 = 4.7μF, C2 = 100μF

τ1 = 235ms
τ2 = 205ms

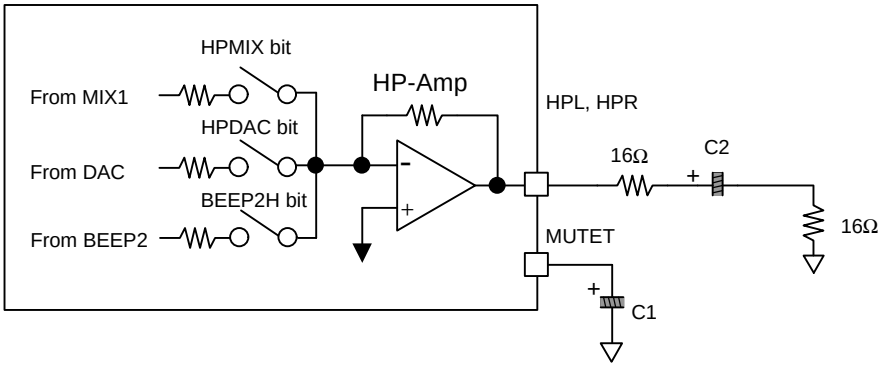


Figure 16. Headphone-Amp internal equivalent circuit

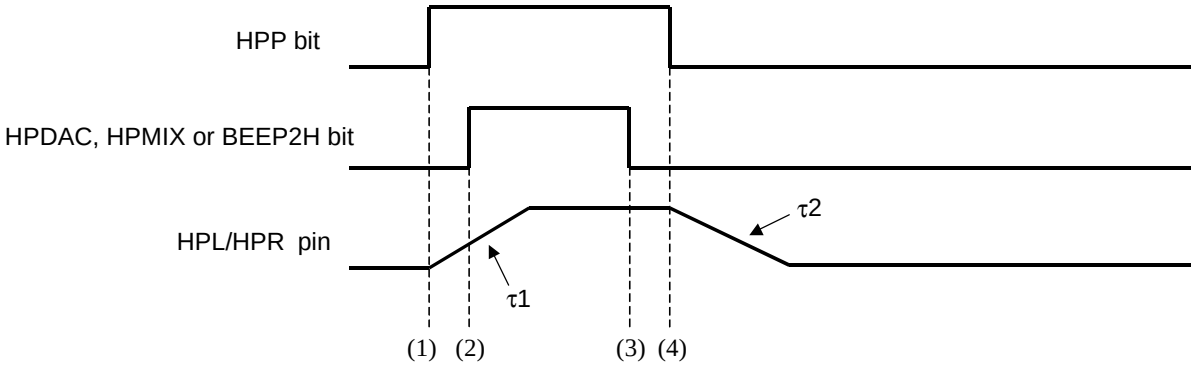


Figure 17. Headphone-Amp Power-Up/Down Timing

(1) Power-up Headphone-Amps: WR (HPP= "1")
The common voltage of HPL/HPR pins rises by the time constant. (τ1)
(2) Enable Headphone-Amp inputs: WR (HPDAC, HPMIX or BEEP2H ="1")
The input signals from MIX1, DAC and BEEP2 are output. Headphone-Amps can output the signals while the common voltage is rising.
(3) Disable Headphone-Amp inputs: WR (HPDAC=HPMIX=BEEP2H="0")
The input signal from MIX1, DAC and BEEP2 are muted. Headphone-Amps output HVCM voltage during muting.
(4) Power-down Headphone-Amps: WR (HPP="0")
The common voltage of HPL/HPR pins falls by the time constant. (τ2)

Headphone-Amps of the AK4564 has a possibility of oscillation depending on headphone characteristics. Therefore, Headphone-amp oscillation prevention circuit may be needed. Headphone-Amps oscillation prevention circuit example is shown in Figure 18.

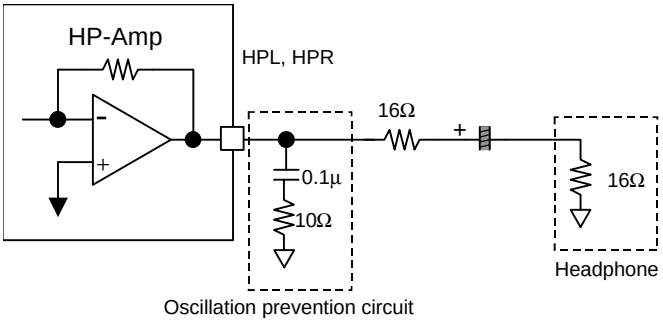


Figure 18. Headphone-Amp oscillation prevention circuit example

*** When Headphone-Amp and Speaker-Amp are powered-up at the same time, refer to the condition of "Note 7", "Note 8" and "Note 10".**

■ SPEAKER BLOCK

The output signal from DAC is converted into a mono signal, [(L+R)/2], and is supplied to Speaker-Amp via ALC2 circuit. This Speaker-Amp has a monaural output by BTL, which can be output up to 80mW at 8Ω. Speaker Blocks (MOUT, ALC2 and Speaker-Amp) can be powered-up/down by SPKP bit. When SPKP bit is "0", MOUT, SP0 and SP1 pins go Hi-Z. When SPPS bit is "0" and SPKP bit is "1", Speaker-Amp becomes Power-Save-Mode. Then SP0 pin goes Hi-Z and SP1 pin is output to SVDD/2 via 100k Ω (typ.).

When PDN pin changes from "L" to "H" after power-up, Speaker-Amp goes to Power-Save-Mode. In Power-Save-Mode, SP1 pin gradually become HVCM voltage via an internal resistor (typ.200kΩ) from Hi-Z to decrease a pop noise. When Power-down (SPKP = "0"), the pop noise can be decreased by controlling via Power-Save-Mode.

*** When Headphone-Amp and Speaker-Amp are powered-up at the same time, refer to the condition of "Note 7", "Note 8" and "Note 10".**

1. Mono Output

MOUT pin outputs analog mixed signal, [(L+R)/2] of DAC output. When MOUT bit is "0", this output is disabled and MOUT pin goes to VCOM voltage. The load impedance is 10kΩ (min.). When SPKP bit is "0", MOUT pin becomes Power-Down-Mode and outputs Hi-Z.

2. ALC2

The input resistance of ALC2 is 23kΩ (typ.) and centered around VCOM voltage. The level diagram of ALC2 operation is shown in Figure 19

ALC2 limiter detection level is –6.5dBV regardless of power supply voltage. When the input signal level exceeds –6.5dBV (=FS-2dB@AVDD=2.8V), the output level of ALC2 is limited.

When the signal over –6.5dBV and is input continuously to the ALC2 circuit, the changing period of ALC2 limiter operation is 2/fs=42μs@fs=48kHz and the output level is attenuated by 0.5dB/step. The ALC2 recovery operation is done by zero crossing detection and the output is gained by 1dB/step. The ALC2 recovery operation is done until the output level of Speaker-Amp goes to –8.5dBV(=FS-4dB@AVDD=2.8V). The ALC2 recovery operation period is fixed to 2048/fs=42.7mS@fs=48kHz. When inputting signal between –6.5dBV and –8.5dBV, both the limiter and recovery operations of ALC2 are not done.

When PDN pin changes from "L" to "H" or SPKP bit changes from "0" to "1", the initilizing cycle (2048/fs = 42.7ms @fs=48kHz) starts. ALC2 is disabled during initilizing cycle, ALC2 starts after finishing the initilizing cycle.

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		-6.5dBV	-8.5dBV
Period	fs=48kHz	2/fs = 42μs	2048/fs = 42.7ms
	fs=32kHz	2/fs = 63μs	2048/fs = 64ms
Zero Crossing Detection		No	Yes(Timeout = 2048/fs)
ATT/GAIN		0.5dB step	1dB step

Table 4. Content of ALC2

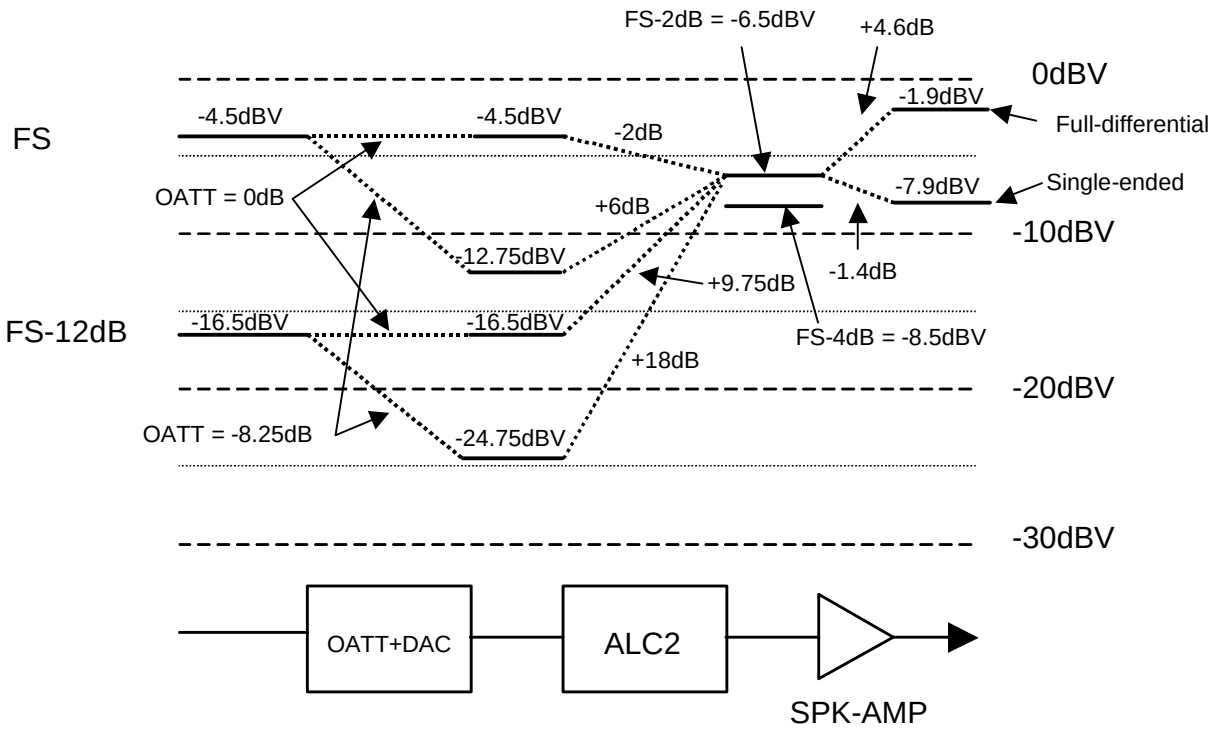


Figure 19. Speaker-Amp Output Level Diagram (AVDD=2.8V, OATT= -8.25dB & 0dB)
*FS = Full Scale

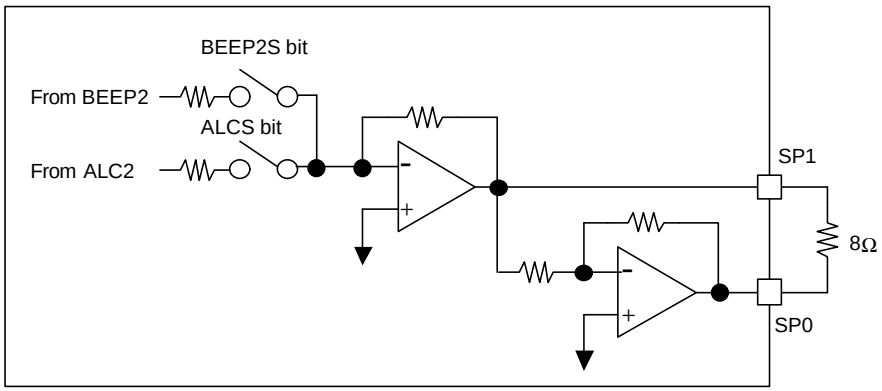


Figure 20. Speaker-Amp Internal equivalent circuit

■ Digital EQ/HPF/LPF Circuits

The AK4564 performs equalizing, filtering and ALC (Automatic Level Control) by digital domain for A/D converter data. The equalizing circuit emphasizes stereo separation when using internal microphone. LPF1, LPF2 and HPF2 are IIR filters of 1st order to compensate frequency response of microphone and etc. HPF3 is IIR filter of 2nd order to cut a wind-noise. Refer to the section of "ALC1 operation" about ALC1.

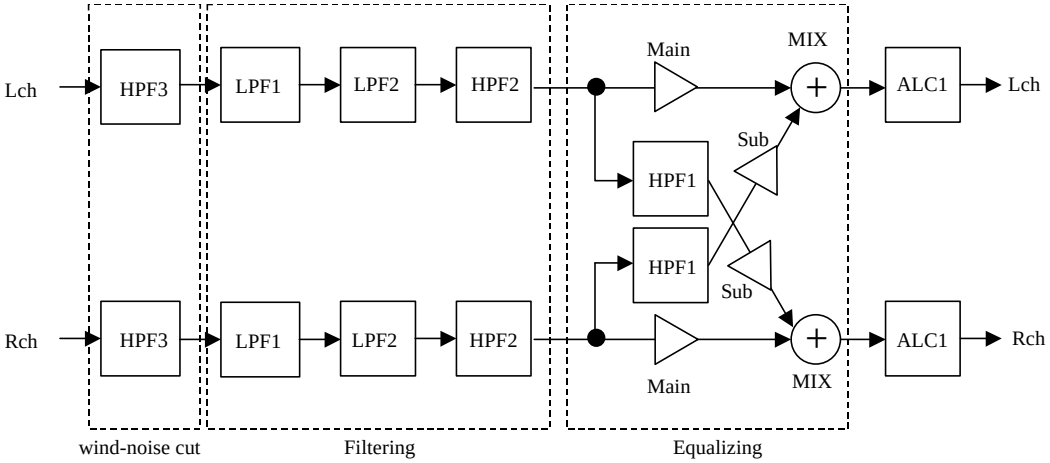


Figure 21. Digital EQ/HPF/LPF

■ ALC1 Operation

1. ALC1 Limiter Operation

When the ALC1 limiter is enabled and either Lch or Rch exceed the ALC1 limiter detection level (LMTH1-0), the IVOL value is attenuated by the amount defined in the ALC1 limiter ATT step (LMAT1-0) automatically. The operation is done at the zero crossing points of the waveform. And the timeout period of the zero crossing detection is set by ZTM1-0 bits. The IVOL value is common between L/R channels.

After finishing the operation for attenuation, if ALC1 bit is set to "0", the operation of attenuation repeats when the input signal level exceed the ALC1 limiter detection level (LMTH1-0).

2. ALC1 Recovery Operation

After completing an ALC1 limiter operation, the ALC1 recovery operation waits a time defined in WTM1-0 bits. If the input signal does not exceed the "ALC1 recovery waiting counter reset level (LMTH1-0)" during the waiting time, the ALC1 recovery operation starts. The IVOL value increases automatically up to the set reference level (REF7-0 bits) during this operation. The IVOL value is common between L/R channels. The ALC1 recovery operation is done at a period set by WTM1-0 bits. If the zero crossing operation of both L/R channels is completed during WTM1-0 period, the ALC1 recovery operation waits WTM1-0 period and then the next recovery operation starts.

When "ALC1 recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC1 limiter detection level (LMTH1-0)" during the ALC1 recovery operation, the waiting timer of ALC1 recovery operation is reset. When "ALC1 recovery waiting counter reset level (LMTH1-0) > Output Signal", the waiting timer of ALC1 recovery operation starts.

When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by FR bit = "1".

■ Writing to IVOL register when ALC1 is OFF

When writing control register continuously, the change of IVOL should be written after zero crossing timeout. If IVOL is changed by writing to control register before zero crossing detection, IVOL value of L/R channels may not give a difference level.

The following registers should not be changed during the ALC1 operation.

WTM1-0, ZTM1-0, LMTH1-0, LMAT1-0, RGAIN1-0, REF7-0, FR

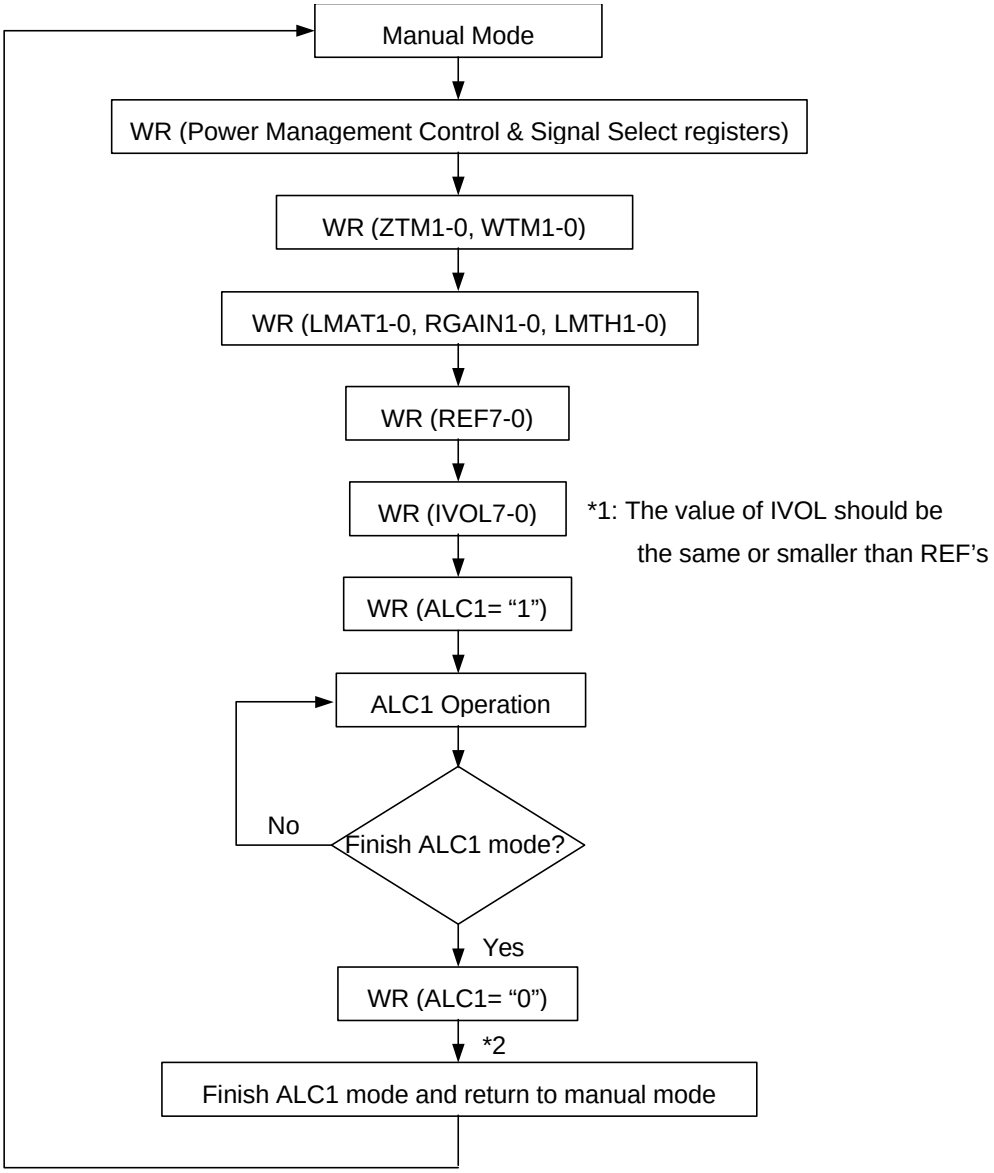


Figure 22. Registers set-up sequence at ALC1 operation

*2: When ALC1 bit changes into "0", it takes a period set by ZTM1-0 bit to return manual mode.

■ FADEIN Mode

In FADEIN Mode, the IVOL value increase gradually by the step set by FDATT1-0 bits when FDIN bit changes from "0" to "1". The FADEIN period is set by FSTM, REF7-0, FDATT1-0 and FDTM1-0 bits. The FADEIN operation is done by the zero crossing detection. The operation stops when the IVOL value becomes the REF value or the limiter detection level (LMTH). If the limiter operation is done during FADAIN period, the FADEIN operation stops and the ALC1 operation starts.

NOTE: When FDIN and FDOUT bits are set to "1" at the same time, FADEOUT operation is prior to FADEIN operation.

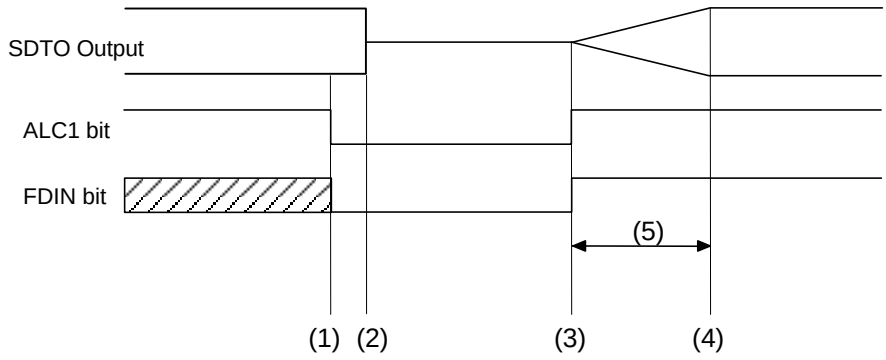


Figure 23. Example for controlling sequence in FADEIN operation

(1) WR (ALC1 = FDIN = "0"): The ALC1 operation is disabled. To start the FADEIN operation, FDIN bit is written in "0".
(2) WR (IVOL = "00H"): IVOL output is muted. **The writing to IVOL should wait a zero crossing timeout period set by ZTM1-0 bits.**
(3) WR (ALC1 = FDIN = "1"): The FADEIN operation starts. The IVOL is fade-in from MUTE state.
(4) The FADEIN operation is done until the limiter detection level (LMTH1-0) or the reference level (REF7-0). After completing the FADEIN operation. The FADEIN operation is completed and the ALC1 operation starts.
(5) FADEIN time is set by REF7-0, FDTM1-0, FSTM and FDATT bits
e.g. REF7-0 = E1H(225 dec), FDTM1-0 = 40ms, FDATT1-0 = 2 step
(225 x FDTM1-0) / FDATT1-0 = 225 x 40ms /2 = 4.5s

■ FADEOUT Mode

In FADEOUT mode, the present IVOL value decreases gradually down to the MUTE state when FDOUT bit changes from “0” to “1”. The operation is done by the zero crossing detection. If the large signal is supplied to the ALC1 circuit during the FADEOUT operation, the ALC1 limiter operation starts. However, the total time of the FADEOUT operation is the same time, even if the limiter operation is done. The period of FADEOUT is set by FSTM and FDTM1-0 bits, the number of step is set by FDATT1-0 bits. When FDOUT bit changes into “0” during the FADEOUT operation, the ALC1 operation starts from the present IVOL value. When FDOUT and ALC1 bits change into “0” at the same time, the FADEOUT operation stops and the IVOL keeps the value at that time.

NOTE: When FDIN and FDOUT bits are set to “1” at the same time, FADEOUT operation is prior to FADEIN operation.

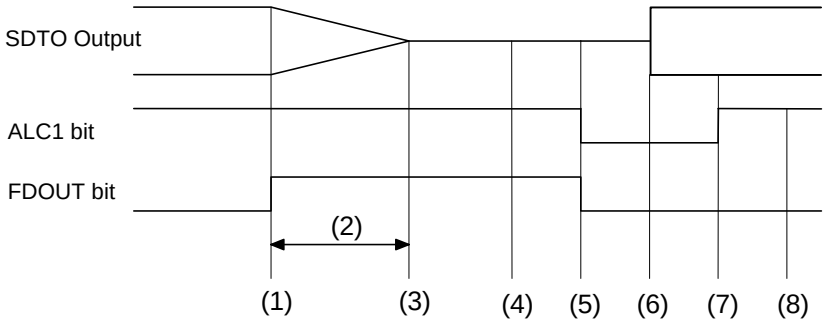


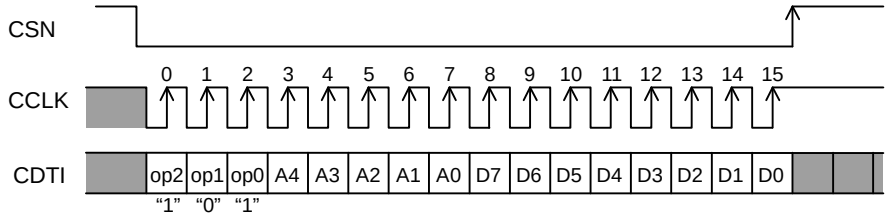
Figure 24. Example for controlling sequence in FADEOUT operation

(1) WR (FDOUT = “1”): The FADEOUT operation starts. Then ALC1 bit should be always “1”.
(2) FADEOUT time is set by REF7-0, FDTM1-0 and FDATT bits.
e.g. REF7-0 = E1H(225 dec), FDTM1-0 = 40ms, FDATT1-0 = 2 step
(225 x FDTM1-0) / FDATT1-0 = 225 x 40ms / 2 = 4.5s
(3) The FADEOUT operation is completed. The IVOL value is the MUTE state. If FDOUT bit keeps “1”, the IVOL value keeps the MUTE state.
(4) Analog and digital outputs are muted externally. Then the IVOL value is the MUTE state.
(5) WR (ALC1 = FDOUT = “0”): Exit the ALC1 and FADEOUT operations
(6) WR (IVOL = XXH): The IVOL value should be set to the same or smaller than REF’s.
(7) WR (ALC1 = “1”, FDOUT = “0”): The ALC1 operation restarts. But the ALC1 bit should be written until completing zero crossing detection operation of IVOL.
(8) Release an external mute function for analog and digital outputs.

■ Control Register WRITE Timing

The data on the 3 wires serial interface consists of op-code (3bit), address (MSB-first, 5bit) and control data (MSB-first, 8bit). The transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of CSN.

CCLK always needs 16 edges of "-" during CSN = "L". PDN pin = "L" resets the registers to their defalut values.Only write to address 00H to 0CH. Writing to the control registers except for op2-0 bit ="101" are ignored.



op2-op0: Op code (101:WRITE)
A4-A0: Register Address
D7-D0: Control data

Figure 25. Control Data Timing

■ Register Map

The following registers are reset at PDN pin = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	0	HPMIX	HPG	BEEP1	AIN2	AIN1	PRE	INT/EXT
01H	Signal Select 2	SPPS	ALCS	BEEP2H	BEEP2S	AOUT2	AOUT1	MOUT	HPDAC
02H	Power Management Control	AOUTP2	AOUTP1	SPKP	HPP	VCOM	DAC	ADC	MIC
03H	Mode Control	VOL2-1	VOL2-0	VOL1-1	VOL1-0	DIF1	DIF0	DEM1	DEM0
04H	Filter Select 1	MIX1	MIX0	HPF3	HPF2-1	HPF2-0	HPF1-1	HPF1-0	FSF
05H	Filter Select 2	0	0	0	LPF2D	LPF2-1	LPF2-0	LPF1-1	LPF1-0
06H	Timer Select	TM1	TM0	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0
07H	ALC Mode Control 1	0	GSEL	FDATT1	FDATT0	RGAIN1	RGAIN0	LMAT1	LMAT0
08H	ALC Mode Control 2	0	FSTM	0	0	0	FR	LMTH1	LMTH0
09H	ALC Mode Control 3	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0AH	Input Digital Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
0BH	Operation Mode	0	0	MIX1P	MONO	ALC2	FDIN	FDOUT	ALC1
0CH	Output Digital ATT Control	ZCE	OATT6	OATT5	OATT4	OATT3	OATT2	OATT1	OATT0

Table 5. AK4564 Register Map

Signal Select 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	0	HPMIX	HPG	BEEP1	AIN2	AIN1	PRE	INT/EXT
Default		0	0	0	0	0	0	1	0

INT/EXT: Select Internal / External MIC
0: Internal MIC (Default)
1: External MIC
PRE: Enable input signal from Pre-Amp to ADC.
0: OFF (Default)
1: ON
AIN1: Enable input signal from LIN1/RIN1 pin to ADC.
0: OFF (Default)
1: ON
AIN2: Enable input signal from LIN2/RIN2 pin to ADC.
0: OFF (Default)
1: ON
BEEP1: Enable input signal from BEEP1 pin to ADC.
0: OFF (Default)
1: ON
HPG: Select gain of Headphone-Amp
0: 0dB (Default)
1: + 16.5dB
HPMIX: Enable input signal from MIX1-Amp to Headphone-Amp
0: OFF (Default)
1: ON

Signal Select 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Signal Select 2	SPPS	ALCS	BEEP2H	BEEP2S	AOUT2	AOUT1	MOUT	HPDAC
Default		0	0	0	0	0	0	0	0

HPDAC: Enable input signal from Headphone-Amp to DAC output
0: OFF (Default)
1: ON
MOUT: Enable mono output [Mixing = (L+R)/2].
0: OFF (Default)
1: ON
When MOUT bit = “0”, MOUT pin outputs VCOM voltage.
AOUT1: Enable LOUT1/ROUT1 output
0: OFF (Default)
1: ON
When AOUT1 bit = “0”, the outputs become HVCM voltage and the amps go to Power-Save-Mode.
AOUT2: Enable LOUT2/ROUT2 output
0: OFF (Default)
1: ON
When AOUT2 bit = “0”, the outputs become HVCM voltage and the amps go to Power-Save-Mode.
BEEP2S: Enable BEEP2 to Speaker-Amp
0: OFF (Default)
1: ON
BEEP2H: Enable BEEP2 to Headphone-Amp
0: OFF (Default)
1: ON
ALCS: Enable ALC2 to Speaker-Amp
0: OFF (Default)
1: ON
SPPS: Speaker-Amp Power-Save-Mode
0: Power-Save-Mode (Default)
1: Normal operation
When SPPS bit = “0”, SP0 pin becomes Hi-Z and SP1 pin is generated to SVDD/2 voltage.

Power Management Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management Control	AOUT2P	AOUT1P	SPKP	HPP	VCOM	DAC	ADC	MIC
Default		1	1	1	0	1	1	1	1

MIC: MIC Block (Pre-Amp and MPWR) Power Control.
0: OFF
1: ON (Default)
When MIC bit = "0", Output of Pre-Amp is Hi-Z and MPWR is terminated by 5kΩ (typ) to MVSS.

ADC: ADC Power Control
0: OFF
1: ON (Default)
When ADC bit = "0", SDTO pin is fixed to "L". When ADC bit changes from "0" to "1", initializing cycle (4128/fs=86ms@fs=48kHz) starts. After initializing cycle, digital data of ADC is generated.

DAC: DAC Power Control
0: OFF
1: ON (Default)

VCOM: Common Voltage (VCOM and HVCM) Power Control
0: OFF
1: ON (Default)

HPP: Headphone-Amp Power Control
0: OFF (Default)
1: ON
When HPP bit = "0", output of Headphone-Amp becomes "L" (AVSS).

SPKP: Speaker Block Power Control (Including BEEP2, MOUT, ALC2 and Speaker-Amp)
0: OFF
1: ON (Default)
When SPKP bit = "0", output of Speaker-Amp and MOUT are Hi-Z.

AOUT1P: LOUT1/ROUT1's Amplifiers Power Control
0: OFF
1: ON (Default)
When AOUT1P bit = "0", LOUT1/ROUT1 pins are Hi-Z.

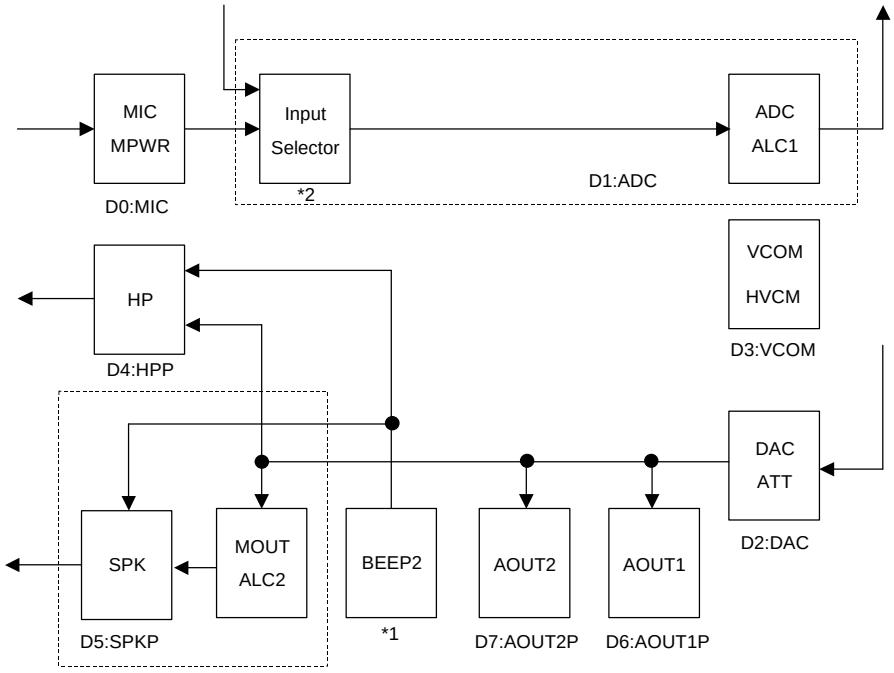
AOUT2P: LOUT2/ROUT2's Amplifiers Power Control
0: OFF
1: ON (Default)
When AOUT2P bit = "0", LOUT2/ROUT2 pins are Hi-Z.

Each block can be partially powered-down by ON/OFF ("1" / "0") of these bits. When PDN pin goes "L", all circuits are powered-down regardless of these bits. However in this case, all register are reset to the default value.

When all these registers in 02H goes "0", all circuits can be powered-down with keeping registers values.

VCOM bit must go "1" before each block operates.

Except the case of MIC=ADC=DAC=VCOM=HPP=SPKP=AOUT1P=AOUT2P = "0" or PDN pin = "L", MCLK, BCLK and LRCK should not be stopped.



*1: BEEP2 is enabled by controlling SPKP or HPP bit.

*2: MIX1-Amp is enabled by controlling ADC or DACMIX bit

Figure 26. Power Management Control

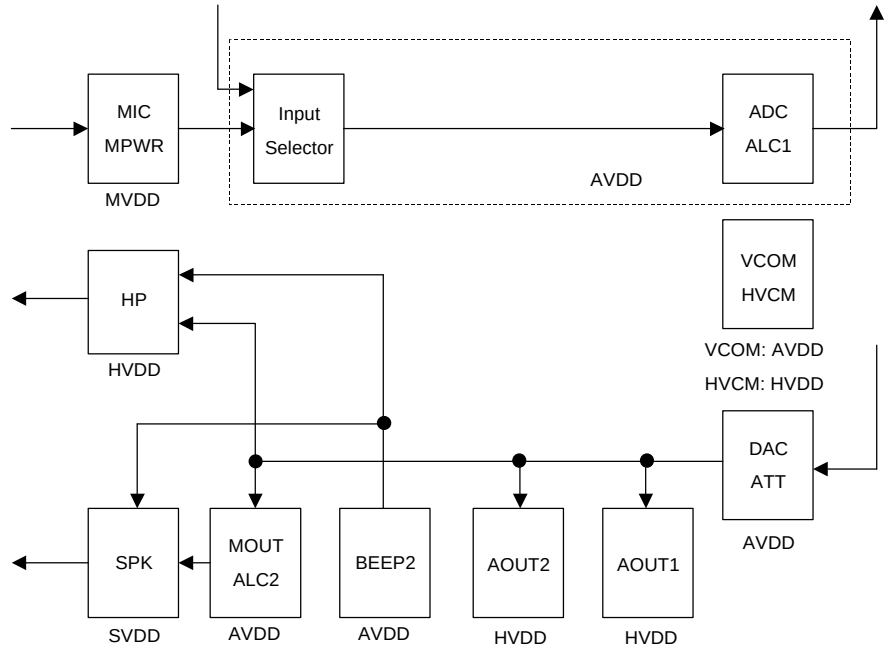


Figure 27. Analog Power Supply Source of Each Block

Mode Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control	VOL2-1	VOL2-0	VOL1-1	VOL1-0	DIF1	DIF0	DEM1	DEM0
Default		0	1	0	1	0	0	0	1

DEM1-0: Select De-emphasis Frequency

The AK4564 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. The filter corresponds to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM1 registers are enabled for input audio data.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 6. De-emphasis Frequencies

DIF1-0: Select Audio Data Format

No.	DIF1 bit	DIF0 bit	SDTO(ADC)	SDTI(DAC)	BCLK	Figure	
0	0	0	MSB justified	LSB justified	≥ 32fs	Figure 8	Default
1	0	1	LSB justified	LSB justified	= 64fs	Figure 9	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 10	
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 11	

Table 7. Audio Data Format

VOL1: LOUT1/ROUT1 output volume setting
VOL2: LOUT1/ROUT1 output volume setting

The Power supply voltage for LINEOUT-Amp is supplied from HVDD pin. The output level of LINEOUT is constant regardless of HVDD voltage. When the output voltage of HVDD pin is low, the distortion of LINEOUT degrades.

VOL2-1 VOL1-1	VOL2-0 VOL1-0	GAIN	AVDD Voltage	LINEOUT	
0	0	+7.1dB	2.6V	+2dBV	
0	1	+6.5dB	2.8V	+2dBV	Default
1	0	+5.9dB	3.0V	+2dBV	
1	1	0dB	2.8V	-4.5dBV	

Table 8. LINEOUT volume setting

Filter Select 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Filter Select 1	MIX1	MIX0	HPF3	HPF2-1	HPF2-0	HPF1-1	HFP1-0	FSF
Default		0	0	0	0	0	0	0	0

FSF: Select sampling rate to match a coefficient of digital filter
0: fs = 48kHz (Default)
1: fs = 32kHz

HPF1: Select cut-off frequency of HPF1 in EQ block. This is 1st order and IIR filter.

HPF1-1	HPF1-0	Cut-off Frequency		
		fs=32kHz	fs=48kHz	
0	0	OFF	OFF	Default
0	1	6kHz	6kHz	
1	0	7.5kHz	7.5kHz	
1	1	9kHz	9kHz	

Table 9. Select cut-off frequency of HPF1

HPF2: Select cut-off frequency of HPF2 to revise frequency response. This is 1st order and IIR filter.

HPF2-1	HPF2-0	Cut-off Frequency		
		fs=32kHz	fs=48kHz	
0	0	OFF	OFF	Default
0	1	100Hz	100Hz	
1	0	200Hz	200Hz	
1	1	300Hz	300Hz	

Table 10. Select cut-off frequency of HPF2

HPF3: Select cut-off frequency of HP3 for wind-noise cut. This is 2nd order and IIR filter. The cut-off frequency is fixed to 400Hz and is changed by FSF bit.
0: OFF (Default)
1: ON

MIX1-0: Select Mixing value in EQ block. When HPF1 is OFF, this circuit is also OFF.

MIX1	MIX0	Main : Sub	
0	0	1: 1	Default
0	1	1: 1.25	
1	0	1: 0.5	
1	1	1: 0.75	

Table 11. Select Mixing value

Filter Select 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Filter Select 2	0	0	0	LPF2D	LPF2-1	LPF2-0	LPF1-1	LPF1-0
Default		0	0	0	0	0	0	0	0

LPF1: Select cut-off frequency of LPF1 to revise frequency response. This is 1st order and IIR filter.

LPF1-1	LPF1-0	Cut-off Frequency		
		fs=32kHz	fs=48kHz	
0	0	OFF	OFF	Default
0	1	6kHz	6kHz	
1	0	9kHz	9kHz	
1	1	13.5kHz	13.5kHz	

Table 12. Select cut-off frequency of LPF1

LPF2: Select cut-off frequency of LPF2 to revise frequency response. This is 1st order and IIR filter.

LPF2-1	LPF2-0	Cut-off Frequency		
		fs=32kHz	fs=48kHz	
0	0	3kHz	3kHz	Default
0	1	4.5kHz	4.5kHz	
1	0	6.75kHz	6.75kHz	
1	1	10.125kHz	10.125kHz	

Table 13. Select cut-off frequency of LPF2

LPF2D: Enable LPF2
0: OFF (Default)
1: LPF2 ON

Timer Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	TM1	TM0	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0
Default		0	1	0	1	1	0	1	0

WTM1-0: ALC1 Recovery Waiting Period

A period of recovery operation when any limiter operation does not occur during ALC1 operation.

WTM1	WTM0	ALC1 Recovery Period	
0	0	6ms	
0	1	24ms	
1	0	48ms	Default
1	1	96ms	

Table 14. ALC1 Recovery Operation Waiting Period

ZTM1-0: IVOL Zero crossing Timeout Period

When IVOL of each L/R channels do zero crossing or timeout independently, the IVOL value is changed by μP WRITE operation or ALC1 recovery operation.

ZTM1	ZTM0	Zero Crossing Timeout Period	
0	0	6ms	
0	1	24ms	
1	0	48ms	Default
1	1	96ms	

Table 15. Zero Crossing Timeout Period

FDTM1-0: FADEIN/OUT Cycle Setting

The FADEIN/OUT operation is done by a period set by FDTM1-0 bits when FDIN or FDOUT bits are set to “1”. When IVOL of each L/R channel do zero crossing or timeout independently, the IVOL value is changed.

FDTM1	FDTM0	FADEIN/OUT Period	
0	0	20ms	
0	1	40ms	Default
1	0	48ms	
1	1	56ms	

Table 16. FADEIN/OUT Period

TM1-0: Select zero crossing timeout period of OATT

These bits are enabled at ZCE = “1”.

TM1	TM0	Zero Crossing Timeout Period	
0	0	8ms	
0	1	16ms	Default
1	0	32ms	
1	1	64ms	

Table 17. Select zero crossing timeout of OATT

*** WTM1-0, ZTM1-0, FDTM1-0 and TM1-0 have the same time between fs=32kHz (FSTM bit = “1”) and fs=48kHz (FSTM bit = “0”).**

ALC Mode Control 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	0	GSEL	FDATT1	FDATT0	RGAIN1	RGAIN0	LMAT1	LMAT0
Default		0	0	0	0	0	0	0	0

LMAT1-0: ALC1 Limiter ATT Step

The IVOL value is attenuated when the input signal exceeds the ALC1 limiter detection level. The number of step to attenuate is decided by output level.

LMAT1	LMAT0	ALC1Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	Default
0	1	2	2	2	2	
1	0	2	2	4	4	
1	1	2	4	4	8	

Table 18. ALC1 Limiter ATT Step

RGAIN1-0: ALC1 Recovery GAIN Step

During the ALC1 recovery operation, the number of steps changed from current IVOL value is set. For example, when the current IVOL value is 30H, RGAIN1-0= "01" are set, IVOL changes to 32H by the auto limiter operation, the input signal level is gained by 0.75dB (=0.375dB x 2).
When the IVOL value exceeds the reference level (REF7-0), the IVOL value does not increase.

RGAIN1	RGAIN0	GAIN STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 19. ALC1 Recovery GAIN Step

FDATT1-0: FADEIN/OUT ATT Step Setting

During the FADEIN/OUT operation, the number of steps changed from current IVOL value is set.

FDATT1	FDATT0	ATT STEP	
0	0	1	Default
0	1	2	
1	0	3	
1	1	4	

Table 20. FADEIN/OUT ATT Step Setting

GSEL: Select IVOL gain

0: MIC (Default)
1: LINE

ALC Mode Control 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	0	FSTM	0	0	0	FR	LMTH1	LMTH0
Default		0	0	0	0	0	1	1	0

LMTH1-0: ALC1 Limiter Detection Level / Recovery Counter Reset Level

LMTH1	LMTH0	ALC1 Limier Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	0	ALC1 Output ≥ -2.5dBFS	-2.5dBFS > ALC1 Output ≥ -4.1dBFS	
0	1	ALC1 Output ≥ -4.1dBFS	-4.1dBFS > ALC1 Output ≥ -6.0dBFS	
1	0	ALC1 Output ≥ -6.0dBFS	-6.0dBFS > ALC1 Output ≥ -8.5dBFS	Default
1	1	ALC1 Output ≥ -8.5dBFS	-8.5dBFS > ALC1 Output ≥ -12dBFS	

Table 21. ALC1 Limiter Detection Level / Recovery Counter Reset Level

FR: Enable ALC1 Fast Recovery Operation
0: Disable
1: Enable (Default)
If the impulse noise is supplied, the ALC1 recovery operation becomes the faster period than a set of ZTM1-0 and WTM1-0 bits.

FSTM: This data determines the time of ALC1 recovery period (WTM1-0 bit), IVOL zero crossing timeout period (ZTM1-0 bit), OATT zero crossing timeout period (TM1-0 bit) and FADEIN/OUT period (FDTM1-0 bit)
0: fs = 48kHz (Default)
1: fs = 32kHz

ALC Mode Control 3

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	ALC Mode Control 3	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		1	1	1	0	0	0	0	1

REF7-0: Reference value at ALC1 Recovery Operation. 0.375dB step, 242 Levels

During the ALC1 recovery operation, if the REF value exceeds the setting reference value by Gain operation, REF value does not become larger than the reference value.

GSEL bit selects the gain table of either MIC or LINE.

DATA	GAIN(dB)		
	MIC (GSEL bit = "0")	LINE (GSEL bit = "1")	
F1H	+36.0	+6.0	
F0H	+35.625	+5.625	
EFH	+35.25	+5.25	
•	•	•	
E2H	+30.375	+0.375	
E1H	+30.0	0	Default
E0H	+29.625	-0.375	
DFH	+29.25	-0.75	
•	•	•	
04H	-52.875	-82.875	
03H	-53.25	-83.25	
02H	-53.625	-83.625	
01H	-54.0	-84.0	
00H	MUTE	MUTE	

Table 22. Set-up Reference Level at ALC1 Recovery operation

Input Digital ATT Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Input Digital Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
Default		1	1	1	0	0	0	0	1

IVOL7-0: Input Digital Volume; 0.375dB step, 242 Level

When the ALC1 operation is OFF, IVOL can be used as volume. When the IVOL is changed, the IVOL is detected by zero crossing. Zero crossing timeout period is set by ZTM1-0 and FSTM bits.
The change of gain table between MIC and LINE is set by GSEL bit.
During the ALC1 operation, the writing value in IVOL7-0 bits is ignored

DATA	GAIN(dB)		
	MIC (GSEL bit = "0")	LINE (GSEL bit = "1")	
F1H	+36.0	+6.0	
F0H	+35.625	+5.625	
EFH	+35.25	+5.25	
•	•	•	
E2H	+30.375	+0.375	
E1H	+30.0	0	Default
E0H	+29.625	-0.375	
DFH	+29.25	-0.75	
•	•	•	
04H	-52.875	-82.875	
03H	-53.25	-83.25	
02H	-53.625	-83.625	
01H	-54	-84	
00H	MUTE	MUTE	

Table 23. Attenuation value of Input Digital Volume

Operation Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Operation Mode	0	0	MIX1P	MONO	ALC2	FDIN	FDOUT	ALC1
Default		0	0	0	0	1	0	0	0

ALC1: ALC1 Enable Flag
0: Disable (Default)
1: Enable

FDOUT: FADEOUT Enable Flag
0: Disable (Default)
1: Enable

FDIN: FADEIN Enable Flag
0: Disable (Default)
1: Enable

ALC2: ALC2 Enable Flag
0: Disable
1: Enable (Default)
After initializing cycle (2048/fs=42.7ms@fs=48kHz), ALC2 is enabled. This initializing cycle starts when PDN pin change "L" to "H" or SPKP bit change from "0" to "1".

MONO: MONO mode for Recoding
When the microphone and line inputs are mono, Rch output data of SDTO can be changed to Lch data. Then Pre-Amp, MIX1-Amp, MIX2-Amp and ADC analog block of right channel are powered down.

MONO	SDTO Output Data		Mode	
	Lch	Rch		
0	Lch	Rch	Stereo	Default
1	Lch	Lch	Mono	

Table 24. SDTO Output Data

MIX1P: MIX1-Amp Power Control
MIX1P and ADC bits are Ored.
0: Power OFF (Default)
1: Power ON

Output Digital ATT Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Output Digital ATT Control	ZCE	OATT6	OATT5	OATT4	OATT3	OATT2	OATT1	OATT0
Default		1	1	0	1	1	0	0	0

ZCE: OATT Zero Crossing Enable Flag
0: Disable
1: Enable (Default)

OATT6-0: Output Digital Volume; 89 Level, 0dB ~ -65.25dB & Mute, 0.75dB step
This volume includes zero crossing detection circuit. When ZCE is "1", the change of volume is detected by zero crossing independently. Zero crossing timeout period is set by TM1-0 and FSTM bits.
When ZCE is "0", the OATT is changed immediately.

DATA(HEX)	ATT Level	
58H	0dB	Default
57H	-0.75dB	
56H	-1.5dB	
•	•	
3DH	-20.25dB	
3CH	-21.0dB	
3BH	-21.75dB	
•	•	
03H	-63.75dB	
02H	-64.5dB	
01H	-65.25dB	
00H	MUTE	

Table 25. Attenuation value of Output Digital Volume

SYSTEM DESIGN

Figure 28 shows the system connection diagram. An evaluation board (AKD4564) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

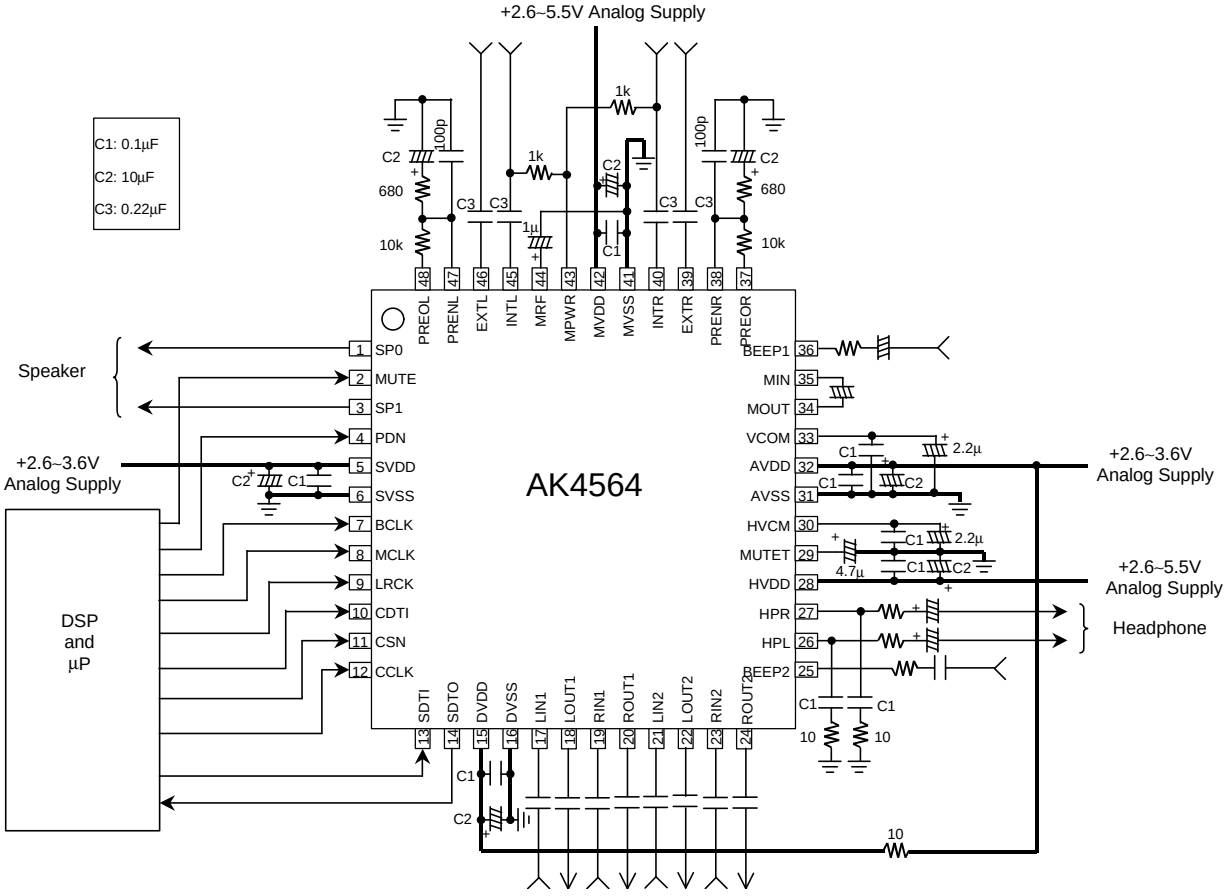
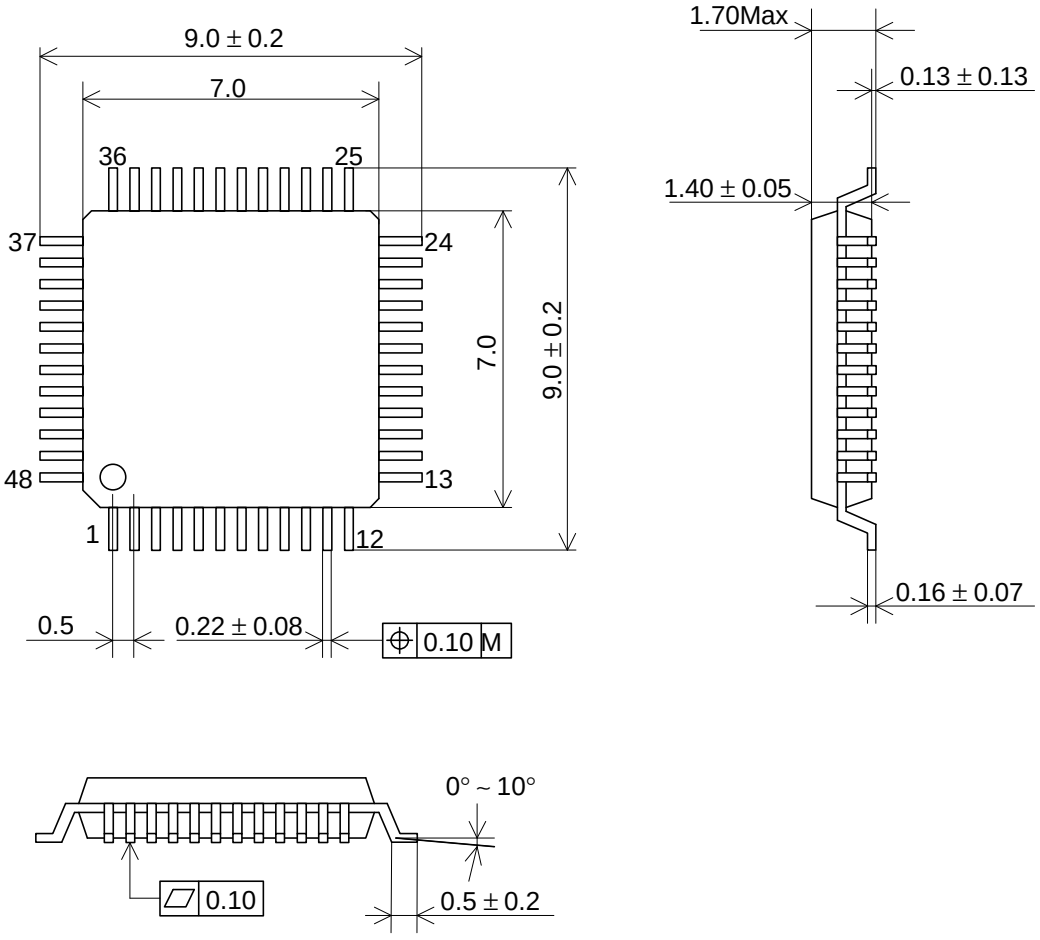


Figure 28. System Connection Diagram

PACKAGE

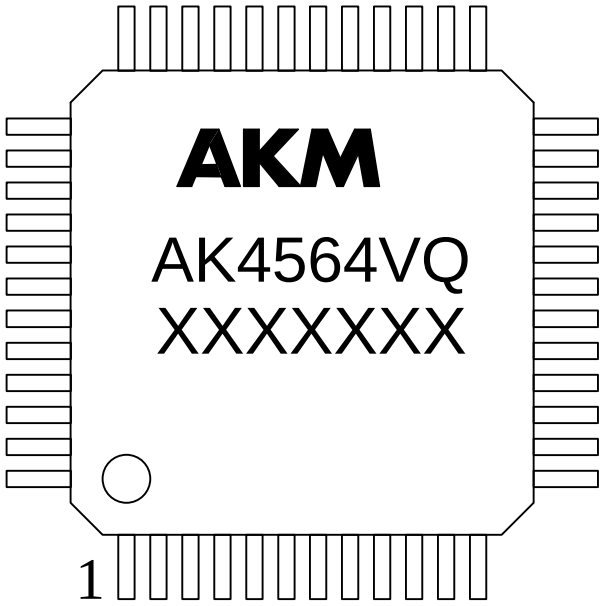
48pin LQFP(Unit:mm)



■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate (Pb free)

MARKING



XXXXXXXX: Date code identifier

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