Product Change Notice

(Notification - P1408037)

(SAG-B-14-0008)

September 9, 2014

To: *Our Valued Digi-Key Customer*

Overview: The purpose of this notification is to communicate a product change of a Renesas Electronics America, Inc. (REA) device. This device is changing its on-chip ROM code. There is no part number change. Please see the "PCN Note" section for additional details.

Affected Products: A review of our shipment records to your company indicates the product listed below is affected by this notification.

Booking Part Number	PCN Note
UPD720210K8-BAF-A	The firmware in the on-chip masked ROM (i.e. masked-ROM code) will be updated to a new version to allow system design without the need for external SPI flash memory. Customers can use the new version of the chip (new masked-ROM code) on existing designs (with external SPI flash memory) and are not expected to be affected by this change. The new masked-ROM code will support system designs with or without the external SPI flash memory. Please see the appendix for revision identification information and associated documentation for detail usage and restrictions.

Part number given in this list is for active part numbers in REA database at the time of this notification.

Key Dates:

Shipments from REA of the above product with the new firmware (masked-ROM code) begins: (Cross shipments between the original and new code may continue for a period of time).	**Oct. 9th, 2014**

Response: No response is required. REA will consider this notification approved 30 days after its issue. If you anticipate volumes beyond your regular rate prior to the transition date, please contact your REA sales representative with a forecast of your requirements.

Please contact your REA sales representative for any questions, comments, or requests for additional information related to this change.

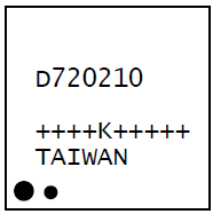
Thank you for your attention.

Sincerely,

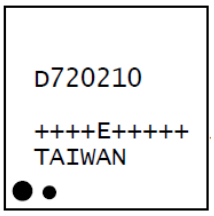
Renesas Electronics America, Inc.

APPENDIX

Identification of Change: The 5th character of lot code will change from “K” to “E”.



Previous Version
“K”



New Version
“E”

Renesas Electronics Product Change Notice (PCN)

PCN Tracking Number : SAG-B-14-0008

Subject : Change of integrated ROM code for USB3.0 HUB Controller (μPD720210K8)

Dear Customers ;

Renesas Electronics Corp. would like to request your kind understanding and acceptance for the following change on above titled matter.

1. Object Product:
μPD720210K8-BAF-A

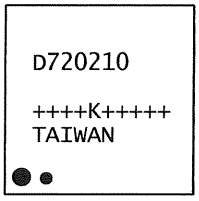
2. Description of change:
Change of integrated ROM code

3. Reason for change:
This change is to enable the usage of eliminating external SPI ROM.
The system using the current version with external SPI ROM is not affected by replacing the version with this change, because the functionality of these versions will be identical, in the case where they are used with the external ROM.

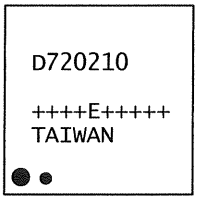
4. Schedule of change:
Mass production will start from beginning of September, 2014.

5.Infulence on quality:
None. Please refer reliability data attached next page.

6. Identification of change :
Changing 5th digit of lot code by each plant as below. (Before change: K, after change: E)



Before change



<- Lot code

After change

7. Request to customers
Please approve above change until 29th August , 2014.

Toshihiro Noma
18th June ,2014
Department Manager
Product Management Division 2
OA & ICT Business Division
Renesas Electronics Corporation

RENESAS

TYPE: UPD720210K8-BAF-A

1.LIFE TESTS AND FAILURE SUMMARY

Sub-Group	Test Performed	Test Condition	Sample Size	Number of Defective
1	High-Temperature Bake	Ta=150°C,1000H	45	0
2	High-Temperature Operating Life	Ta=125°C,1000H Specification voltage	77	0
3	Temperature Humidity Bias (Preconditioning)	Ta=85°C,RH=85% 1000H Specification voltage	45	0
4	UHAST (Preconditioning)	Ta=130°C,RH=85% 2.30×10^5Pa, 192H	45	0
5	Temperature Cycling (Preconditioning)	Ta=-65°C~150°C 30min,300cycles	45	0

Preconditioning :T/C(20C)+HT(125°C)10hr+HHT(30°C,70%RH)168hr+IR Reflow(260°C Peak)×3Times

MSL : JEDEC level3

ESD DATA

DEVICE TYPE:UPD720210K8-BAF-A

1-1.Test Condition

(1) C=200pF,Rs=0Ω,(JEDEC)
(2) 1 Times force to each pins against VSS(GND) or VDD(VCC)

1-2.Test Result

Condition	Forcing Voltage & Polarity	Gnd Condition	Forcing Times	Sample Size	# Of Failure
1	+200V Voltage Force to Each Pins	VDD(Vcc)=0V	1 Times	3 Pcs	0
2	-200V Voltage Force to Each Pins	VDD(Vcc)=0V	1 Times	3 Pcs	0
3	+200V Voltage Force to Each Pins	Vss(GND)=0V	1 Times	3 Pcs	0
4	-200V Voltage Force to Each Pins	Vss(GND)=0V	1 Times	3 Pcs	0

2-1.Test Condition

(1) C=100pF,Rs=1.5kΩ,(JEDEC)
(2) 1 Times force to each pins against VSS(GND) or VDD(VCC)

2-2.Test Result

Condition	Forcing Voltage & Polarity	Gnd Condition	Forcing Times	Sample Size	# Of Failure
1	+2000V Voltage Force to Each Pins	VDD(Vcc)=0V	1 Times	3 Pcs	0
2	-2000V Voltage Force to Each Pins	VDD(Vcc)=0V	1 Times	3 Pcs	0
3	+2000V Voltage Force to Each Pins	Vss(GND)=0V	1 Times	3 Pcs	0
4	-2000V Voltage Force to Each Pins	Vss(GND)=0V	1 Times	3 Pcs	0

LATCH-UP DATA

DEVICE TYPE:UPD720210K8-BAF-A

1. TEST CONDITION

DC CURRENT METHOD (ROOM TEMPERATURE)

2. TEST RESULT

TERMINAL	LATCH-UP CURRENT	SAMPLE SIZE	# OF FAILURE
I/O	±150mA	6	0