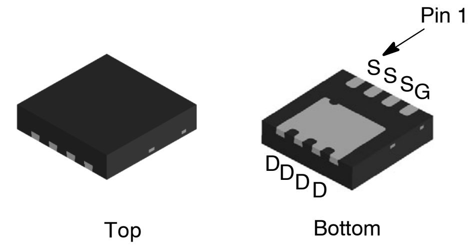
MOSFET – P-Channel, POWERTRENCH®

-150 V, -2.6 A, 1.2 Ω

FDMC86265P



**WDFN8 3.3x3.3, 0.65P
CASE 511DH**

General Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for the on−state resistance and yet maintain superior switching performance.

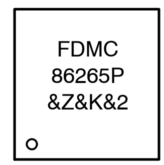
Features

- Max $r_{DS(on)} = 1.2\ \Omega$ at $V_{GS} = -10$ V, $I_D = -1$ A
- Max $r_{DS(on)} = 1.4\ \Omega$ at $V_{GS} = -6$ V, $I_D = -0.9$ A
- Very Low RDS−On Mid Voltage P−Channel Silicon Technology Optimized for Low Qg
- This Product is Optimized for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Applications

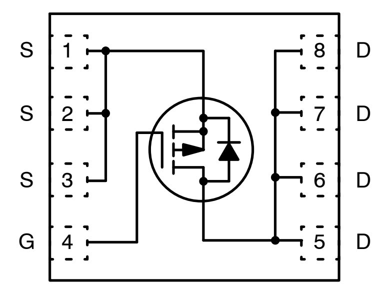
- Active Clamp Switch
- Load Switch

MARKING DIAGRAM



FDMC	= Specific Device Code
86265P	= Specific Device Code
&Z	= Assembly Location
&K	= Lot Run Traceability Code
&2	= Date Code (Year and Week)

PIN ASSIGNMENT



P−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

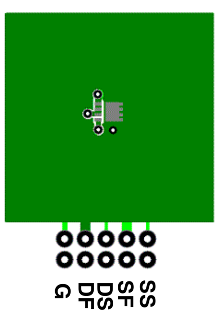
Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			−150	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current	Continuous (Note 5)	T_C = 25°C	−2.6	A
		Continuous (Note 5)	T_C = 100°C	−1.65	
		Continuous (Note 1a)	T_A = 25°C	−1	
		Pulsed (Note 4)		−9	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			6	mJ
P_D	Power Dissipation		T_C = 25°C	16	W
	Power Dissipation (Note 1a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

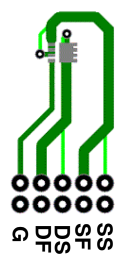
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; P−ch: L = 3 mH, I_{AS} = −2 A, V_{DD} = −150 V, V_{GS} = −10 V. 100% test al L = 0.1 mH, I_{AS} = −9 A.
4. Pulsed Id please refer to Figure 11 and Figure 24 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−150	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	–	−125	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −120 V, V_{GS} = 0 V	–	–	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−2	−3.2	−4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	–	5	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −1 A	–	0.86	1.2	Ω
		V_{GS} = −6 V, I_D = −0.9 A	–	0.95	1.4	
		V_{GS} = −10 V, I_D = −1 A, T_J = 125°C	–	1.53	2.2	
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −1 A	–	1.9	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −75 V, V_{GS} = 0 V, f = 1 MHz	–	158	210	pF
C_{oss}	Output Capacitance		–	16	25	pF
C_{rss}	Reverse Transfer Capacitance		–	0.7	5	pF
R_g	Gate Resistance		0.1	3	7.5	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −75 V, I_D = −1 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	–	5.8	12	ns
t_r	Rise Time		–	2.2	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	8	16	ns
t_f	Fall Time		–	6.4	13	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} = −75 V, I_D = −1 A, V_{GS} = 0 V to −10 V	–	2.8	4	nC
Q_{gs}	Total Gate Charge	V_{DD} = −75 V, I_D = −1 A	–	0.8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	0.7	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −1 A (Note 2)	–	−0.87	−1.3	V
t_{rr}	Reverse Recovery Time	I_F = −1 A, di/dt = 100 A/μs	–	50	80	ns
Q_{rr}	Reverse Recovery Charge		–	78	124	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

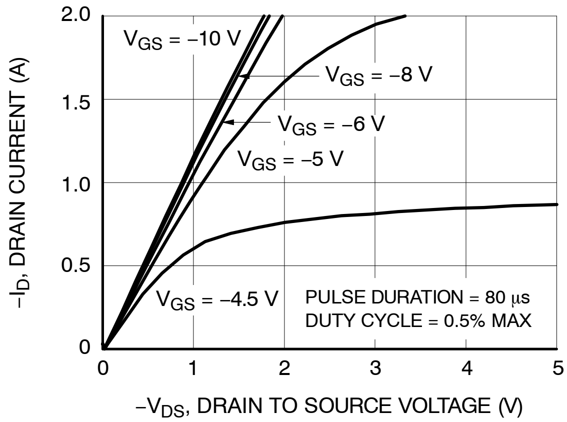


Figure 1. On Region Characteristics

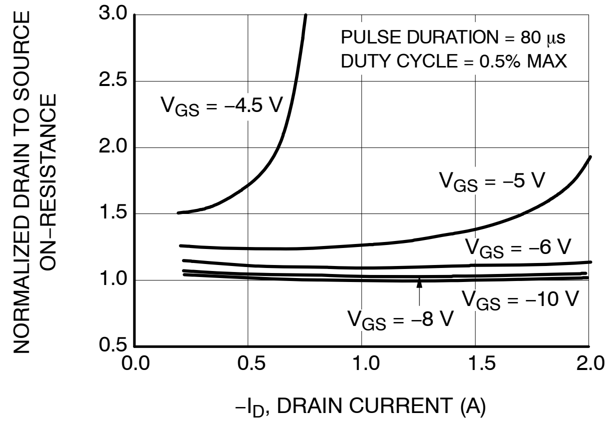


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

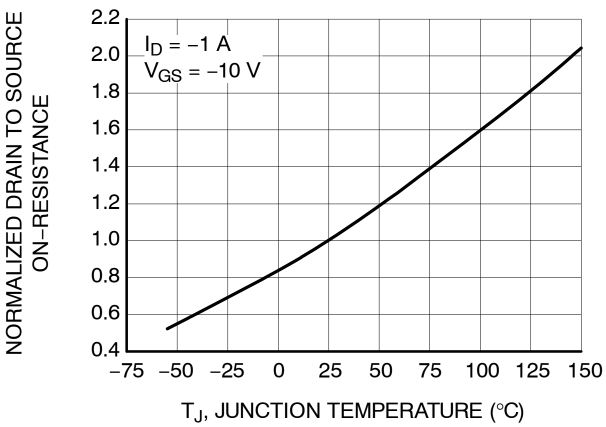


Figure 3. Normalized On Resistance vs. Junction Temperature

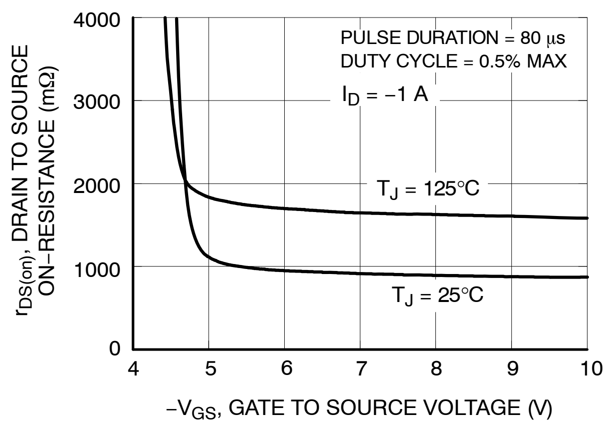


Figure 4. On−Resistance vs. Gate to Source Voltage

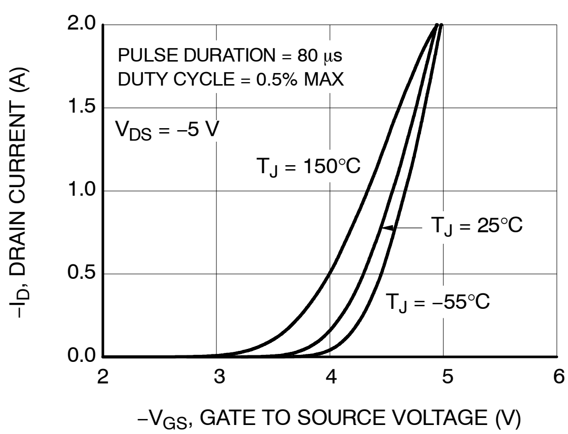


Figure 5. Transfer Characteristics

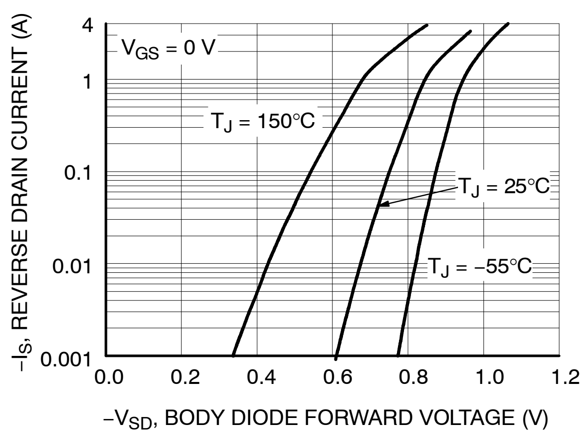


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

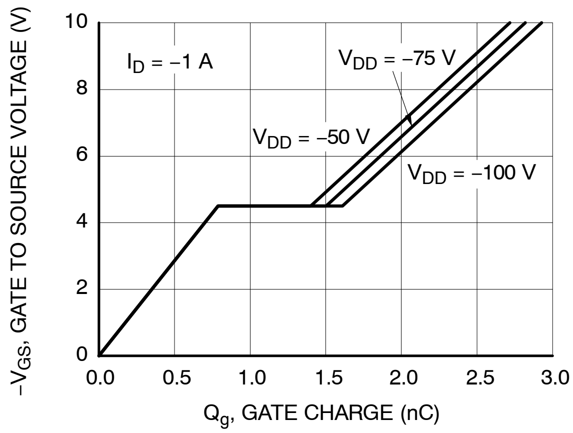


Figure 7. Gate Charge Characteristics

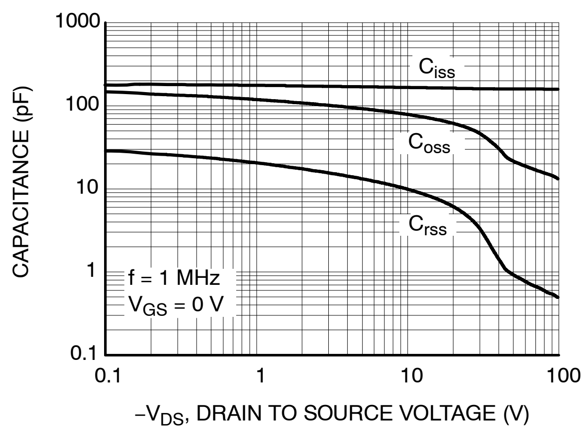


Figure 8. Capacitance vs. Drain to Source Voltage

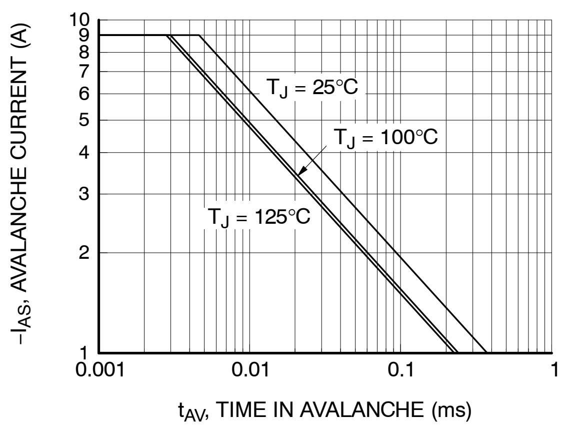


Figure 9. Unclamped Inductive Switching Capability

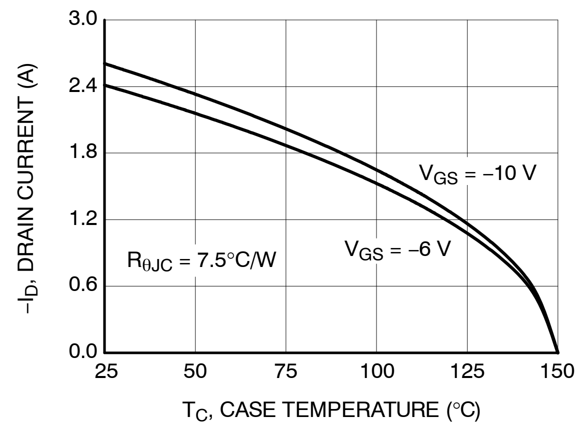


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

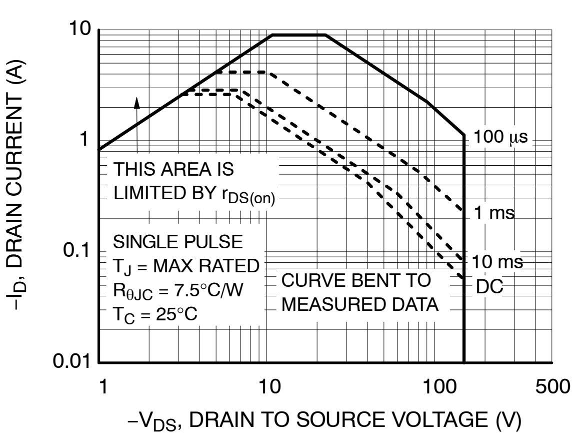


Figure 11. Forward Bias Safe Operating Area

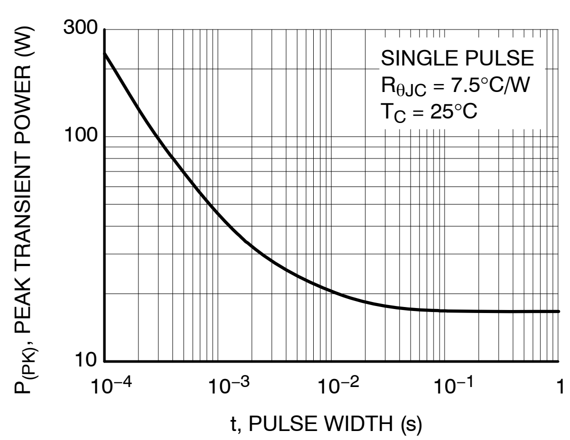


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

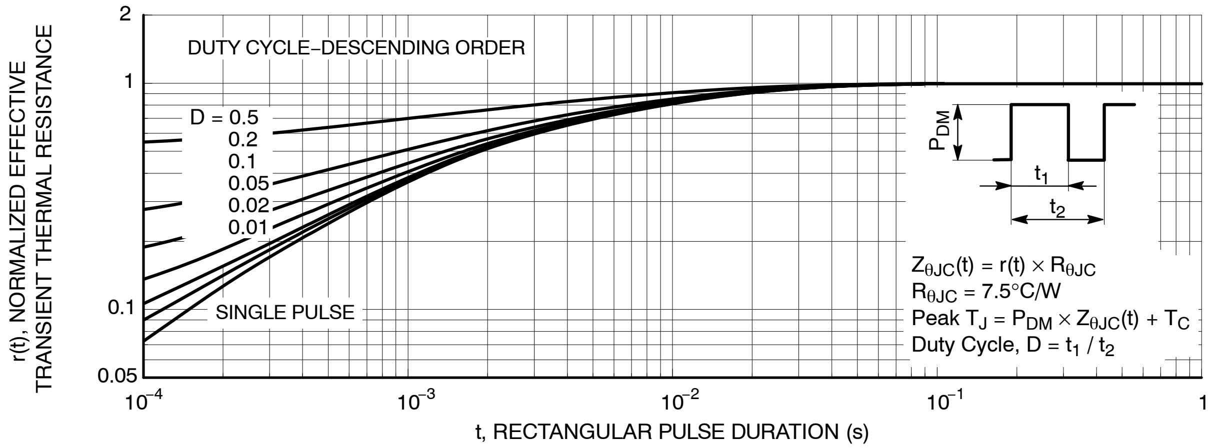


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

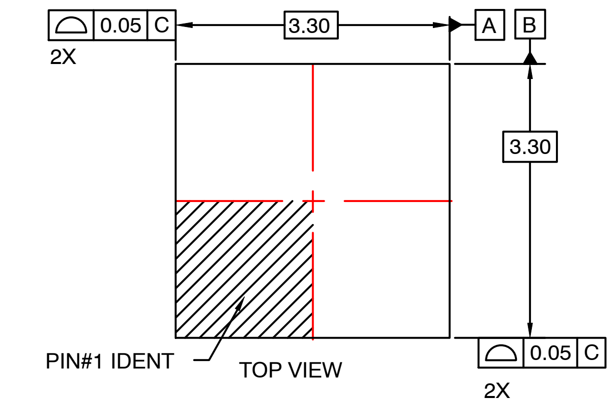
ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDMC86265P	FDMC86265P	WDFN8 3.3x3.3, 0.65P (Pb−Free)	3000 / Tape & Reel

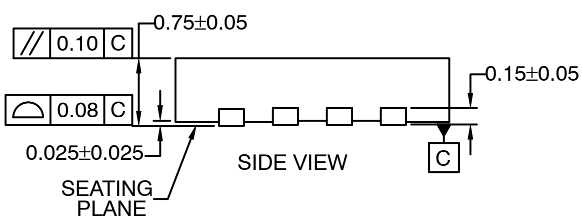
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

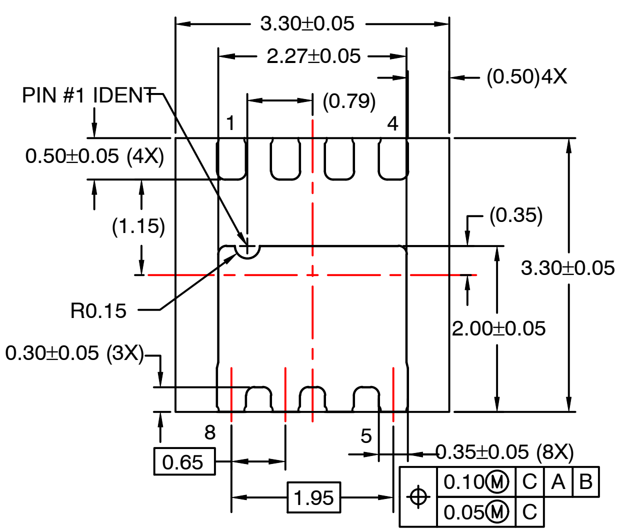
DATE 31 JUL 2016



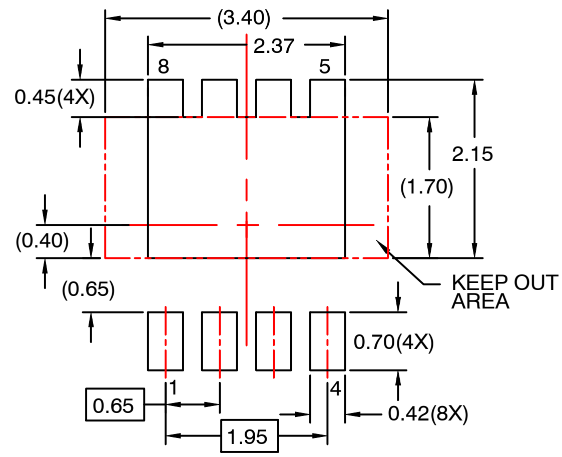
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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