

**Vishay Siliconix** 

## Dual P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A)		
- 20	0.086 at V <sub>GS</sub> = - 4.5 V	- 4.1		
	0.121 at V <sub>GS</sub> = - 2.5 V	- 3.4		
	0.171 at V <sub>GS</sub> = - 1.8 V	- 2.9		

# 1206-8 ChipFET® Marking Code

Bottom View

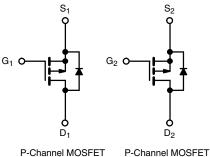
DF XX Lot Traceability and Date Code Part # Code

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- Low R<sub>DS(on)</sub> Dual and Excellent Power Handling in a Compact Footprint
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

- Load Switch
- PA Switch
- **Battery Switch**



Ordering Information: Si5935DC-T1-E3 (Lead (Pb)-free) Si5935DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T	<sub>A</sub> = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20		V
Gate-Source Voltage		V <sub>GS</sub>	± 8		
Continuous Drain Current (T <sub>.I</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	– I <sub>D</sub>	- 4.1	- 3	А
Continuous Drain Current $(T_j = T_{30}, C)$	T <sub>A</sub> = 85 °C		- 2.9	- 2.2	
Pulsed Drain Current		I <sub>DM</sub>	- 15		A
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	- 1.8	- 0.9	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	2.1	1.1	W
	T <sub>A</sub> = 85 °C		1.1	0.6	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum has the Associated	$t \le 5 s$	- R <sub>thJA</sub> R <sub>thJF</sub>	50	60		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		90	110	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State		30	40		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See reliability manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$	- 0.4		- 1.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = ± 8 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 V, V_{GS} = 0 V$	- 1				
		$V_{DS}$ = - 20 V, $V_{GS}$ = 0 V, $T_{J}$ = 85 °C			- 5	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS}$ $\leq$ - 5 V, $V_{GS}$ = - 4.5 V	- 15			Α	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$		0.069	0.069 0.086		
	R <sub>DS(on)</sub>	$V_{GS}$ = - 2.5 V, I <sub>D</sub> = - 2.5 A		0.097	0.121	Ω	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 0.6 A		0.137	0.171		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -3 \text{ A}$		8		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{\rm S}$ = - 0.9 A, $V_{\rm GS}$ = 0 V		- 0.8	- 1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg			5.5	8.5		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = - 10 V, $V_{GS}$ = - 4.5 V, $I_D$ = - 3 A		0.91		nC	
Gate-Drain Charge	Q <sub>gd</sub>			1.6		1	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD}$ = - 10 V, R <sub>L</sub> = 10 $\Omega$		18	30	-	
Rise Time	t <sub>r</sub>			32	50		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 6 $\Omega$		42	65	ns	
Fall Time	t <sub>f</sub>			26	40		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 0.9 A, dl/dt = 100 A/μs		30	60		

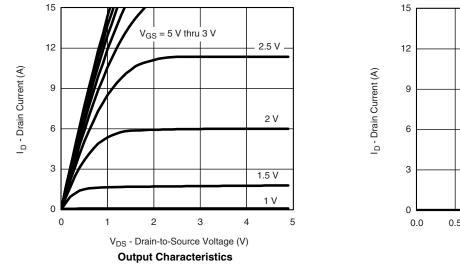
Notes:

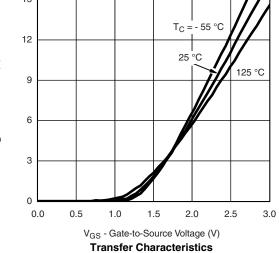
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

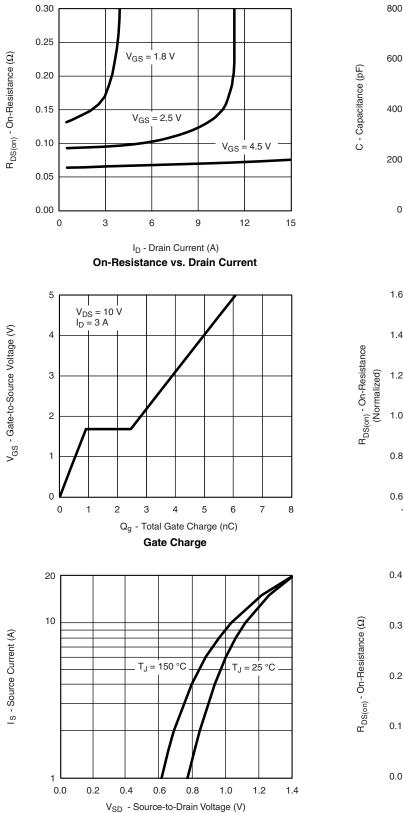






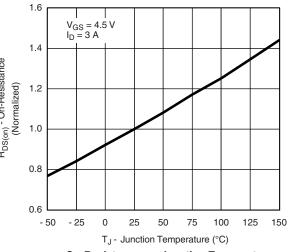
## Si5935DC Vishay Siliconix

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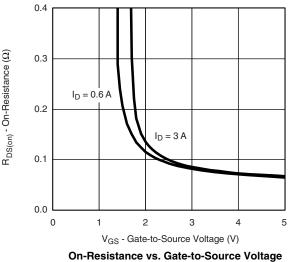


Source-Drain Diode Forward Voltage

 $G_{0}$   $G_{0}$   $G_{1}$   $G_{1$ 

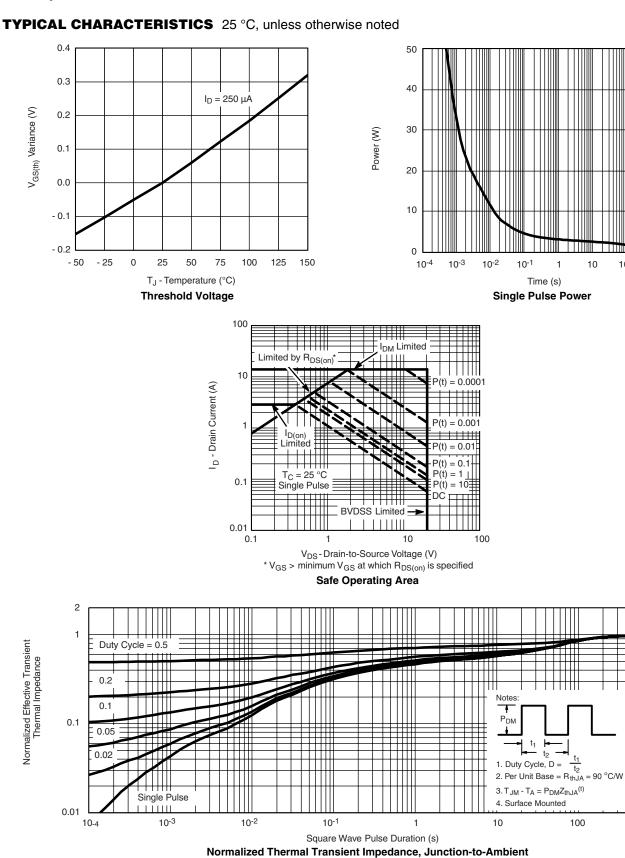


**On-Resistance vs. Junction Temperature** 



## Si5935DC

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600



600

100

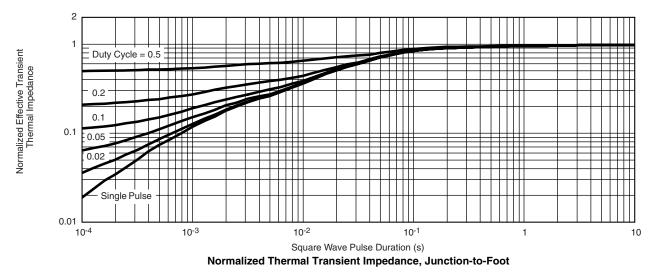
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Si5935DC

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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg772220">www.vishay.com/ppg772220</a>.



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