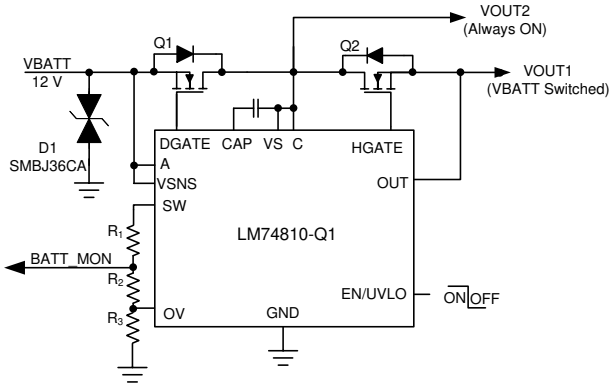
LM7481-Q1 Ideal Diode Controller with Active Rectification and Load Dump Protection

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3-V to 65-V input range
- Reverse input protection down to –65 V
- Drives external back to back N-channel MOSFETs
- Ideal diode operation with 9.1-mV A to C forward voltage drop regulation
- Low reverse detection threshold (–4 mV) with fast response (0.5 µs)
- Active rectification up to 200-KHz
- 60-mA peak gate (DGATE) turn-on current
- 2.6-A peak DGATE turnoff current
- Integrated 3.8-mA charge pump
- Adjustable over voltage protection
- Low 2.87 µA shutdown current (EN/UVLO=Low)
- 2.6-A peak DGATE turn-off current
- Meets automotive ISO7637 transient requirements with a suitable TVS diode
- Available in space saving 12-Pin WSON package

2 Applications

- Automotive battery protection
  - ADAS domain controller
  - Head unit
  - Premium audio
- Active ORing for redundant power



Ideal Diode with Switched Output

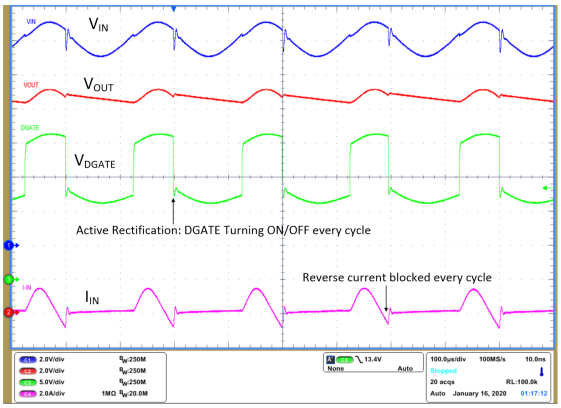
3 Description

The LM74810-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control and over voltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong charge pump of 3.8 mA with 60-mA peak GATE source current driver stage and short turn ON and turn OFF delay times ensures fast transient response ensuring robust and efficient MOSFET switching performance during automotive testing such as ISO16750 or LV124 where an ECU is subjected to input short interruptions and AC superimpose input signals upto 200-KHz frequency. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and over voltage protection using HGATE control. The device features an adjustable over voltage cut-off protection feature for load dump protection.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74810-Q1	WSON (12)	3.0 mm x 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



ISO16750, LV124 AC Superimpose Performance

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Changed status from "Advance Information" to "Production Data"	1

5 Pin Configuration and Functions

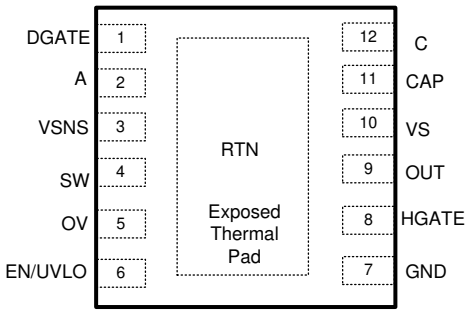


Figure 5-1. 12-Pin WSON Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	LM74810-Q1 WSON		
DGATE	1	O	Diode Controller Gate Drive Output. Connect to the GATE of the external MOSFET. Anode of the ideal diode.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET
VSNS	3	I	Voltage sensing input.
SW	4	I	Voltage sensing disconnect switch terminal. VSNS and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN/UVLO is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used then short them together and connect to VS pin.
OV	5	I	Adjustable over voltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OVP exceeds the over voltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OVP falling threshold.
EN/UVLO	6	I	EN/UVLO Input. Connect to VS pin for always ON operation. Can be driven externally from a mirco controller I/O. Pulling it low below $V_{(ENF)}$ makes the device enter into low Iq shutdown mode. For UVLO, connect an external resistor ladder to EN/UVLO to GND.
GND	7	G	Connect to the system ground plane.
HGATE	8	O	GATE driver output for the HSFET. Connect to the GATE of the external FET
OUT	9	I	Connect to the output rail (external MOSFET source).
VS	10	I	Input power supply to the IC. Connect VS to middle point of the common drain back to back MOSFET configuration. Connect a 100nF capacitor across VS and GND pins.
CAP	11	O	Charge pump output. Connect a 100-nF capacitor across CAP and VS pins.
C	12	I	Cathode of the ideal diode. Connect to the drain of the external MOSFET
RTN	Thermal Pad	—	Leave exposed pad floating. Do not connect to GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	–65	70	V
	VS to GND	–1	70	
	VSNS, SW, EN/UVLO, C, OV, OUT to GND, $V_{(A)}$ > 0 V	–0.3	70	
	VSNS, SW, EN/UVLO, C, OV, OUT to GND, $V_{(A)}$ ≤ 0 V	$V_{(A)}$	(70 + $V_{(A)}$)	
	RTN to GND	–65	0.3	
	I_{VSNS}, I_{SW}	–1	10	mA
	$I_{EN/UVLO}$, I_{OV}, $V_{(A)}$ > 0 V	–1		mA
	$I_{EN/UVLO}$, I_{OV}, $V_{(A)}$ ≤ 0 V	Internally limited		
Output Pins	OUT to VS	–65	16.5	V
Output Pins	CAP to VS	–0.3	15	V
	CAP to A	–0.3	85	
	DGATE to A	–0.3	15	
	HGATE to OUT	–0.3	15	
Output to Input Pins	C to A	–5	85	
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (DGATE, OV, and C)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
	VS to GND	0		65	V
	EN/UVLO to GND	0		65	V
External Capacitance	CAP to A, VS to GND, A to GND	0.1			µF
External MOSFET max VGS rating	DGATE to A and HGATE to OUT	15			V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM74810-Q1 DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = $V_{(VSNS)}$ = 12 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3		65	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.4	2.6	2.85	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		1.9	2.1	2.3	V
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V		2.87	5	µA
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		396		µA
		$V_{(A)}$ = $V_{(VS)}$ = 24 V, $V_{(EN/UVLO)}$ = 2 V		408	480	µA
$I_{(REV)}$	$I_{(A)}$ leakage current during Reverse Polarity,	0 V ≤ $V_{(A)}$ ≤ – 65 V		19	112	µA
	$I_{(OUT)}$ leakage current during Reverse Polarity				1	µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	EN/UVLO threshold voltage, rising		1.195	1.231	1.267	V
$V_{(UVLOF)}$	EN/UVLO threshold voltage, falling		1.091	1.132	1.159	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3	0.67	0.93	V
$V_{(EN\_Hys)}$	Enable Hysteresis		37	72	95	mV
$I_{(EN/UVLO)}$		0 V ≤ $V_{(EN/UVLO)}$ ≤ 65 V		52	200	nA
OVER VOLTAGE PROTECTION AND BATTERY SENSING (VSNS, SW, OV) INPUT						
$R_{(SW)}$	Battery sensing disconnect switch resistance	3 V ≤ $V_{(SNS)}$ ≤ 65 V	10	19.5	46	Ω
$V_{(OVR)}$	Overvoltage threshold input, rising		1.195	1.231	1.267	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.091	1.13	1.159	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = $V_{(VSNS)}$ = 12 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(OV)}$	OV Input leakage current	0 V ≤ $V_{(OV)}$ ≤ 65 V		53	200	nA
CHARGE PUMP (CAP)						
$I_{(CAP)}$	Charge Pump source current (Charge pump on)	$V_{(CAP)}$ – $V_{(A)}$ = 7 V, 6 V ≤ $V_{(S)}$ ≤ 65 V	2.5	3.8		mA
VCAP – VS	Charge Pump Turn ON voltage		11	12.2	13.2	V
	Charge Pump Turnoff voltage		11.9	13.2	14.1	V
$V_{(CAP\ UVLO)}$	Charge Pump UVLO voltage threshold, rising		5.4	6.6	7.9	V
	Charge Pump UVLO voltage threshold, falling		4.4	5.5	6.6	V
IDEAL DIODE (A, C, DGATE)						
$V_{(A\_PORR)}$	$V_{(A)}$ POR threshold, rising		2.2	2.35	2.6	V
$V_{(A\_PORF)}$	$V_{(A)}$ POR threshold, falling		2	2.2	2.4	V
$V_{(AC\_REG)}$	Regulated Forward $V_{(A)}$–$V_{(C)}$ Threshold		5.8	9.1	12.4	mV
$V_{(AC\_REV)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Fast Reverse Current Blocking		–6.4	–4	–1.3	mV
$V_{(AC\_FWD)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Reverse to Forward transition		150	177	200	mV
$V_{(DGATE)}$ – $V_{(A)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.5	13	V
$I_{(DGATE)}$	Peak Gate Source current	$V_{(A)}$ – $V_{(C)}$ = 100 mV, $V_{(DGATE)}$ – $V_{(A)}$ = 1 V		60		mA
	Peak Gate Sink current	$V_{(A)}$ – $V_{(C)}$ = –12 mV, $V_{(DGATE)}$ – $V_{(A)}$ = 11 V		2670		mA
	Regulation sink current	$V_{(A)}$ – $V_{(C)}$ = 0 V, $V_{(DGATE)}$ – $V_{(A)}$ = 11 V	8.4	14.9		µA
$I_{(C)}$	Cathode leakage Current	$V_{(A)}$ = –14 V, $V_{(C)}$ = 12 V	4	9	32	µA
HIGH SIDE CONTROLLER (HGATE, OUT, SNS, SW, OV)						
$V_{(HGATE)}$ – $V_{(OUT)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.1	14.5	V
$I_{(HGATE)}$	Source Current		39	55	75	µA
	Sink Current	$V_{(OV)}$ > $V_{(OVR)}$	168	260		mA

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGATE\_OFF(dly)}$	DGATE Turnoff Delay during reverse voltage detection	$V_{(A)}$ – $V_{(C)}$ = +30 mV to –100 mV to $V_{(DGATE–A)}$ < 1 V, $C_{(DGATE–A)}$ = 10 nF		0.5	0.875	µs
$t_{DGATE\_ON(dly)}$	DGATE Turnon Delay during forward voltage detection	$V_{(A)}$ – $V_{(C)}$ = –20 mV to +700 mV to $V_{(DGATE-A)}$ > 5 V, $C_{(DGATE-A)}$ = 10 nF		0.85	1.6	µs
$t_{EN(dly)\_DGATE}$	DGATE Turnon Delay during EN/UVLO	EN/UVLO ↑ to $V_{(DGATE-A)}$ > 5V, $C_{(DGATE-A)}$ = 10 nF	98	175	270	µs
$t_{EN\_OFF(deg)\_DGATE}$	DGATE Turnoff Deglitch during EN/UVLO	EN/UVLO ↓ to DGATE ↓		8.1		µs
$t_{EN\_OFF(deg)\_HGATE}$	HGATE Turnoff Deglitch during EN/UVLO	EN/UVLO ↓ to HGATE ↓	3	4.6	6	µs

6.6 Switching Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OVP\_OFF(deg)\_HGATE}$	HGATE Turnoff Deglitch during OV	OV ↑ to HGATE ↓		3.98	5.4	µs
$t_{OVP\_ON(deg)\_HGATE}$	HGATE Turnon Deglitch during OV	OV ↓ to HGATE ↑		2.95		µs

6.7 Typical Characteristics

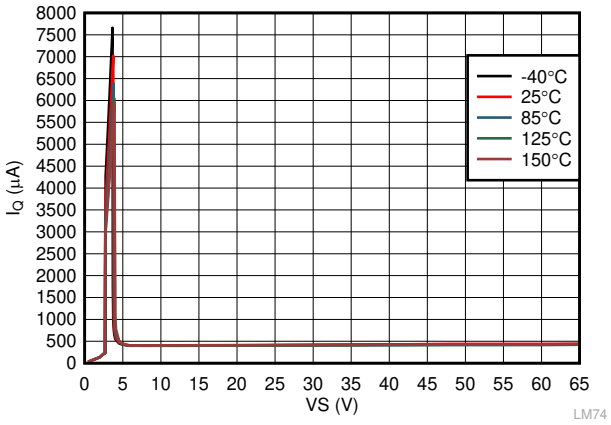


Figure 6-1. Operating Quiescent Current vs Supply Voltage

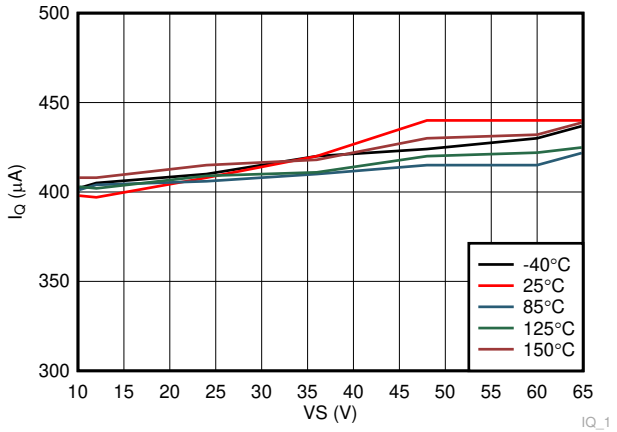


Figure 6-2. Operating Quiescent Current vs Supply Voltage (> 10 V)

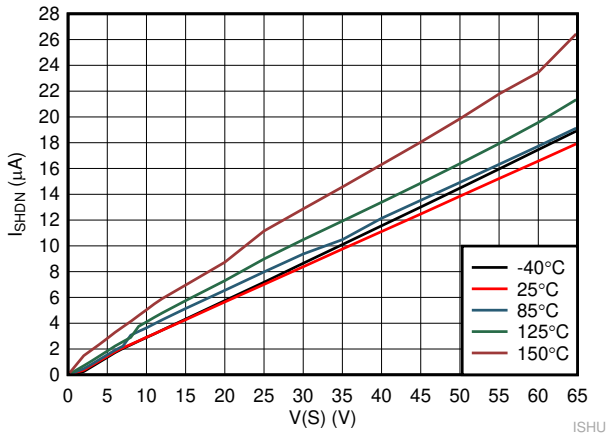


Figure 6-3. Shutdown Supply Current vs Supply Voltage

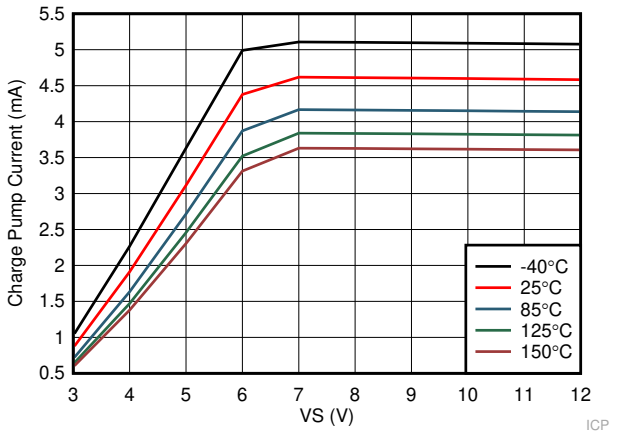


Figure 6-4. Charge Pump Current vs Supply Voltage at CAP = 6 V

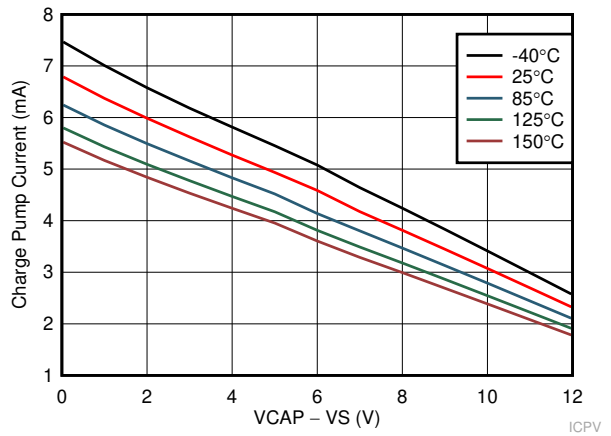


Figure 6-5. Charge Pump V-I Characteristics at VS > = 12 V

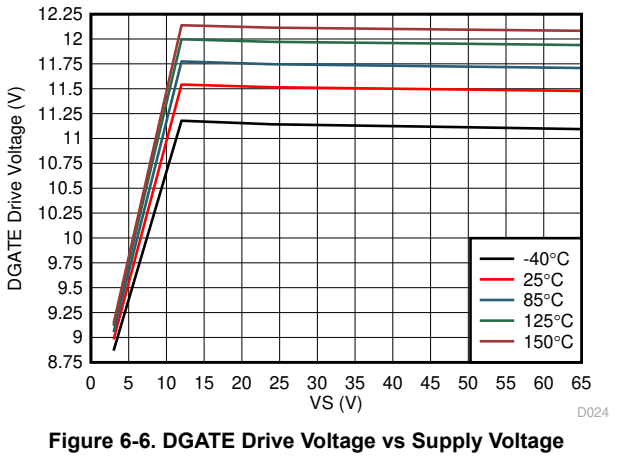


Figure 6-6. DGATE Drive Voltage vs Supply Voltage

6.7 Typical Characteristics (continued)

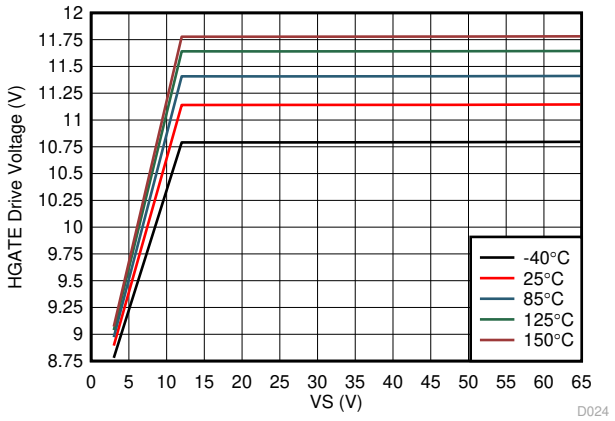


Figure 6-7. HGATE Drive Voltage vs Supply Voltage

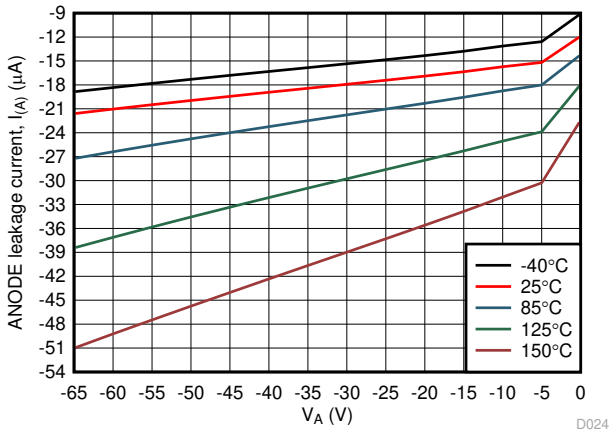


Figure 6-8. ANODE Leakage Current vs Reverse ANODE Voltage

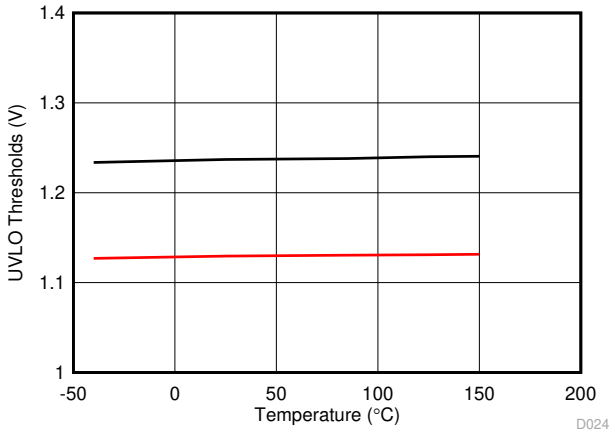


Figure 6-9. UVLO Thresholds vs Temperature

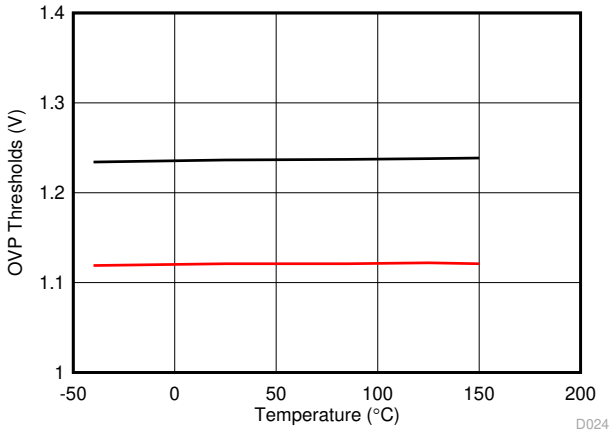


Figure 6-10. OVP Thresholds vs Temperature

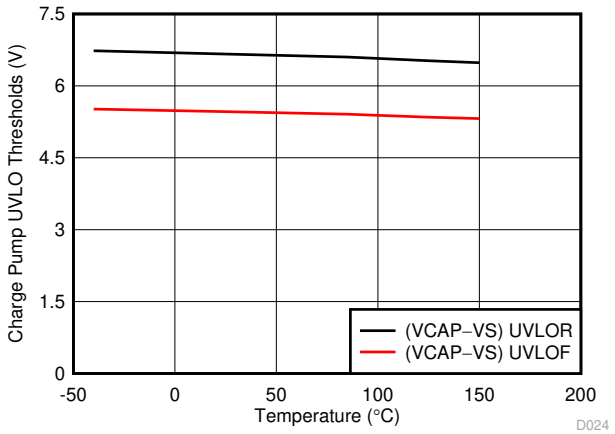


Figure 6-11. Charge Pump UVLO Threshold vs Temperature

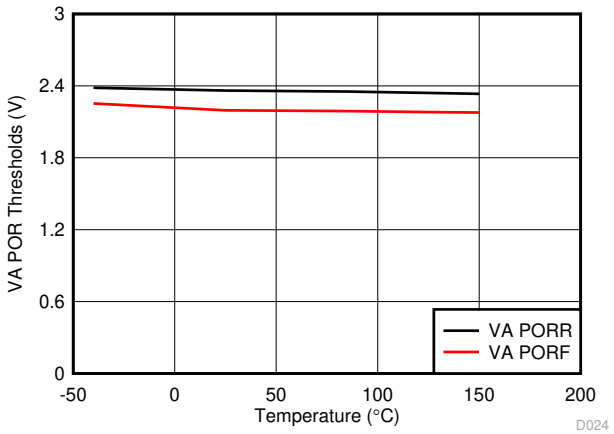


Figure 6-12. VA POR Threshold vs Temperature

6.7 Typical Characteristics (continued)

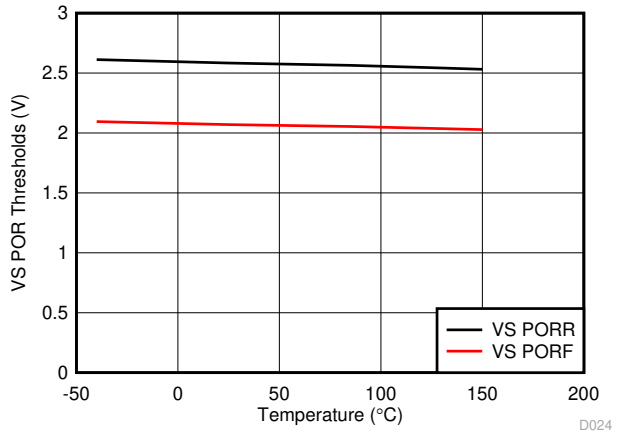


Figure 6-13. VS POR Threshold vs Temperature

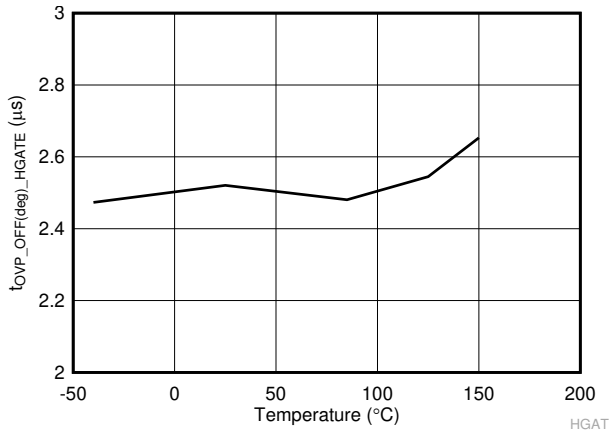


Figure 6-14. HGATE Turn OFF Delay during OV

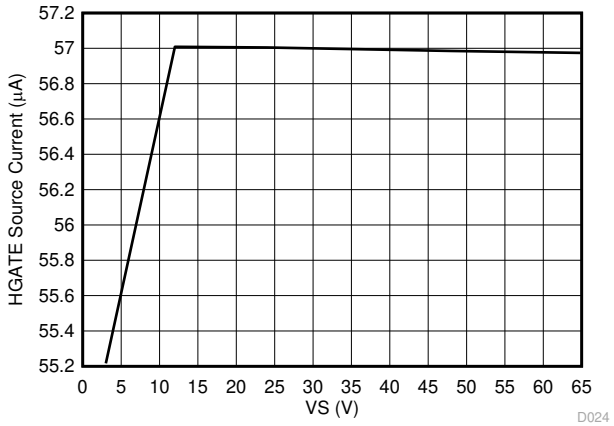


Figure 6-15. HGATE Current (IHGATE) vs Supply Voltage

7 Parameter Measurement Information

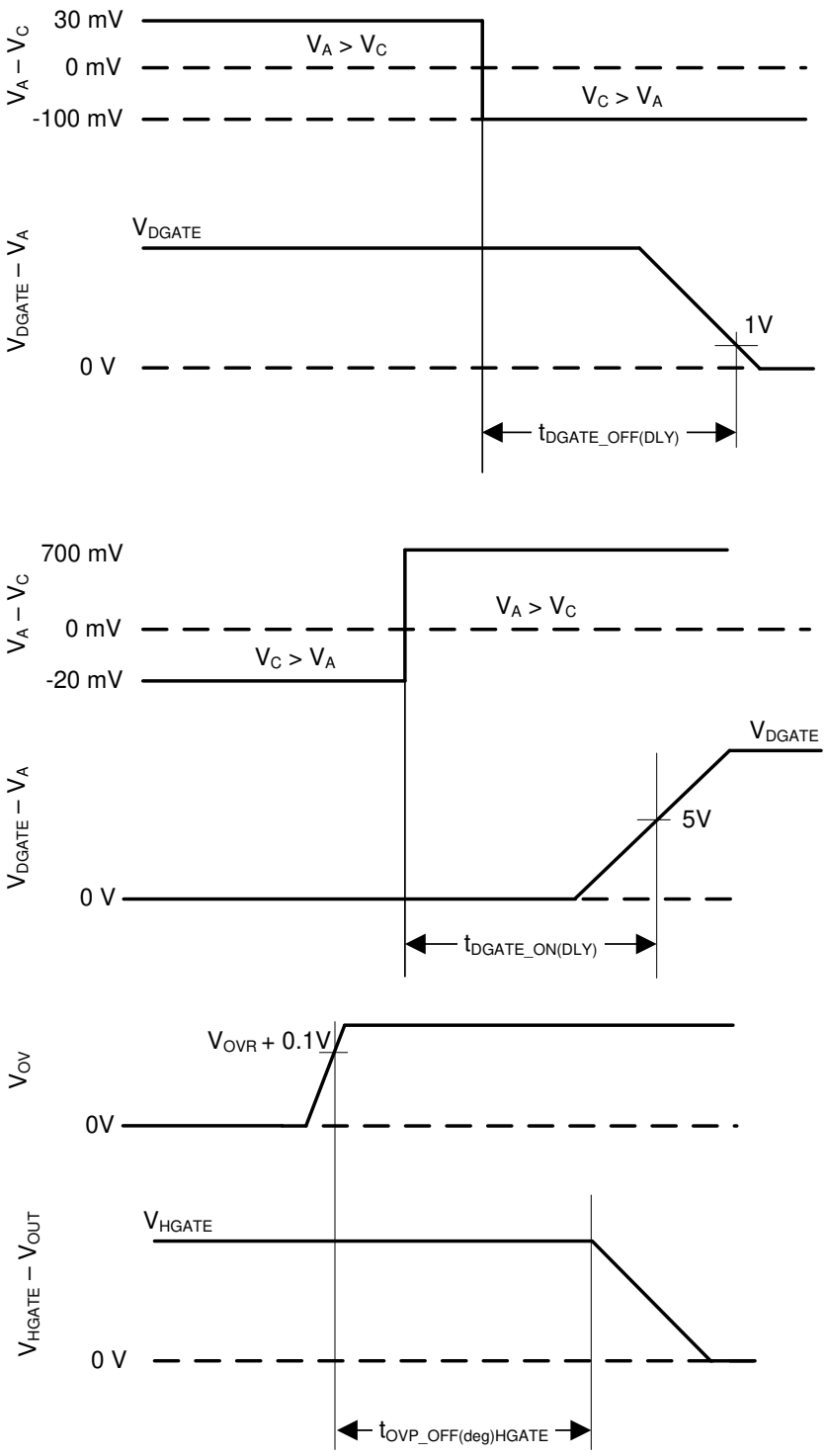


Figure 7-1. Timing Waveforms

8 Detailed Description

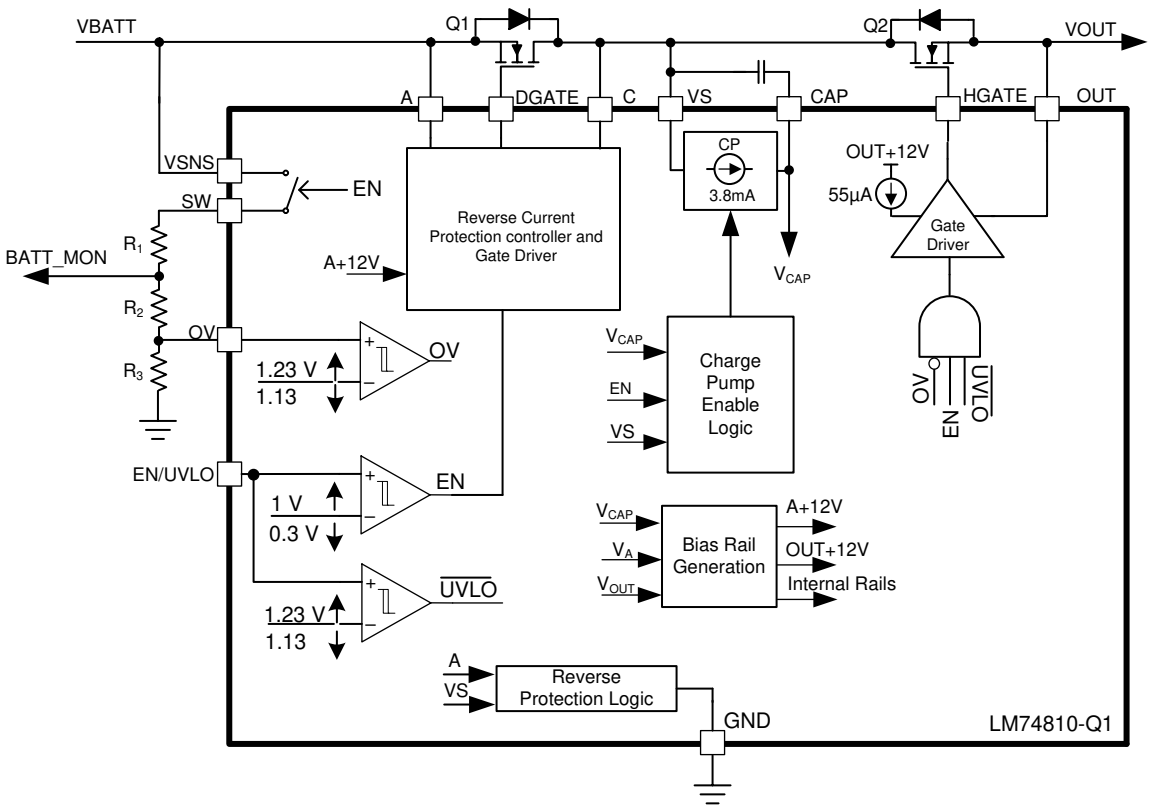
8.1 Overview

The LM74810-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control, inrush current limiting and over voltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong charge pump with 60-mA peak GATE source current driver stage and short turn ON and turn OFF delay times ensures fast transient response ensuring robust performance during automotive testing such as ISO16750 or LV124 where an ECU is subjected to AC superimpose input signals upto 200-KHz frequency. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and over voltage protection using HGATE control. The device features an adjustable over voltage cut-off protection feature using a programming resistor across SW and OVP terminal.

The LM74810-Q1 controls the DGATE of the MOSFET to regulate the forward voltage drop at 9.1 mV. The linear regulation scheme in these devices enables graceful control of the GATE voltage and turns off of the MOSFET during a reverse current event and ensures zero DC reverse current flow.

The device features enable control. With the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low 2.87 µA of current. The high voltage rating of LM74810-Q1 helps to simplify the system designs for automotive ISO7637 protection. The LM74810-Q1 are also suitable for ORing applications

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN/UVLO pin voltage must be above the specified input high threshold, $V_{(ENR)}$. When enabled, the charge pump sources a charging current of 3.8-mA typical. If EN/UVLO pin is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the CAP to VS voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 175\mu s + C_{(CAP)} x \frac{V_{(CAP\_UVLOR)}}{3.8mA} \quad (1)$$

where

- $C_{(CAP)}$ is the charge pump capacitance connected across VS and CAP pins
- $V_{(CAP\_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive approximately 1 V of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the CAP to VS voltage reaches 13.2 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the CAP to VS voltage is below to 12.2 V typically at which point the charge pump is enabled. The voltage between CAP and VS continue to charge and discharge between 12.2 V and 13.2 V as shown in Figure 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74810-Q1 is reduced. When the charge pump is disabled it sinks 15 µA.

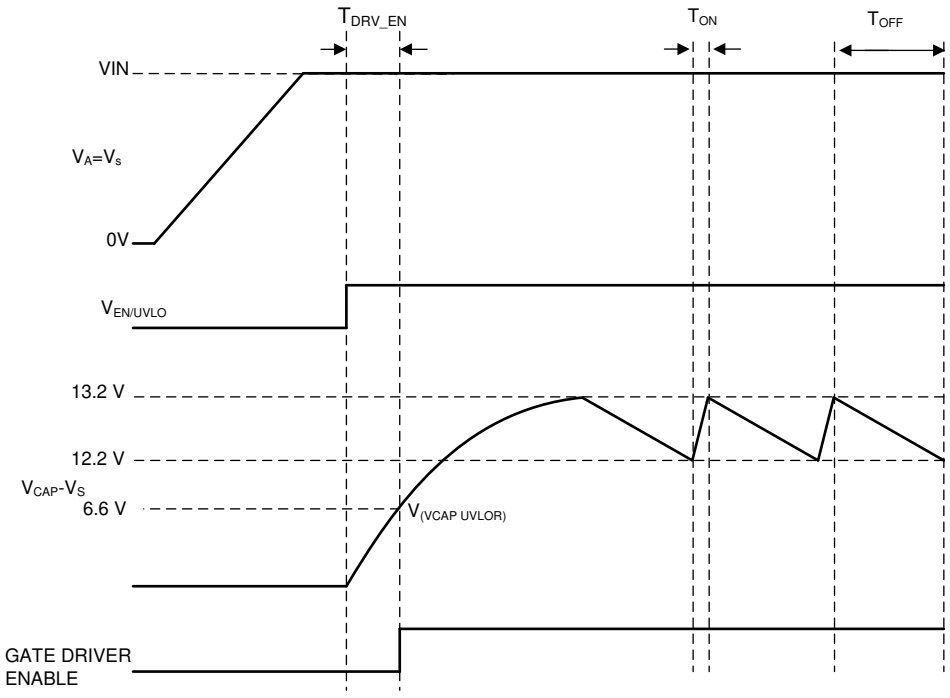


Figure 8-1. Charge Pump Operation

8.3.2 Dual Gate Control (DGATE, HGATE)

The LM74810-Q1 features two separate gate control and driver outputs to drive back to back N-channel MOSFETs.

8.3.2.1 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises of Ideal Diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to DGATE. The LM74810-Q1 has integrated reverse input protection down to –65 V.

Before the DGATE driver is enabled, following conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at A pin must be greater than VA POR Rising threshold.
- Voltage at Vs pin must be greater than Vs POR Rising thershold.

If the above conditions are not achieved, then the DGATE pin is internally connected to the A pin, assuring that the external MOSFET is disabled.

In LM74810-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 9.1 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74810-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{(AC\_REV)}$ threshold then the DGATE goes low within 0.5-µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{(AC\_FWD)}$ threshold within 0.85 µs (typ).

For Ideal Diode only designs, connect LM74810-Q1 as shown in Figure 8-2.

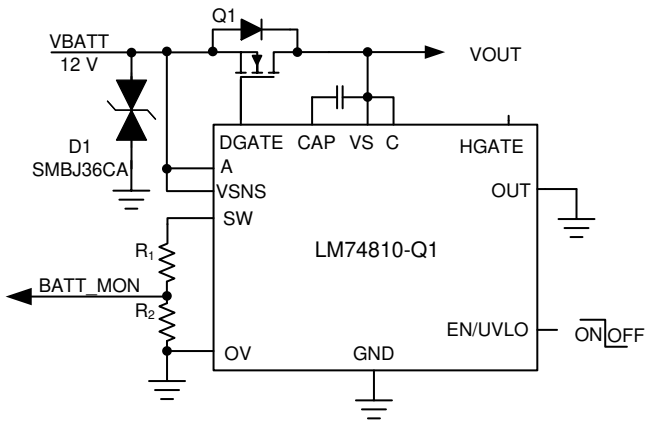


Figure 8-2. Configuring LM74810-Q1 for Ideal Diode Only

8.3.2.2 Load Disconnect Switch Control (HGATE, OUT)

HGATE and OUT comprises of Load disconnect switch control stage. Connect the Source of the external MOSFET to OUT and Gate to HGATE.

Before the HGATE driver is enabled, following conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at Vs pin must be greater than Vs POR Rising thershold.

If the above conditions are not achieved, then the HGATE pin is internally connected to the OUT pin, assuring that the external MOSFET is disabled.

For Inrush Current limiting, connect C_{dVdT} capacitor and R_1 as shown in Figure 8-3.

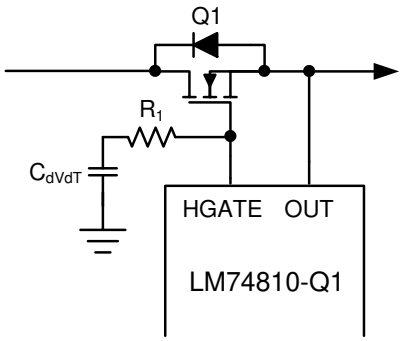


Figure 8-3. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate C_{dVdT} capacitance value .

$$C_{dVdT} = \frac{I_{HGATE\_DRV}}{I_{INRUSH}} xC_{OUT} \quad (2)$$

where I_{HATE_DRV} is 55 µA (typ), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn off time.

For Load disconnect switch only designs, configure the LM74810-Q1 as shown in Figure 8-4

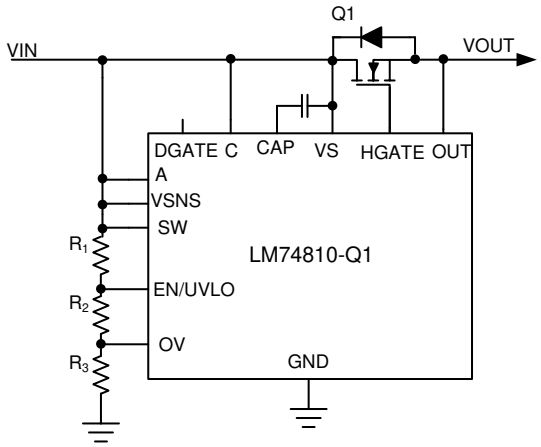


Figure 8-4. Configuring LM74810-Q1 for Load Disconnect Switch Only

8.3.3 Over Voltage Protection and Battery Voltage sensing (VSNS, SW, OV)

Connect a resistor ladder as shown in Figure 8-5 for Over Voltage threshold programming.

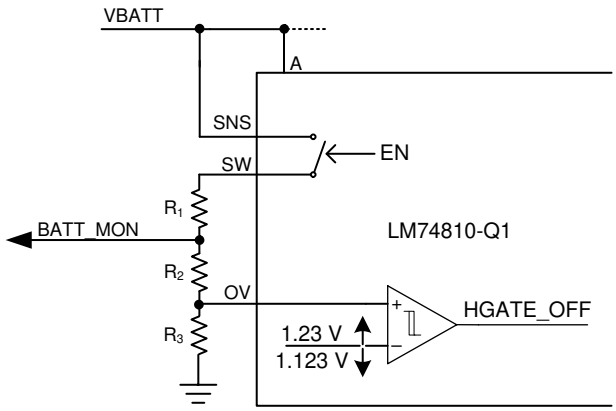


Figure 8-5. Programming Over Voltage Threshold and Battery Sensing

A disconnect switch is integrated between VSNS and SW pins. This switch is turned OFF when EN/UVLO pin is pulled low. This helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

8.3.4 Low Iq Shutdown and Under Voltage Lockout (EN/UVLO)

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in Charge Pump section. If EN/UVLO pin voltage is less than the input low threshold, $V_{(ENF)}$, the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM74810-Q1 in shutdown mode.

If $V_{(ENF)} < V_{(EN/UVLO)} < V_{(UVLOF)}$ then only HGATE is disabled disconnecting the load from the supply, DGATE remains ON.

The EN/UVLO pin can withstand a maximum voltage of 65 V. For always ON operation connect EN/UVLO pin to VS.

8.4 Device Functional Modes

The LM74810-Q1 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold $V_{(ENF)}$. Both the gate drivers and the charge pump are disabled in shutdown mode. During shutdown mode the LM74810-Q1 enters low IQ operation with a total input quiescent consumption of 2.87 µA (typ). When the LM74810-Q1 is in shutdown mode, forward current flow to always ON loads connected to the common drain point of the back to back MOSFETs is not interrupted but is conducted through the MOSFET's body diode.

8.5 Application Examples

8.5.1 Redundant Supply OR-ing with Inrush Current Limiting, Over Voltage Protection and ON/OFF Control

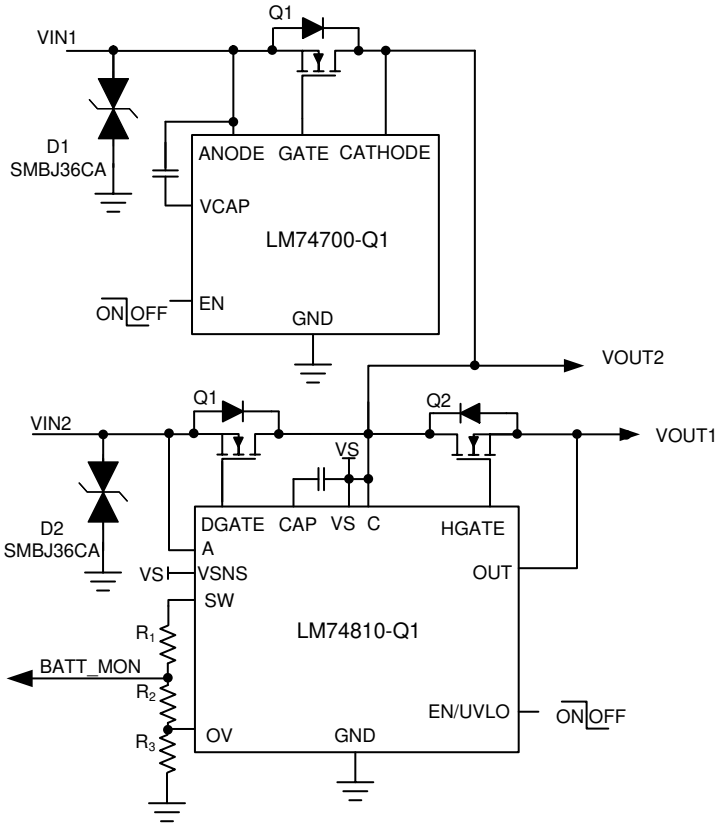


Figure 8-6. Redundant Supply OR-ing with Over Voltage Protection and ON/OFF Control

Figure 8-6 shows the implementation of Dual OR-ing with Inrush Current Limiting, Over Voltage Protection and power path ON/OFF control. The input side SMBJ36CA TVS across the ideal diodes is required for ISO7637 Pulse 1 transient suppression to limit the input voltage within the device max voltage rating of –65 V.

R1 and R2 are the programming resistors for over voltage protection (OVP) threshold. When the voltage at OVP pin exceeds OVP cut-off reference threshold then the HGATE driver turns OFF the FET Q3, disconnecting the power path and protecting the downstream load. HGATE goes high once the OVP pin voltage goes below the OVP falling hysteresis threshold. Use 0.1-µF to 1-µF capacitor across VS to CAP pins of the LM74810-Q1. This is the charge pump capacitor and acts as the supply for both the DGATE and HGATE driver stages. The DGATE driver of the LM74810-Q1 is equipped with 60-mA peak source current and 1.5-A peak sink current capability resulting in fast and efficient transient responses during the ISO16750 or LV124 short interruptions as well as AC superimpose testing.

Pull EN low during the sleep/standby mode. With EN low, both the DGATE and HGATE drivers are pulled low turning OFF both the power FETs. VOUT1 gets disconnected from the VBATT rail reducing the system I_Q. VOUT2 is gets power through the body diode of the MOSFET Q2 and this supply can be utilized for always ON loads. The LM74810-Q1 draws a 2.87-µA current during this mode.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

LM74810-Q1 controls two N-channel power MOSFETs with DGATE used to control diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during an over voltage protection. HGATE controlled MOSFET can be used to clamp the output during over voltage or load dump conditions. LM74810-Q1 can be placed into low quiescent current mode using EN/UVLO, where both DGATE and HGATE are turned OFF.

9.2 Typical 12-V Reverse Battery Protection Application

A typical application circuit of LM74810-Q1 configured to provide reverse battery protection with over voltage protection is shown in Figure 9-1.

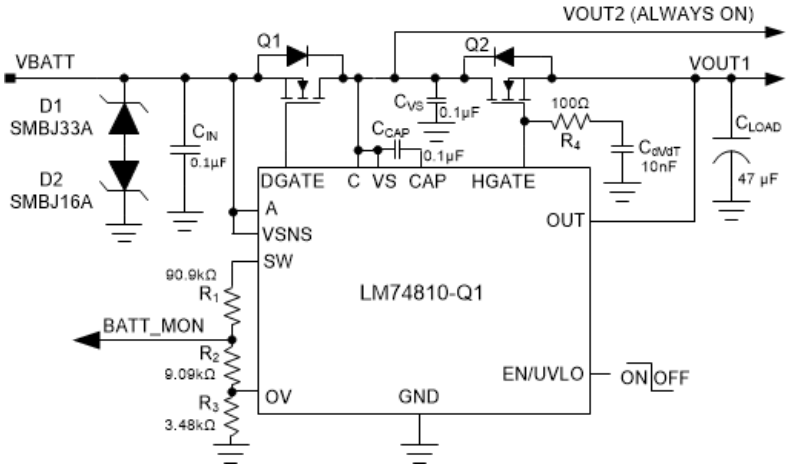


Figure 9-1. Typical Application Circuit - 12-V Reverse Battery Protection and Over Voltage Protection

9.2.1 Design Requirements for 12-V Battery Protection

The system design requirements are listed in Table 9-1.

Table 9-1. Design Parameters - 12-V Reverse Battery Protection and Over Voltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	12-V battery, 12-V nominal with 3.2-V Cold Crank and 35-V Load Dump
Output Power	200 W
Output Current Range	12-A Nominal, 18-A maximum
Input Capacitance	0.1-µF minimum
Output Capacitance	0.1-µF minimum, (optional 470bµF for E-10 functional class A performance)
Over Voltage Cut-off	37.0 V, output cut-off >37.0 V
AC Super Imposed Test	2-V Peak-Peak to 6-V Peak-Peak, 20 Hz to 30 KHz extendable to 200 KHz
Automotive Transient Immunity Compliance	ISO 7637-2, ISO 16750-2 and LV124
Battery Monitor Ratio	8:1

9.2.2 Automotive Reverse Battery Protection

The LM74810-Q1 feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs. This enables LM74810-Q1 to provide comprehensive immunity with robust system protection during various automotive transient tests as per ISO 7637-2 and ISO 16750-2 standard as well as other automotive OEM standards. For more information, see the *Automotive EMC-compliant reverse-battery protection with ideal-diode controllers* article.

LM74810-Q1 gate drive output DGATE controls MOSFET Q1 to provide reverse battery protection and true reverse current blocking functionality. HGATE controls MOSFET Q2 to turn off the power path during input over voltage condition. Resistor network R1, R2 and R3 connected to OV and SW can be configured for over voltage protection and also for battery monitoring under normal operating conditions as well as reverse battery conditions. TVS D1 and D2 clamps the automotive transient input voltages on the 12-V battery, both positive and negative transients, to voltage levels safe for MOSFET Q1 and LM74810-Q1.

Fast reverse current blocking response and quick reverse recovery enables LM74810-Q1 to turn ON/OFF MOSFET Q1 during AC super imposed input specified by ISO 16750-2 and LV124 E-06 and provide active rectification of the AC input superimposed on DC battery voltage. Fast reverse current blocking response of LM74810-Q1 helps to turn off MOSFET Q1 during negative transients inputs such as –150-V 2-ms Pulse 1 specified in ISO 7637-2 and input micro short conditions such as LV124 E-10 test.

9.2.3 Input Transient Protection: ISO 7637-2 Pulse 1

ISO 7637-2 Pulse 1 specifies negative transient immunity of electronic modules connected in parallel with an inductive load when the battery is disconnected. A typical pulse 1 specified in ISO 7637-2 starts with battery disconnection where supply voltage collapses to 0 V followed by –150 V 2 ms applied with a source impedance of 10 Ω at a slew rate of 1 µs on the supply input. LM74810-Q1 blocks reverse current and prevents the output voltage from swinging negative, protecting the rest of the electronic circuits from damage due to negative transient voltage. MOSFET Q1 is quickly turned off within 0.5 µs by fast reverse comparator of LM74810-Q1.

A single bi-directional TVS or two uni-directional TVS are required at the input to clamp the negative transient pulse within the operating maximum voltage across cathode to anode of 85 V and does not violate the MOSFET Q1 drain-source breakdown voltage rating. ISO 7637-2 Pulse 1 performance of LM74810-Q1 is shown in Figure 9-2.

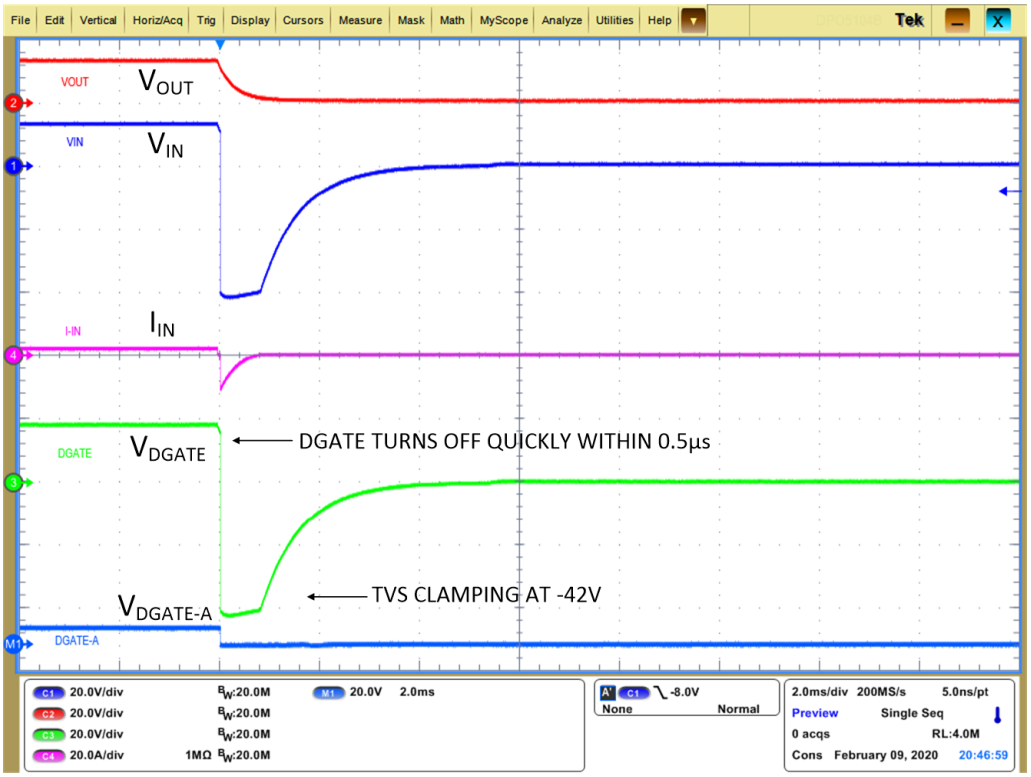


Figure 9-2. ISO 7637-2 Pulse 1

9.2.4 AC Super Imposed Input Rectification: ISO 16750-2 and LV124 E-06

Alternators are used to power the automotive electrical system and charge the battery during normal runtime of the vehicle. Rectified alternator output contains residual AC ripple voltage superimposed on the DC battery voltage due to various reasons which includes engine speed variation, regulator duty cycle with field switching ON/OFF and electrical load variations. On a 12-V battery supply, alternator output voltage is regulated by a voltage regulator between 14.5 V to 12.5 V by controlling the field current of alternator's rotor. All electronic modules are tested for proper operation with superimposed AC ripple on the DC battery voltage. AC super imposed test specified in ISO 16750-2 and LV124 E-06 requires AC ripple of 2-V Peak-Peak on a 13.5-V DC battery voltage, swept from 15 Hz to 30 KHz and extended to 200 KHz in case of LV148 E48-05. LM74810-Q1 rectifies the AC superimposed voltage by turning the MOSFET Q1 OFF quickly to cut-off reverse current and turning the MOSFET Q1 ON quickly during forward conduction.

Active rectification of 2-V peak-peak 200 KHz AC input by LM74810-Q1 is shown in Figure 9-3. Fast turn off and quick turn ON of the MOSFET reduces power dissipation in the MOSFET Q1 and active rectification reduces power dissipation in the output hold-up capacitor's ESR by half. Active rectification of 2-V peak-peak 5-KHz AC input is shown in Figure 9-4.

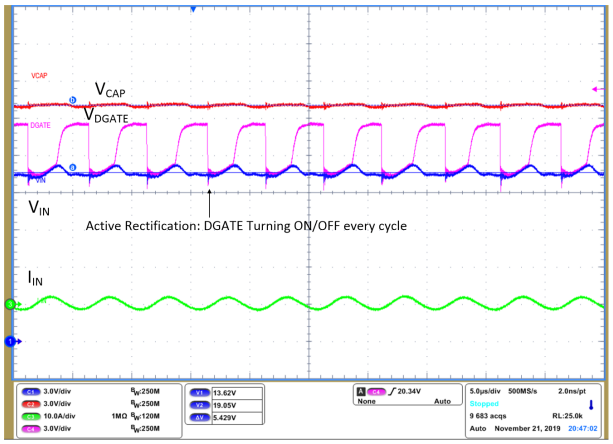


Figure 9-3. AC Super Imposed Test on 15 nC Q_{GS}-2-V Peak-Peak 200 KHz

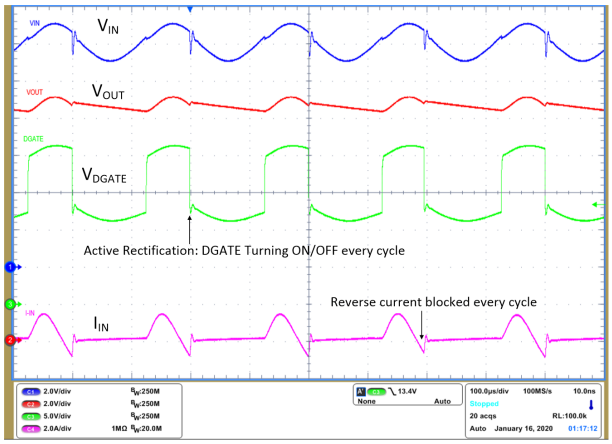


Figure 9-4. AC Super Imposed Test - 2-V Peak-Peak 5 KHz

9.2.5 Input Micro-Short Protection: LV124 E-10

E-10 test specified in LV124 standard checks for immunity of electronic modules to short interruptions in power supply input due to contact issues or relay bounce. During this test (case 2), micro-short is applied on the input for a duration as low as 10 µs to several ms. For a functional pass status A, electronic modules are required to run uninterrupted during the E-10 test (case 2) with 100-µs duration. Dual-Gate drive architecture of LM74810-Q1 - DGATE and HGATE - enables to achieve a functional pass status A with optimum hold up capacitance on the output when compared to a single gate drive controller. When input micro-short is applied for 100 µs, LM74810-Q1 quickly turns off MOSFET Q1 by shorting DGATE to ANODE (source of MOSFET) within 0.5 µs to prevent the output from discharging and the HGATE remains ON keeping MOSFET Q2 ON, enabling fast recovery after the input short is removed.

Performance of LM74810-Q1 during E10 input power supply interruption test case 2 is shown in Figure 9-5. After the input short is removed, input voltage recovers and MOSFET Q1 is turned back ON within 130 µs. Note that dual-gate drive topology allows MOSFET Q2 to remain ON during the test and helps in restoring the input power faster. Output voltage remains unperturbed during the entire duration, achieving functional status A.

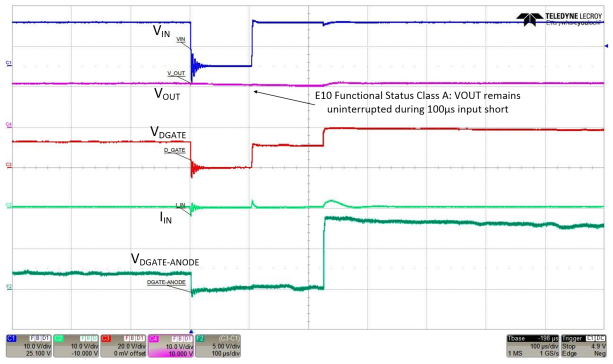


Figure 9-5. Input Micro-Short - LV124 E10 TC 2 100 µs

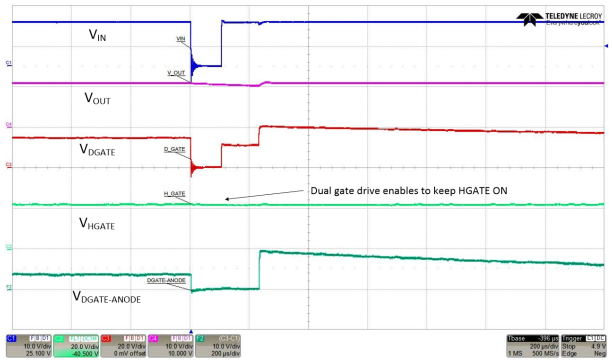


Figure 9-6. Input Micro-Short - LV124 E10 TC 2 100 µs with HGATE

9.2.6 Detailed Design Procedure

9.2.6.1 Design Considerations

Table 9-1 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with over voltage cut-off. During power up, inrush current through MOSFET Q2 needs to be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2 and maximum operating voltage

determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q2 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple and ISO 7637-2 pulse 1 requirements. Over voltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2 and LM74810-Q1.

9.2.6.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capactiance of Q2 $C_{ISS(MOSFET)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET\_Q1)}$ + $C_{ISS(MOSFET\_Q2)}$) (µF).

9.2.6.3 Input and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

9.2.6.4 Hold-up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74810-Q1 is based on the UVLO settings of downstream DC-DC converters. For this design, 4.0-V drop in output voltage for 100 µs is considered and the minimum hold-up capacitance required is calculated by

$$C_{HOLD\_UP\_MIN} = \frac{I_{LOAD\_MAX}}{dV_{OUT}} x 100\mu s \tag{3}$$

Minimum hold-up capacitance required to hold output with 4.0-V drop at 18-A current for 100 µs is 450 µF. A 470-uF electrolytic capacitor is a closest standard value that can be placed at the output. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

9.2.6.5 Over Voltage Protection and Battery Monitor

Resistors R_1, R_2 and R_3 connected in series are used to program the over voltage threshold and battery monitor ratio. The resistor values required for setting the over voltage threshold V_{OV} to 37.0 V and battery monitor ratio V_{BATT_MON} : V_{BATT} to 1:8 are calculated by solving Equation 4 and Equation 5.

$$V_{OVR} = \frac{R_3}{R_1 + R_2 + R_3} x V_{OV} \tag{4}$$

$$V_{BAT\_MON} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} x V_{BATT} \tag{5}$$

For minimizing the input current drawn from the battery through resistors R_1, R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_1 + R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{OVR} is 1.23 V and battery monitor ratio (V_{BATT_MON} / V_{BATT}) is designed for a ratio of 1/8. To limit (R_1 + R_2 + R_3) < 120 kΩ, select (R_1 + R_2) = 100 kΩ. Solving Equation 4 gives

R_3 = 3.45 kΩ. Solving Equation 5 for R2 using (R_1 + R_2) = 100 kΩ and R_3 = 3.45 kΩ, gives R_2 = 9.48 kΩ and R_1 = 90.52 kΩ.

Standard 1% resistor values closest to the calculated resistor values are R1 = 90.9 kΩ, R2 = 9.09 kΩ and R3 = 3.48 kΩ.

9.2.7 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include all the automotive transient events and any anticipated fault conditions. It is recommended to use MOSFETs with V_{DS} voltage rating of 60 V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back-back at the input.

The maximum V_{GS} LM74810-Q1 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level, but this would result in increased I_Q current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74810-Q1's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point.

For active rectification of AC super imposed ripple on the battery supply voltage, gate-source charge Q_{GS} of Q1 must be selected to meet the required AC ripple frequency. Maximum gate-source charge Q_{GS} (at 4.5-V V_{GS}) for active rectification every cycle is

$$Q_{GS\_MAX} = \frac{2.5mA}{F_{AC\_RIPPLE}} \tag{6}$$

where 2.5 mA is minimum charge pump current at 7-V V_{DGATE} - V_A, F_{AC_RIPPLE} is frequency of the AC ripple superimposed on the battery and Q_{GS_MAX} is the Q_{GS} value specified in manufacturer datasheet at 6-V V_{GS}. For active rectification at F_{AC_RIPPLE} = 30 KHz, Q_{GS_MAX} = 83 nC. Further for active rectification at F_{AC_RIPPLE} = 200 KHz, Q_{GS_MAX} = 12.5 nC.

Based on the design requirements, BUK9J0R9-40H MOSFET is selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and 16-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 0.97-mΩ typical at 4.5-V V_{GS} and 0.82 mΩ rated at 10-V V_{GS}
- MOSFET Q_{GS_MAX} 30.2 nC

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.8 MOSFET Selection: Hot-Swap MOSFET Q2

The V_{DS} rating of the MOSFET Q2 should be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12-V design, transient over voltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2 A 50 V for 50 µs. Further, ISO 7637-2 Pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors and the maximum voltage on the 12-V battery can be limited to < 40 V the minimum recommended input capacitance of 0.1 µF. The 50-V SO 7637-2 Pulse 2 A can also be absorbed by input and output capacitors and its amplitude could be reduced to 40-V peak by placing sufficient amount of capacitance at input and output. For this 12-V design, a 40-V V_{DS} rated MOSFET is selected.

The VGS rating of the MOSFET Q2 should be higher than that maximum HGATE-OUT voltage 15 V.

Inrush current through the MOSFET during input hot-plug into the 12-V battery is determined by output capacitance. External capacitor on HGATE, C_{DVDT} is used to limit the inrush current during input hot-plug or startup. The value of inrush current determined by Equation 2 need to be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA). Considering C_{OUT} = 470 µF and inrush current of 2.5 A, the calculated value of C_{DVDT} is 9.96 nF. Closest standard value of 10.0 nF is chosen for this design.

Duration of inrush current is calculated by

$$dT_{INRUSH} = \frac{12}{I_{INRUSH}} xC_{OUT} \tag{7}$$

Calculated inrush current duration is 2.36 ms with 2.5-A inrush current.

MOSFET BUK9J0R9-40H having 40-V V_{DS} and 16 V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET's safe operating area (SOA).

9.2.9 TVS selection

For 40-V rated MOSFET, two bi-directional 600-W SMBJ TVS, SMBJ33A and SMBJ16A are recommended for input transient clamping and protection. For detailed explanation on TVS selection for 12-V battery systems, refer to *TVS Selection for 12-V Battery Systems* and refer to *TVS Selection for 24-V Battery Systems* for 24-V battery systems.

9.2.10 Application Curves

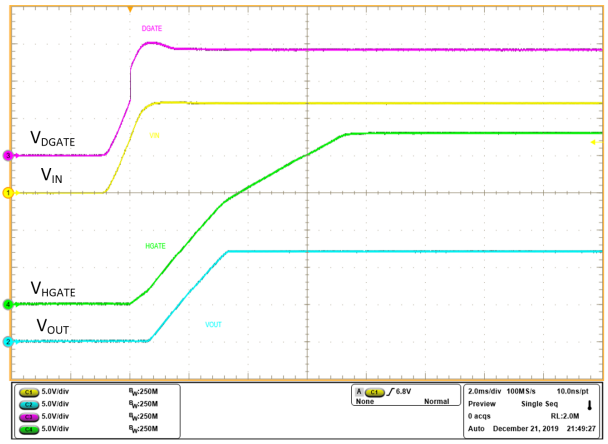


Figure 9-7. Startup 12 V with EN pulled to VIN

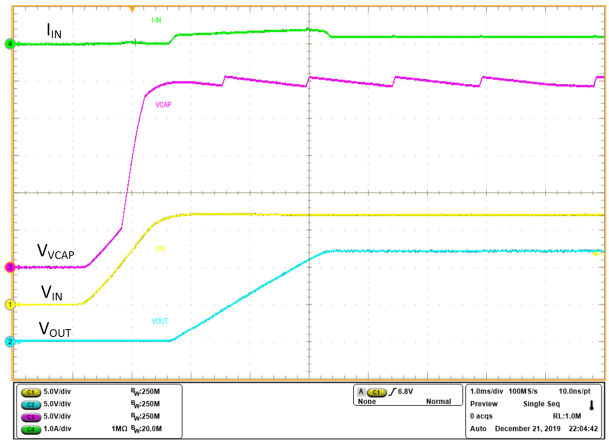


Figure 9-8. Startup 12 V showing Charge Pump VCAP

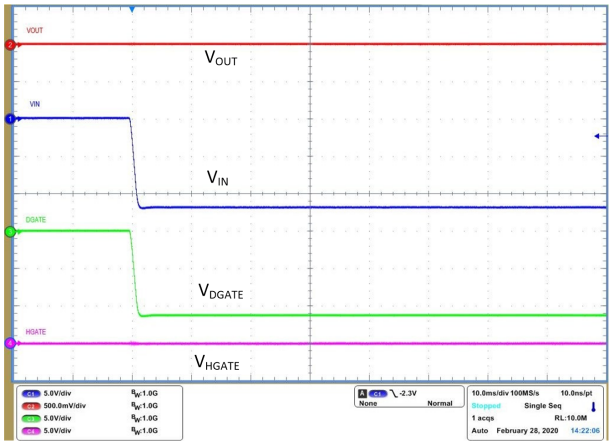


Figure 9-9. Reverse Input Voltage -12 V

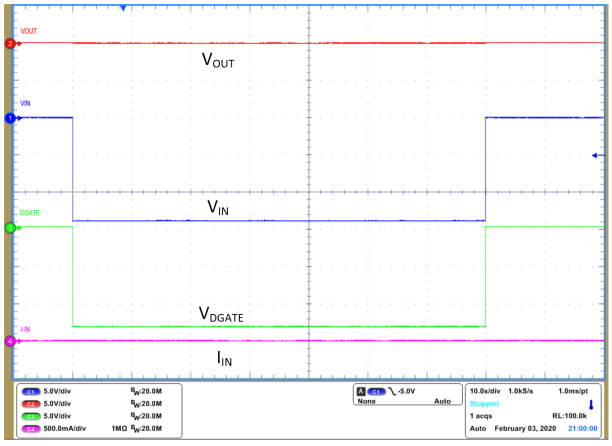


Figure 9-10. Reverse Input Voltage -12 V for 60s

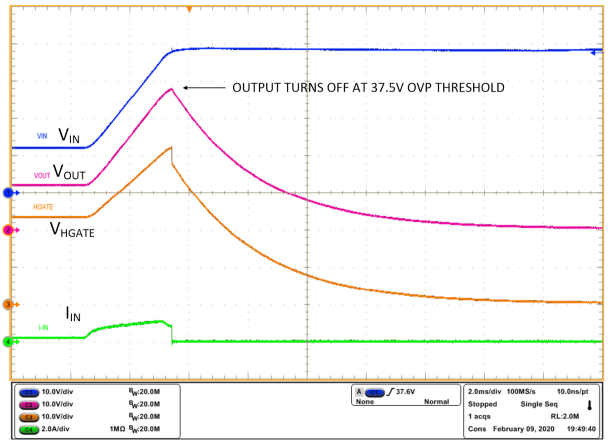


Figure 9-11. Over Voltage Cut-off

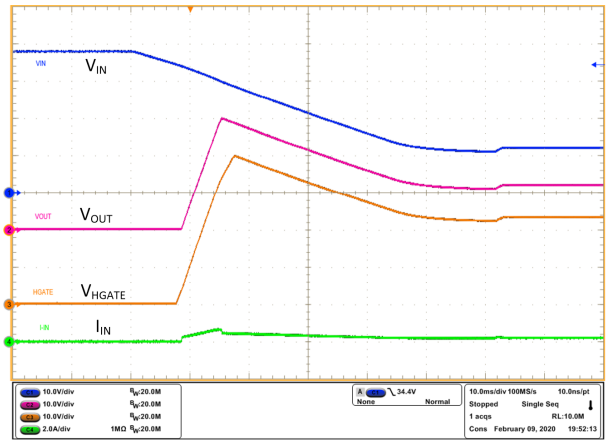


Figure 9-12. Over Voltage Recovery

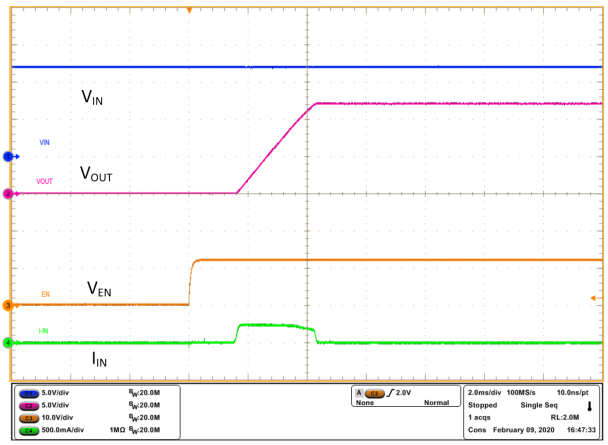


Figure 9-13. Turn ON with ENABLE Control

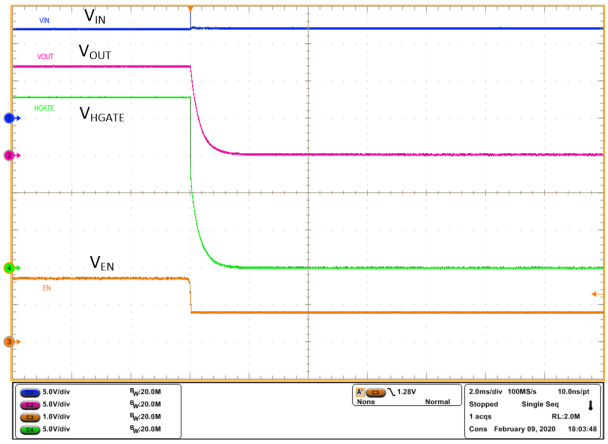


Figure 9-14. Turn OFF with ENABLE Control

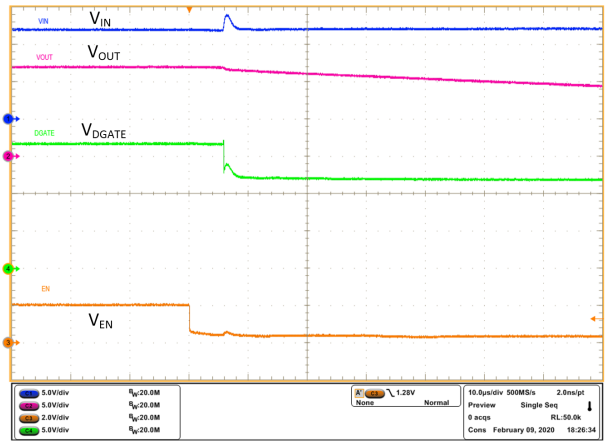


Figure 9-15. Disable Delay DGATE

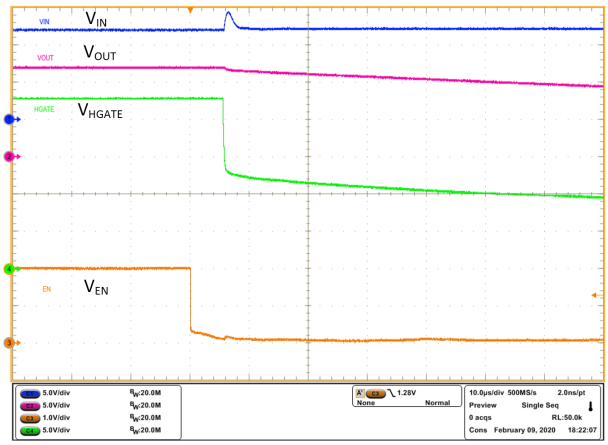


Figure 9-16. Disable Delay HGATE

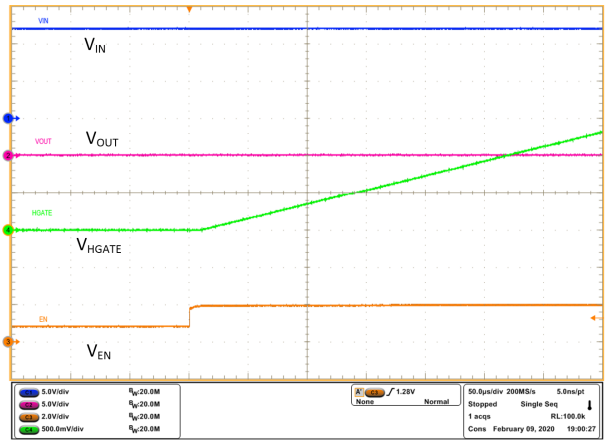


Figure 9-17. Enable Delay HGATE

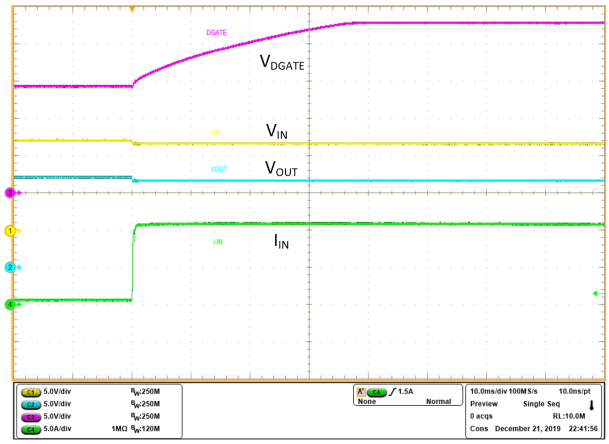


Figure 9-18. Load Transient Response DGATE

9.3 Do's and Don'ts

Leave exposed pad (RTN) of the IC floating. Do not connect it to the GND plane. Connecting RTN to GND disables the Reverse Polarity protection feature.

10 Power Supply Recommendations

10.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as over voltage cut-off, reverse current blocking, EN/UVLO causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 8.

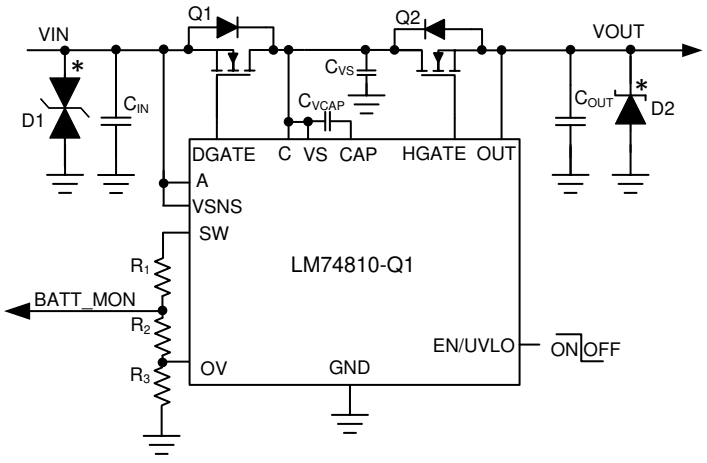
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (8)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 10-1



* Optional components needed for suppression of transients

Figure 10-1. Circuit Implementation with Optional Protection Components for LM74810-Q1

10.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74810-Q1 (65 V). The breakdown voltage of TVS- should be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM74810-Q1 (85 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 40-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 40 V.

During ISO 7637-2 pulse 1, the anode of LM74810-Q1 is pulled down by the ISO pulse, clamped by TVS- and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- should not exceed, (40 V – 16) V = –24 V.

On the positive side, the SMBJ33A TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side. On the negative side, TVS has to withstand 16-V reverse battery connection and clamping voltage has to be –(40 V - 16 V) = –24 V. SMBJ16A can be used.

However if 60-V rated MOSFET is selected, a single bi-directional TVS SMBJ33CA is recommended. SMBJ series of TVS' are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

10.3 TVS Selection for 24-V Battery Systems

For 24-V battery protection application, the TVS and MOSFET Q1 and Q2 needs to be changed to suit 24-V battery requirements.

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74810-Q1 (70 V) and should withstand 65-V suppressed load dump. The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12-A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (-TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- should not exceed, 85 V – 32 V = 53 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65V, maximum clamping voltage is ≤ 53 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ28A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ28A and SMBJ58A connected back-back at the input.

11 Layout

11.1 Layout Guidelines

- For the ideal diode stage, connect A, DGATE and C pins of LM74810-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- For the load disconnect stage, connect HGATE and OUT pins of LM74810-Q1 close to the MOSFET's GATE and SOURCE pins.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick and short traces for source and drain of the MOSFET to minimize resistive losses.
- The DGATE pin of the LM74810-Q1 must be connected to the MOSFET GATE with short trace.
- Place transient suppression components close to LM74810-Q1.
- Place the decopuling capacitor, C_{VS} close to VS pin and chip GND.
- The charge pump capacitor across CAP and VS pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and to produce good results.

11.2 Layout Example

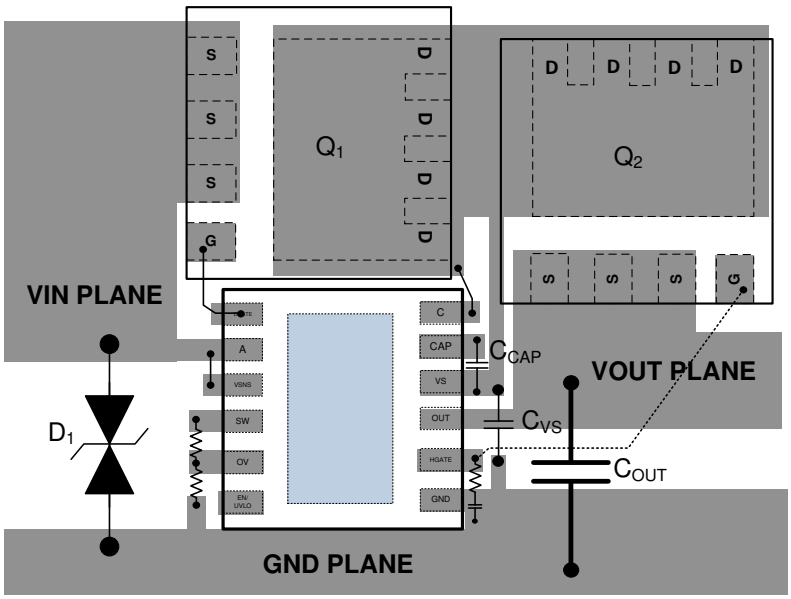


Figure 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74810QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L74810	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

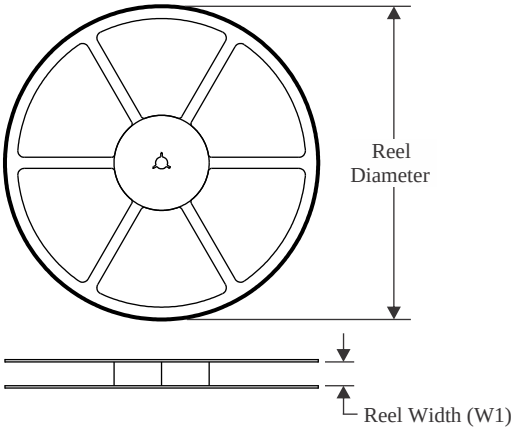
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

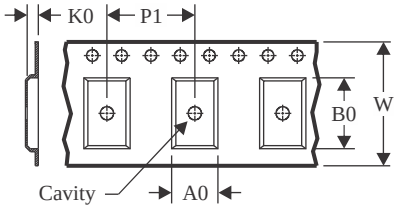
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

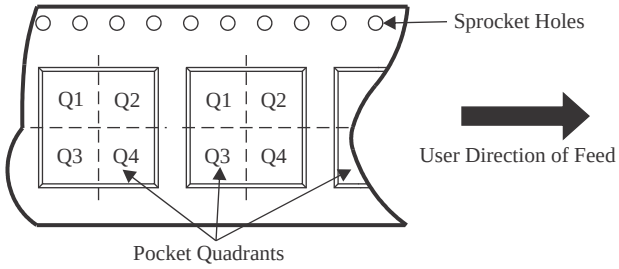


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

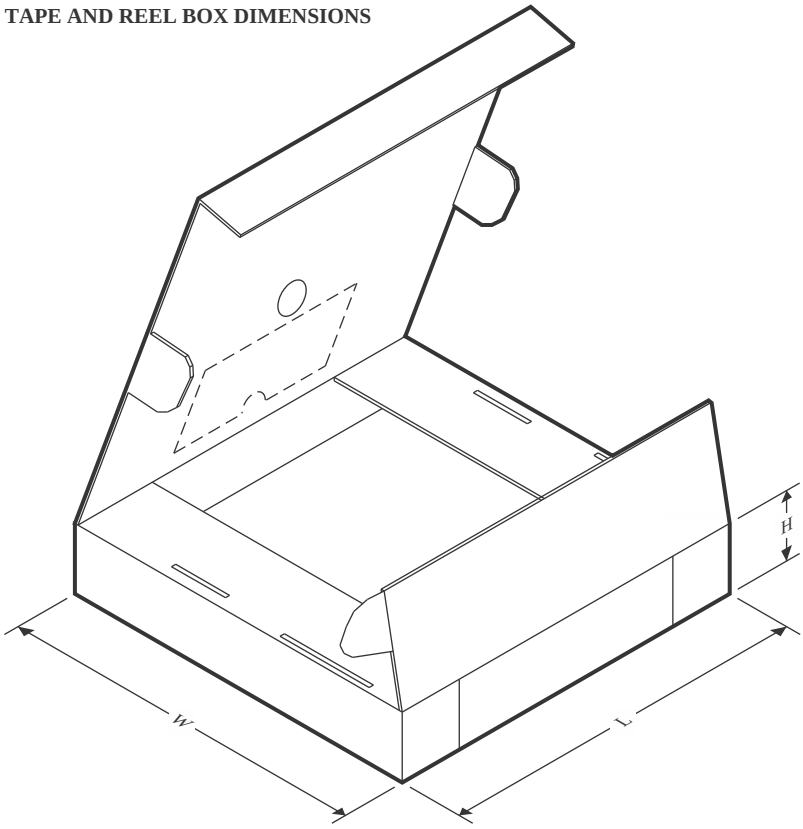
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74810QDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



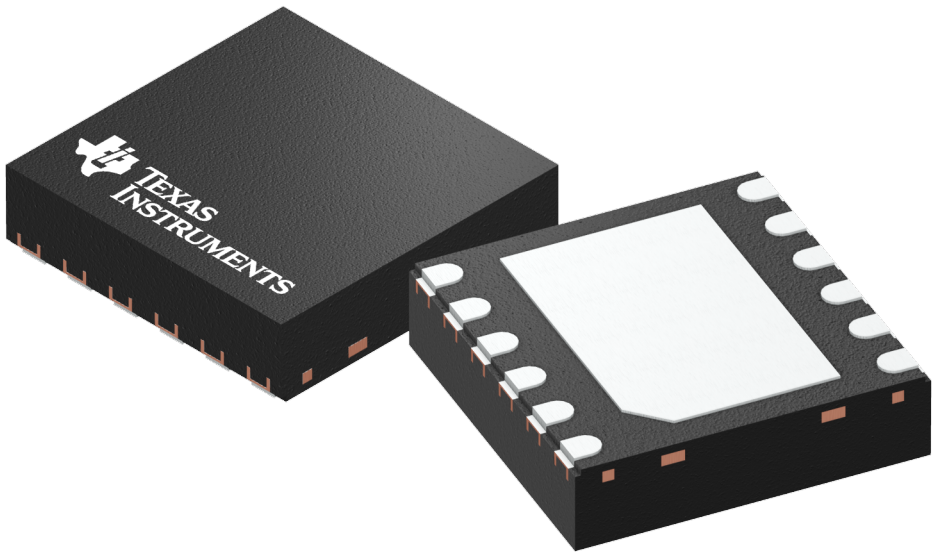
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74810QDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

DRR 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

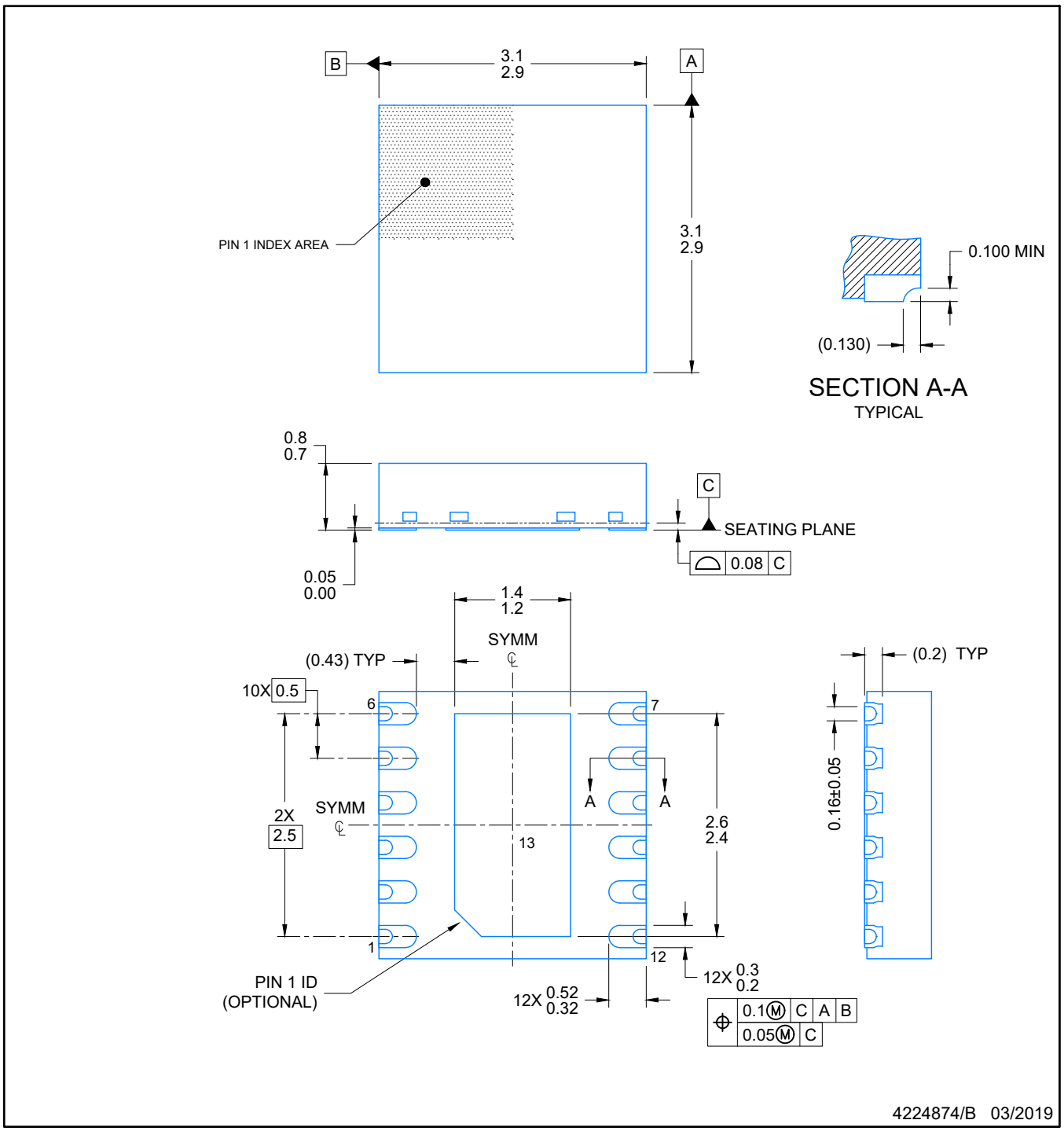
4223490/A

PACKAGE OUTLINE

DRR0012E

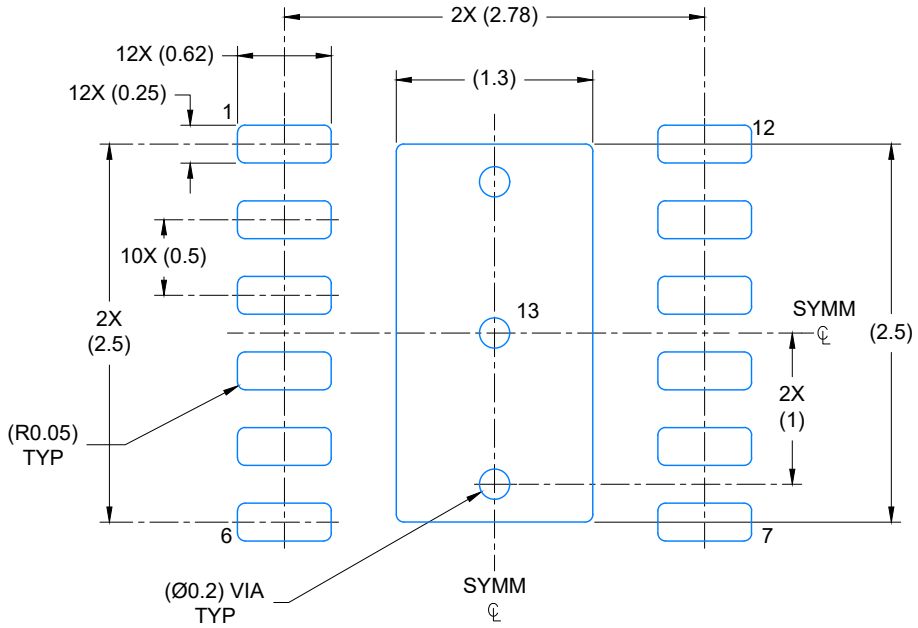
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

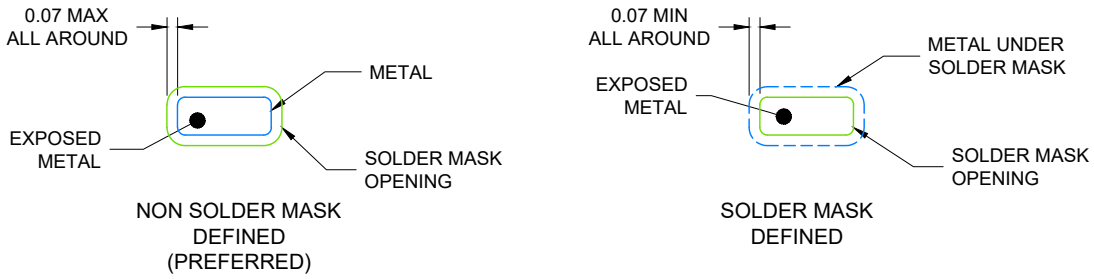


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

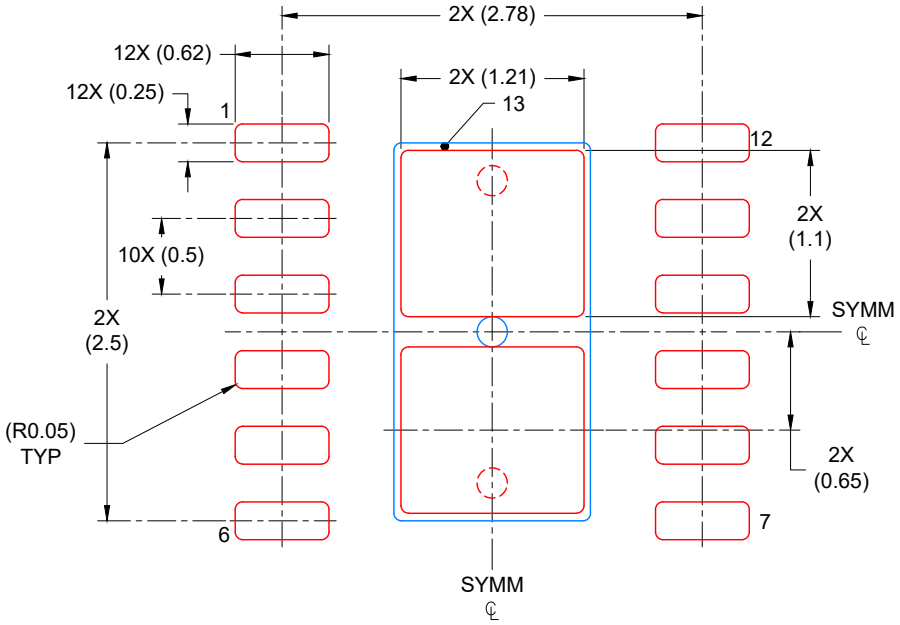


SOLDER MASK DETAILS

4224874/B 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/B 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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