# Infineon® LITIX™ Power

## 700mA High Integration - DC/DC Step-Down Converter

TLD5045EJ

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# Infineon® LITIX™ Power

700mA High Integration - DC/DC Step-Down Converter

## Data Sheet

Revision 1.0
2015-05-28

Automotive Power

# Table of Contents

# 1        Overview

- Constant Current Generation
- Wide Input Voltage Range from 5V to 40V
- Peak Current Regulation
- Very low current consumption (<2uA) in Sleep Mode
- Integrated power transistor with low saturation voltage
- Integrated fast freewheeling diode
- Integrated load current sense resistor
- Integrated status pull down transistor
- Overtemperature Protection
- Switching frequency (typ. 200kHz) adjustable via external RC network
- External PWM Dimming Input
- Integrated PWM Dimming Engine
- Analog Dimming (output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during overtemperature conditions)
- Stable switching frequency due to fix OFF-time concept with VREC (supply voltage) feedforward
- Under- and Overvoltage shutdown with hysteresis
- Small thermally enhanced exposed heatslug SMD package
- Automotive AEC Qualified
- Green Product (RoHS) Compliant
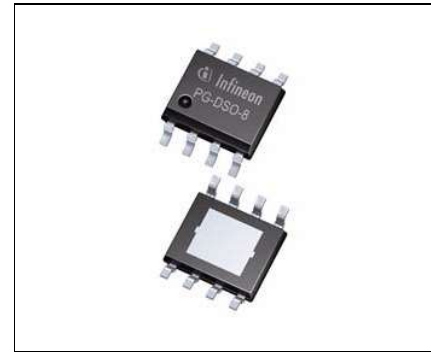
**PG-DSO-8 EP**

## Description

The TLD5045EJ is a highly integrated smart LED buck controller with built in protection functions. The main function of this device is to drive single or multiple series connected LEDs efficiently from a voltage source higher than the LED forward voltage by regulating a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and long LED lifetime. The built in freewheeling diode and switching transistor with current sense requires less external components and saves system costs. High flexibility is achieved by placing low power resistors to adjust output currents up to 700mA and the regulator switching frequency (typ. 200kHz). An integrated PWM dimming engine provides a LED dimming function by placing a simple RC network to GND. This feature is dedicated for decentralized light modules without micro controller involvement. In addition to that an integrated status pull down transistor can be used to simulate a minimum current flow for decentralized modules to avoid a wrong open load detection by a highside switch located in the body control module (BCM).

## Application

- Automotive LED driven Exterior Lighting: Brake, Tail, CHMSL, Daytime Running Light, Position Light
- Automotive LED driven Interior Lighting: Reading Light, Dome Light, Display Backlighting

| Type | Package | Marking |
|------|---------|---------|
| Device1 | PG-DSO-8 EP | PG-DSO-8 EP |

# 2    Block Diagram

The TLD5045 regulates the LED current by monitoring the load current (Peak Current Measurement) through the internal switch cycle by cycle. When the current through the switch reaches the threshold $I_{peak}$ the switch is shut-OFF and it is kept OFF for a time equal to $t_{OFF}$. Both $I_{peak}$ and $t_{OFF}$ can be fixed through few external components.

The peak current $I_{peak}$ is fixed by a resistor connected to the SET pin while the $t_{OFF}$ is fixed by RC network. As $t_{OFF}$ is fixed and the duty cycle depends on $V_{REC}$, the frequency depends on $V_{REC}$ as well. Refer to **Chapter 8.2** for the evaluation of the switching frequency.
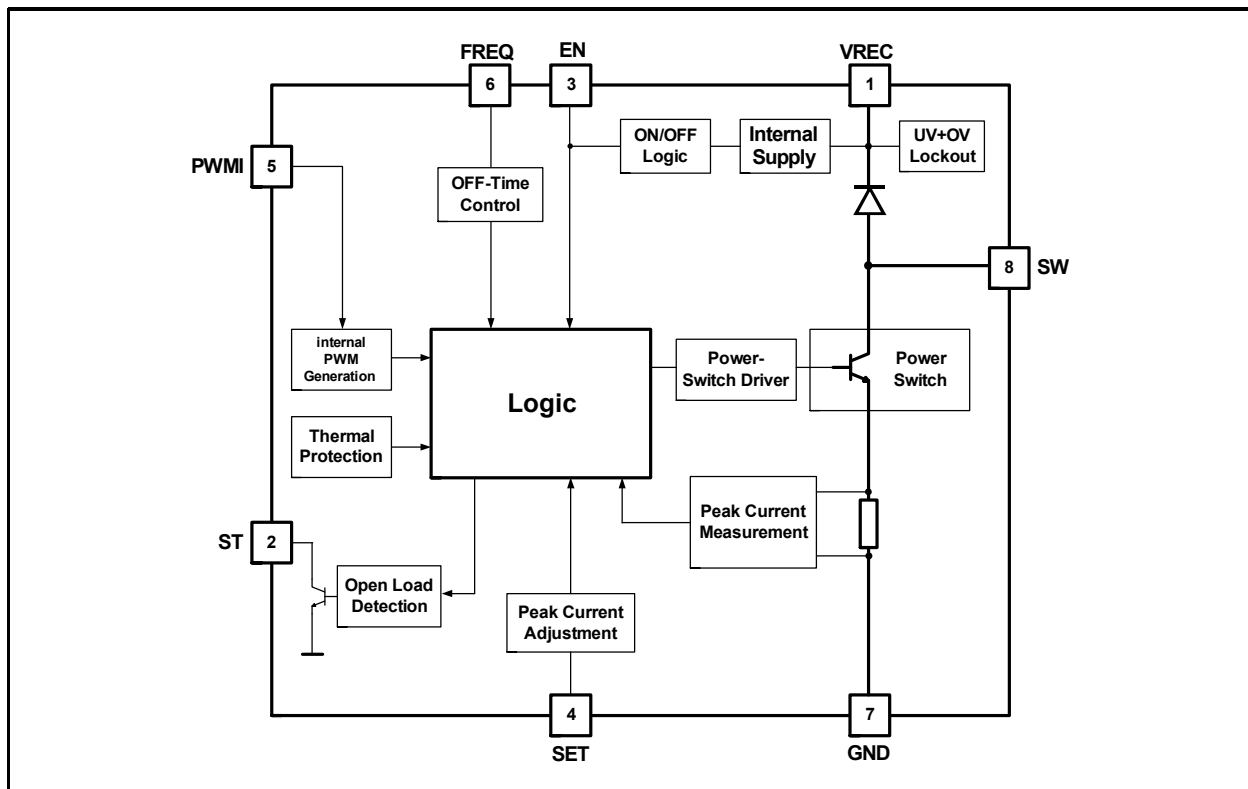


**Figure 2-1    Block Diagram TLD5045EJ**

# 3 Pin Configuration

## 3.1 Pin Assignment
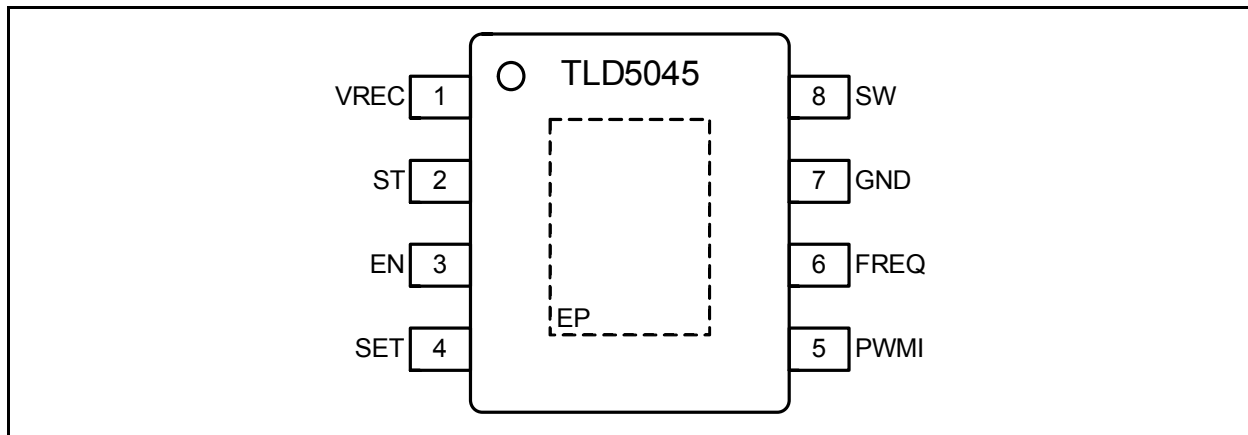


**Figure 3-1    Pin Configuration TLD5045EJ**

## 3.2 Pin Definitions and Functions

**Table 3-1    sec_bias_prereg pin definition and function**

| # | Name | Direction | Type | Function |
|---|------|-----------|------|----------|
| 1 | VREC | | | **Voltage Recirculation Output and Internal Supply Input;**<br>This pin is the supply pin of the IC (see block diagram). Furthermore the cathode of the integrated fast free-wheeling diode is connected to this pin as well. |
| 2 | ST | | | **Status Output;**<br>Open collector diagnostic output to indicate an open load failure.<br>Refer to **Chapter 7** for more details. |
| 3 | EN | | | **Enable;**<br>Apply logic HIGH signal to enable the device |
| 4 | SET | | | **SET Input;**<br>Connect a low power resistor to adjust the output current. |

**Table 3-1    sec_bias_prereg pin definition and function** (continued)

| # | Name | Direction | Type | Function |
|---|------|-----------|------|----------|
| 5 | PWMI | | | **PWM Input;**<br>PWM signal for dimming LEDs. Connect external R and C combination to achieve an auto PWM-dimming function with defined frequency and duty cycle.<br>1) internal PWM dimming function (external RC connected to GND)<br>2) external PWM dimming function (µC is controlling this pin)<br>Refer to **Chapter 6** for more details. |
| 6 | FREQ | | | **FREQuency Select Input;**<br>Connect external Resistor and Capacitor to GND to set the OFF-time of the switching frequency. |
| 7 | GND | | | **Ground;**<br>Connect to system ground. |
|   | SW | | | **Integrated Power-Switch Output;**<br>Collector of the integrated NPN-power transistor. |
|   | EP | | | **Exposed Pad;**<br>Connect to external heatspreading copper area with electrically GND (e.g. inner GND layer of the PCB via thermal vias) |

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

Tj = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

**Table 4-1 Absolute Maximum Ratings[1]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| VREC (Pin 1) Recirculation and Supply Input | $V_{REC}$ | -0.3 | | 45 | V | | P_4.1.1 |
| VREC (Pin 1) Maximum current flowing continuously through the freewheeling diode and the power switch | $V_{FW,SW}$ | | | 1.2 | A | – Maximum ambient temperature must be calculated with given Rthja of the application | P_4.1.2 |
| ST (Pin 2) Diagnostic Status Output Voltage | $V_{ST}$ | -0.3 | | 45 | V | | P_4.1.3 |
| ST (Pin 2) Diagnostic Status Current | $I_{ST}$ | | | 150 | mA | –no short circuit protection and no current limitation implemented | P_4.1.4 |
| EN (Pin 3) Enable Input Voltage | $V_{EN}$ | -0.3 | | 45 | V | | P_4.1.5 |
| SET (Pin 4) Peak Current Adjust Input Voltage | $V_{SET}$ | -0.3 | | 6 | V | | P_4.1.6 |
| PWMI (Pin 5) PWM Input Voltage | $V_{PWMI}$ | -0.3 | | 6 | V | | P_4.1.7 |
| FREQ (Pin 6) OFF-time Adjustment Input | $V_{FREQ}$ | -0.3 | | 6 | V | | P_4.1.8 |
| SW (Pin 8) Switch Output | $V_{SW}$ | -0.3 | | 45 | V | | P_4.1.9 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_j$ | -40 | | 150 | °C | | P_4.1.10 |
| Storage Temperature | $T_{SW}$ | -55 | | 150 | °C | | P_4.1.11 |

**General Product Characteristics**

**Table 4-1    Absolute Maximum Ratings[1]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **ESD Susceptibility** | | | | | | | |
| ESD Resistivity all Pins to GND | $V_{ESD, HBM}$ | -2 | | 2 | kV | HBM[2] ESD Results available? | P_4.1.12 |
| ESD Resistivity to GND | $V_{ESD}$ | -500 | | 500 | V | CDM[3] | P_4.1.13 |
| ESD Resistivity corner pins to GND | $V_{ESD}$ | -750 | | 750 | V | CDM | P_4.1.14 |

1) Not subject to production test, specified by design.
2) ESD susceptibility HBM according to EIA/JESD 22-A 114B
3) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

*Note:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2    Functional Range

**Table 4-2    Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Extended Supply Voltage | $V_{REC}$ | 5 | | 40[1] | V | Parameter deviations possible | P_4.2.1 |
| Nominal Supply Voltage Range | $V_{FW,SWREC}$ | 8 | | 36 | V | | P_4.2.2 |
| External Inductor | $L_{SW}$ | 220 | | 560 | µH | max.560µH to avoid OL | P_4.2.3 |
| Output current range | $I_{OUT}$ | 100 | | 700 | mA | | P_4.2.4 |
| Switching Frequency | $f_{SW}$ | 50 | | 300 | kHz | $T_j$ = 25°C to 150°C | P_4.2.5 |
| Junction Temperature | $T_j$ | -40 | | 150 | °C | | P_4.2.6 |

1) Not subject to production test, specified by design

*Note:  Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards.
For more information, go to www.jedec.org.*

**Table 4-3    Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Junction to Case | $R_{\text{thJ-case}}$ | | 10 | | K/W | 1)2) | P_4.3.1 |
| Junction to Ambient (2s2p) | $R_{\text{thJA}}$ | | 40 | | K/W | 1)3) | P_4.3.2 |

1) Not subject to production test, specified by design.

2) Specified $R_{\text{thJ-case}}$ value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature). Ta=25°C, Power Switch and freewheeling diode are dissipating 1W.

3) Specified RthJA value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). According to JESD51-5 a thermal via array under the exposed pad contacted the first inner copper layer. Ta=25°C, Power Switch and freewheeling diode are dissipating 1W.

# 5 Electrical Characteristics

Tj = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

## 5.1 General Parameters

**Table 5-1 Electrical Characteristics**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Voltage Drop over Power Transistor | $V_{Drop,100}$ | – | 0.8 | – | V | Ipeak=100mA | P_5.1.1 |
| Voltage Drop over Power Transistor | $V_{Drop,700}$ | – | 1.4 | – | V | Ipeak=700mA | P_5.1.2 |
| Freewheeling diode forward voltage | $V_{fw,100}$ | – | 0.8 | – | V | Ipeak=100mA | P_5.1.3 |
| Freewheeling diode forward voltage | $V_{fw,70}0$ | – | 1.4 | – | V | Ipeak=700mA | P_5.1.4 |
| Peak over current limit | $I_{peak\_lim}$ | – | 1.4 | – | A | | P_5.1.5 |
| Peak current accuracy | $I_{peak\_acc}$ | 450 | 500 | 550 | mA | VREC = 12V VEN = 5V VLED = 7.2V RSET = 14kΩ LSW = 220µH fSW = 200kHz | P_5.1.6 |
| Input under voltage shutdown threshold | $V_{REC,UVOFF}$ | – | – | 5 | V | VEN = 5V VREC decreasing; see **Figure 5-1** | P_5.1.7 |
| Input voltage startup threshold | $V_{REC,UVON}$ | – | – | 6 | V | VEN = 5V VREC increasing; see **Figure 5-1** | P_5.1.8 |
| Input under voltage shutdown hysteresis | $V_{REC,UVhyst}$ | – | 1 | – | V | | P_5.1.9 |
| Input over voltage shutdown threshold | $V_{REC,OVOFF}$ | 40.5 | – | – | V | VEN = 5V VREC increasing; see **Figure 5-1** | P_5.1.10 |
| Input over voltage startup threshold | $V_{REC,OV}$ | 40 | – | – | V | VEN = 5V VREC decreasing; see **Figure 5-1** | P_5.1.11 |
| Input over voltage shutdown hysteresis | $V_{REC,OVhyst}$ | – | 0.5 | – | V | | P_5.1.12 |
| Switch ON delay | $t_{dON}$ | – | 400 | 600 | ns | [1]– | P_5.1.13 |
| Switch OFF delay | $t_{dOFF}$ | – | 500 | 850 | ns | [1]– | P_5.1.14 |

**Table 5-1    Electrical Characteristics**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Reference Voltage at SET pin | $V_{SET}$ | 1.16 | 1.225 | 1.29 | V | | P_5.1.15 |
| Pull up current for FREQ pin | $I_{FREQ}$ | 5 | – | – | mA | VFREQ=0V | P_5.1.16 |
| Oscillator switch off threshold | $V_{FREQ,HIGH}$ | – | 3.2 | – | V | | P_5.1.17 |
| Oscillator switch on threshold | $V_{FREQ,LOW}$ | – | 1.2 | – | V | | P_5.1.18 |

1) The minimum switching ON time tON must be greater than tdON + tdOFF

## 5.2    Power Supply Monitoring

**Over- and Undervoltage Shutdown**

If the supply voltage $V_{REC}$ drops below the input under voltagae threshold voltage $V_{REC,UVOFF}$, the power stage is switched OFF and the device is in normal consumption mode ($I_{q,ON}$).

If $V_{REC}$ rises again and reaches the input undervoltage startup threshold $V_{REC,UVON}$ the power stage is restarted and the device is back to normal operation mode.

Same behaviour applies to overvoltage.

The internal status transistor switches off during an overvoltage or undervoltage event on $V_{REC}$.

A detailed description of the under and overvoltage behaviour is displayed in **Figure 5-1** below.
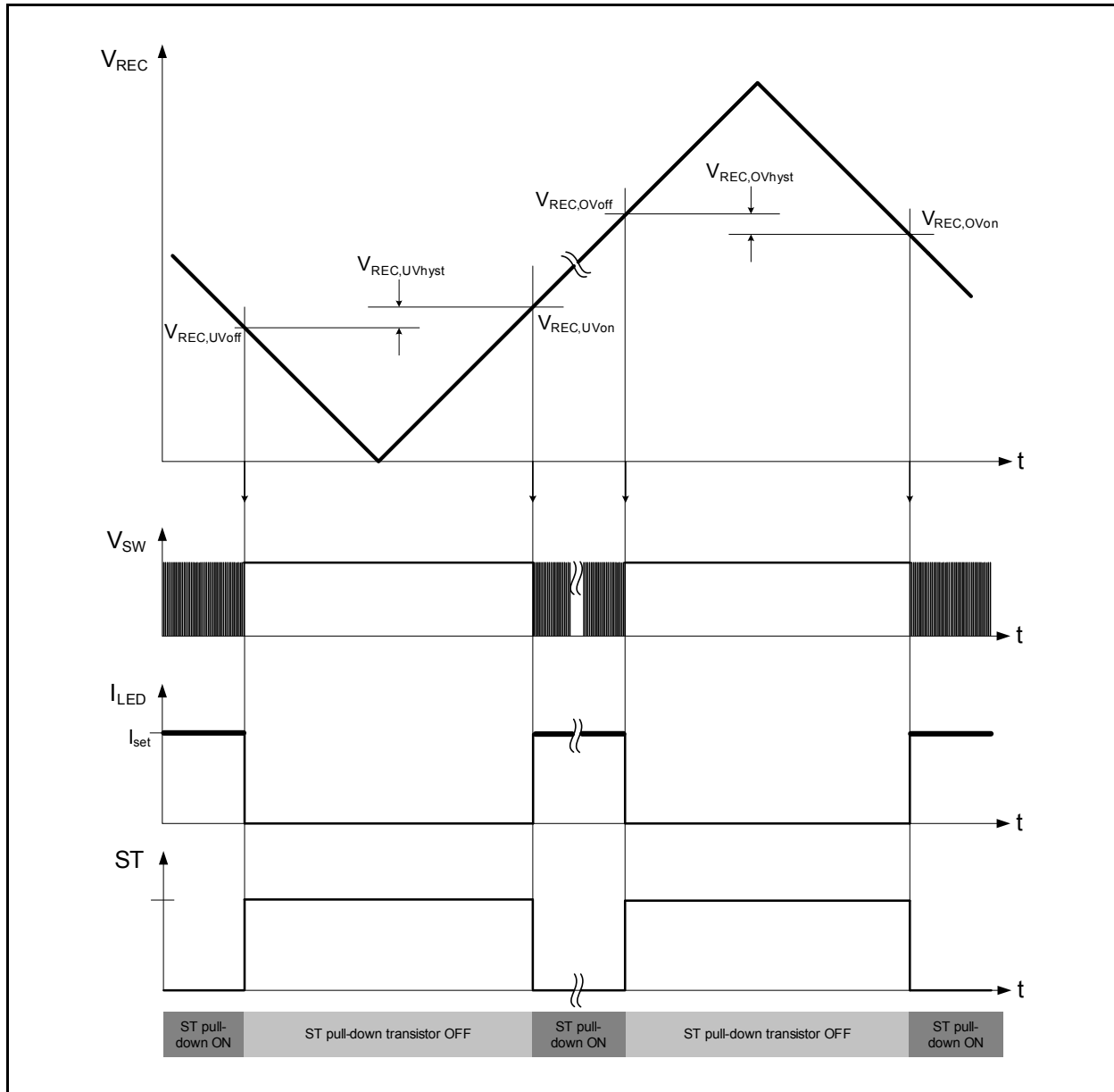
**Figure 5-1    Over- and Undervoltage Protection**

# 6    Enable, Dimming Function and Thermal Protection

## 6.1    Description

**Enable Function**

A logic high signal on the EN pin turns the device on. A logic low signal on enable pin EN brings the device in sleep mode. The current consumption is typ. 0.1 µA in this case. The EN pin has an internal pull down resistor which ensures that the IC is in sleep mode and the power stage is switched off in case the pin EN is externally not connected.

**Dimming Function**

The PWMI pin combines two functions:

1. PWM dimmming via a µC (3.3V and 5V µC)

2. Integrated PWM dimming engine for standalone solutions in decentralized light module (frequency and duty cycle adjustable via external R,C network)

A detailed description of the PWMI pin is displayed in below.
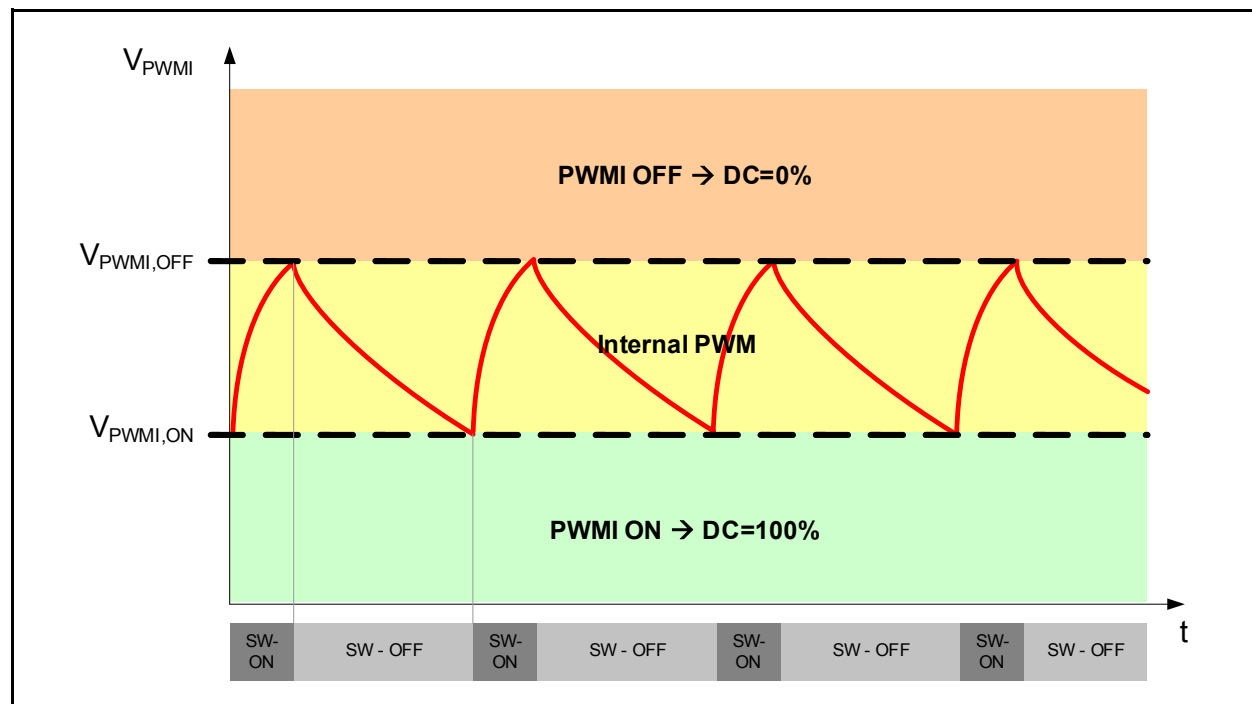


**Figure 6-1    PWMI Pin Description**

## 6.2 Electrical Characteristics Enable, Bias, Dimming Function and Thermal Protection

$V_{REC}$ = 4.5 V to 18 V, Tj = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

**Table 6-1    Electrical Characteristics: Enable, Bias, Dimming Function and Thermal Protection**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Current Consumption, sleep mode | $I_{q,OFF}$ | – | 0.1 | 2 | µA | $V_{EN}$ = 0V; $V_{REC}$ = 16V | P_6.2.1 |
| Current Consumption, active mode (Open Load) | $I_{q,ON}$ | – | – | 5 | mA | $V_{EN}$ = 5.0V; $I_{peak}$ = 0mA (open load); $V_{REC}$ = 16V | P_6.2.2 |
| Current Consumption, active mode | $I_{q,ON}$ | – | – | 10 | mA | $V_{EN}$ = 5.0V; $I_{peak}$ = 700mA $V_{REC}$ = 16V | P_6.2.3 |
| EN Turn On Threshold | $V_{EN,ON}$ | 2.8 | – | – | V | – | P_6.2.4 |
| EN Turn Off Threshold | $V_{EN,OFF}$ | – | – | 0.8 | V | | P_6.2.5 |
| EN high input current | $I_{EN,hi}$ | – | 100 | – | µA | $V_{EN}$ = 5V | P_6.2.6 |
| EN low input current | $I_{EN,lo}$ | 0 | – | 20 | µA | $V_{EN}$ = 0.5V | P_6.2.7 |
| PWMI Turn On Threshold | $V_{PWMI,ON}$ | – | 1 | – | V | see **Figure 6-1** | P_6.2.8 |
| PWMI Turn Off Threshold | $V_{PWMI,OFF}$ | – | 2 | – | V | see **Figure 6-1** | P_6.2.9 |
| PWMI source current | $I_{PWMI}$ | – | 250 | – | µA | $R_{set}$ = 10kΩ $V_{PWMI}$ = 0.5V; | P_6.2.10 |
| Over temperature shutdown | $T_{j,sd}$ | 150 | 175 | – | °C | [1] | P_6.2.11 |
| Over temperature shutdown hysteresis | $T_{j,sd\_hyst}$ | – | 15 | – | K | [1] | P_6.2.12 |

1)  Specified by design. Not subject to production test.

### 6.2.1 PWM Dimming with µC connected to TLD5045EJ PWMI pin

The PWMI pin can be used for PWM dimming. It is a commonly practiced dimming method to prevent color shift in LED light applications.
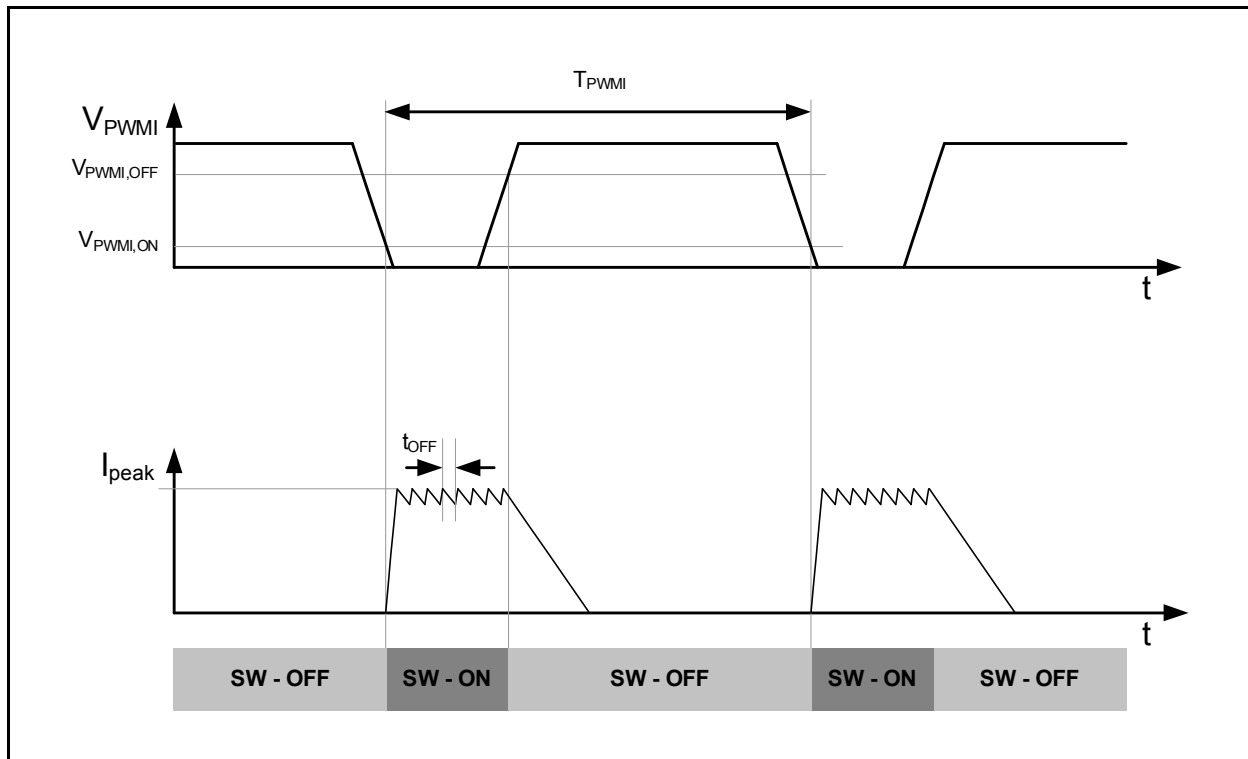


**Figure 6-2    Timing Diagram for LED Dimming with µC**

### 6.2.2 Internal PWM dimming Function

The TLD5045EJ has an integrated PWM dimming engine. Via an external $R_{PWM}$ and $C_{PWM}$ network it is possible to achieve a PWM LED current waveform. The duty cycle and dimming frequency is depending on the size of the external components (see formula in **Figure 6-4**). This feature is specially designed to achieve a stand alone PWM dimming function without the usage of micro controllers or external logic. This allows a flexible and cost effective usage of the device in a decentralized light module application (refer to application drawing ).

The advantage of a PWM dimming (to reduce the LED load current) is the change of light intensity only, at constant light color.

With an external RC network a PWM programming between 100Hz and 1200Hz and Duty Cycles between 4% and max. 20%. is possible. **Figure 6-3** displays the external components corresponding to the desired PWM frequency and duty cycle.

The following setup applies for the table displayed in **Figure 6-3**: $V_{REC}$=12V, $V_{LED}$=7.2V, $L_{SW}$=220µH, $R_{SET}$=14k$\Omega$.

| $R_{PWMI}$ | $C_{PWMI}$ | $f_{PWMI}$ | DC |
|---|---|---|---|
| 216k$\Omega$ | 64nF | 100Hz | 4% |
| 216k$\Omega$ | 32nF | 200Hz | 4% |
| 216k$\Omega$ | 21nF | 300Hz | 4% |
| 216k$\Omega$ | 16nF | 400Hz | 4% |
| 87k$\Omega$ | 150nF | 100Hz | 10% |
| 87k$\Omega$ | 75nF | 200Hz | 10% |
| 87k$\Omega$ | 50nF | 300Hz | 10% |
| 87k$\Omega$ | 37nF | 400Hz | 10% |
| 44k$\Omega$ | 265nF | 100Hz | 20% |
| 44k$\Omega$ | 132nF | 200Hz | 20% |
| 44k$\Omega$ | 88nF | 300Hz | 20% |
| 44k$\Omega$ | 66nF | 400Hz | 20% |

**Figure 6-3** $R_{PWMI}$ and $C_{PWMI}$ versus $f_{PWMI}$ and DC

## 6.3 Overtemperature Protection of the Device

A temperature sensor at the power stage causes the overheated device to switch OFF to prevent destruction. During over temperature condition the internal ST transistor is switched OFF. Due to the autorestart function of the device the status signal will toggle accordingly. The timing of this pattern is dependant on the thermal capability of the application and can be used to distinguish between open load error and overtemperature condition. More details on the overtemperature behavior is displayed in **Figure 6-4** below.
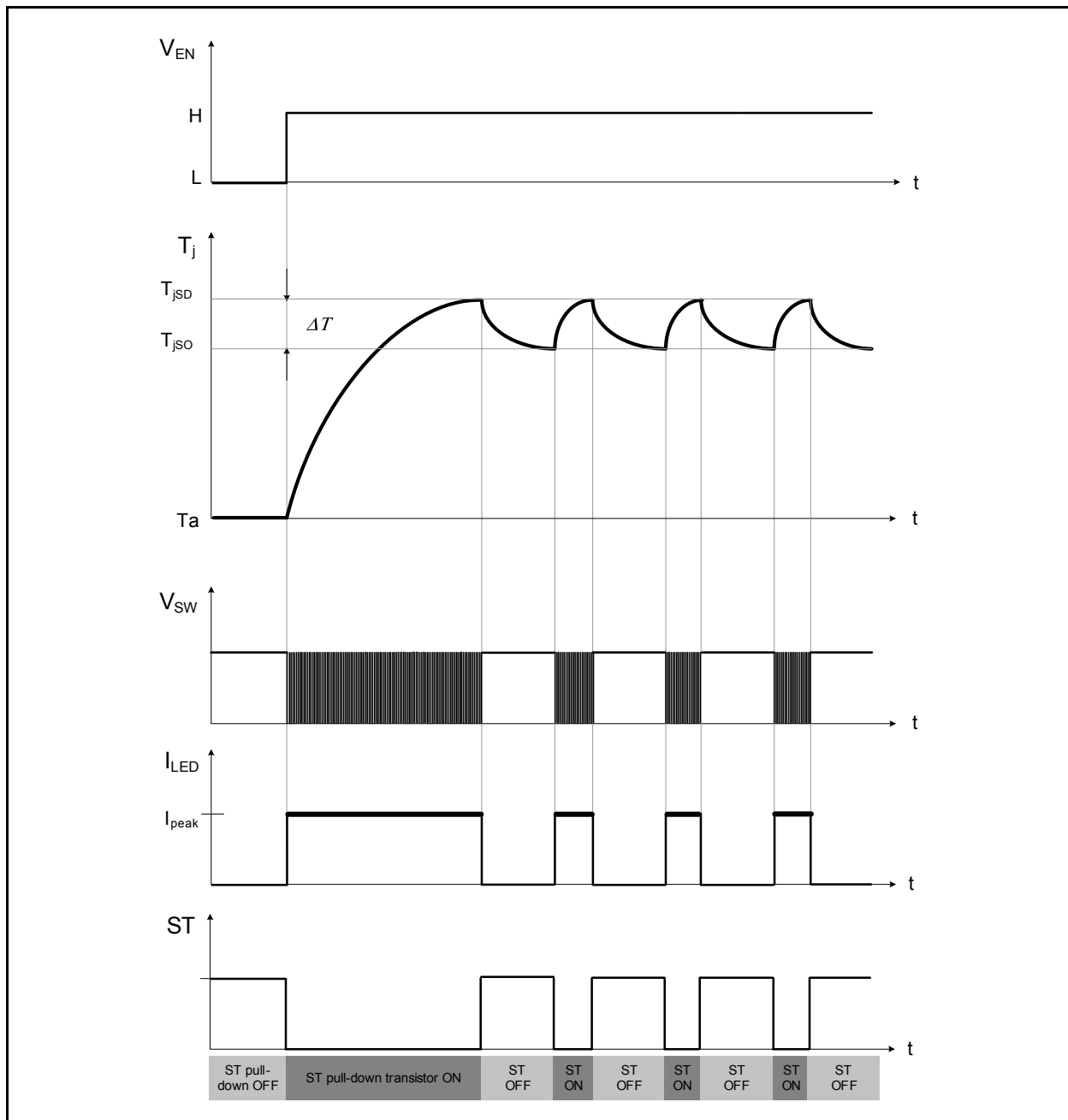


**Figure 6-4     R$_{PWMI}$ and C$_{PWMI}$ versus f$_{PWMI}$ and DC**

# 7 Open Load Diagnosis

## 7.1 Description

The TLD5045EJ has an integrated open load during ON diagnosis. During normal operation the ST pin (open collector output) is pulled to GND (internal transistor is ON). The open load detection is realized by monitoring the switching behavior at the SW pin. During an open load event the integrated power stage at the SW pin will be statically turned ON. If the output stage is turned ON for more than the open load diagnosis delay time ($t_{OL}$) an open load condition is detected. An open load event will switch OFF the internal transistor. If a µC is connected to the ST pin an external pull up resistor should be placed to achieve a logic HIGH level for the proper open load error signalling reporting. For a timing diagram on the functionality of the open load diagnosis please refer to **Figure 7-1** and **Figure 7-2**.

## 7.2 Electrical Characteristics: Open Load Diagnosis

$V_{REC}$ = 4.5 V to 18 V, Tj = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

**Table 7-1    Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Open Load diagnosis DelayTime | $t_{OL}$ | 20 | – | – | µs | | P_7.2.1 |
| Open Load diagnosis current | $I_{OL}$ | – | 50 | – | mA | | P_7.2.2 |
| Voltage Drop over internal ST transistor | $V_{Drop,ST}$ | – | 0.3 | – | V | $I_{ST}$=150mA | P_7.2.3 |

## 7.3    Open Load Diagnosis in different Application Conditions

### 7.3.1    Light module application without µC

Most of the time, the open load diagnosis of the whole light module is done via the current sense of the driver IC (e.g. PROFET) located in the light control module (or BCM module). See **Figure 8-6** for a simplified application schematic. The light module needs to sink a specified minimum current (e.g. 100mA) to indicate normal operation. To guarantee this minimum current also under light load conditions (e.g. high efficiency LED bin at high supply voltages = min. load current required) system designers often have to place resistors in parallel to the application circuit (see Resistors connected to supply lines in **Figure 8-6**). When using such resistors connected between $V_S$ and GND, an open LED diagnosis is not possible anymore. To overcome this issue an internal transistor (open collector) is connected to the ST pin of the TLD5045EJ. During normal operation the ST pin is LOW and a minimum module current can be guaranteed.

As soon as an open load occurs the internal ST transistor switches off. Due to this, the current on the $V_{REC}$ pin decreases below the open load detection threshold of the driver IC located in the light control module.

*Note:    Open Load is only detected during the ON cycle of the switching transistor. During the OFF state the ST signal displays what was detected in the previous ON state.*
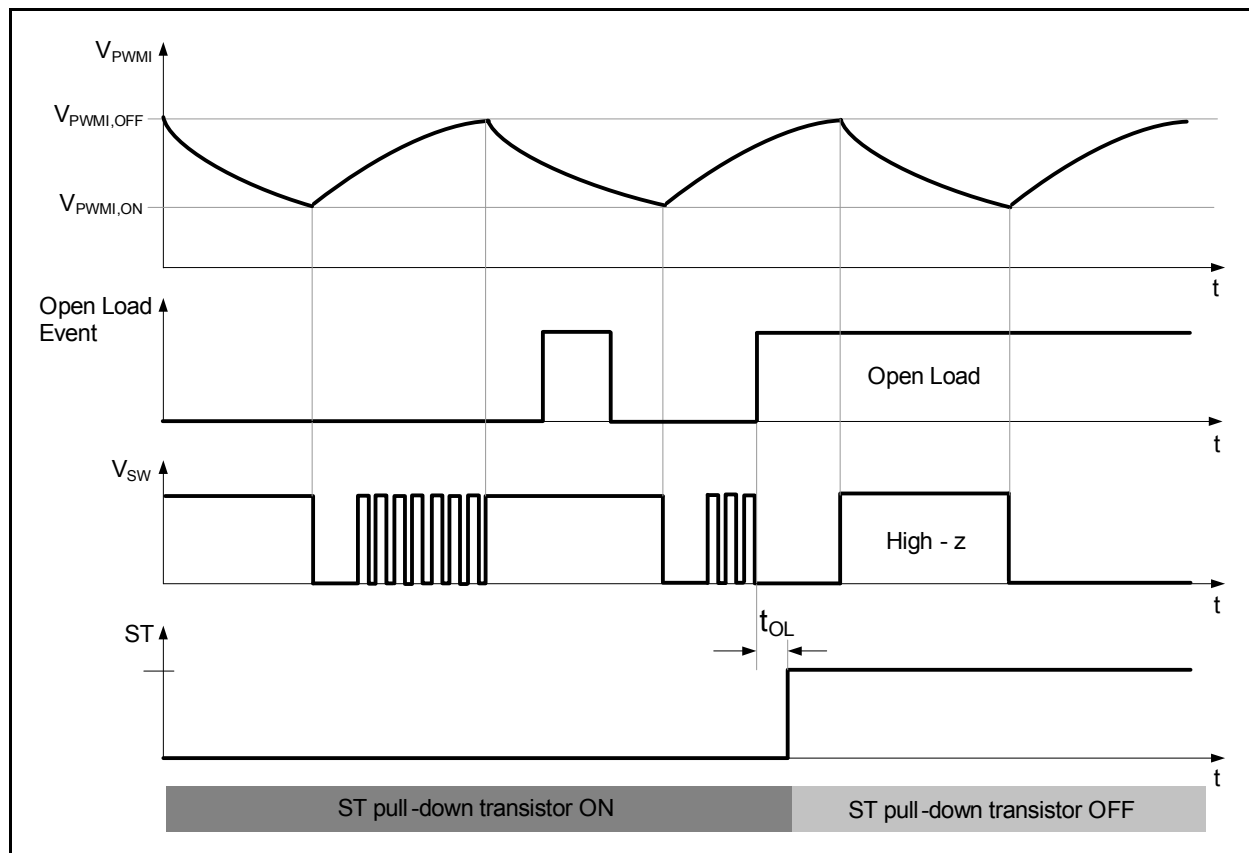


**Figure 7-1    Open Load Diagnosis using Internal PWM Mode**

## 7.4 Application with µC connected to TLD5045EJ IC

The ST pin can be connected directly to a µC input. During an open load condition the ST transistor is OFF. An external pull up resistor connected to $V_{DD}$ is required to signal a logic high signal on the ST pin during an open load error. Please consider that this diagnosis functionality is only active if the device is in active mode (HIGH potential at the EN pin).
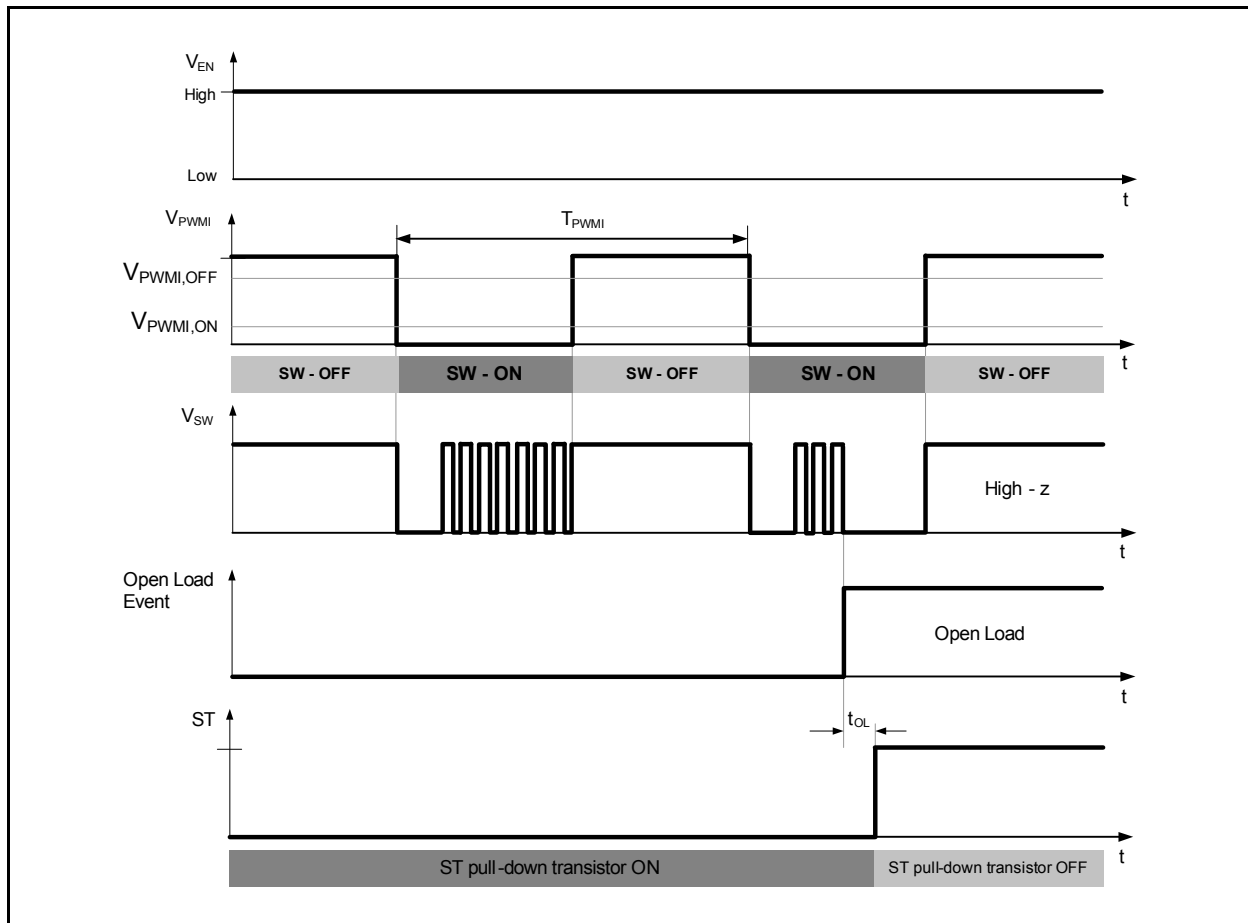
Refer to application drawing **Figure 8-5**.



**Figure 7-2    Open Load diagnosis via µC connected to ST pin**

# 8 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 8.1 Output Peak current Adjustment via R<sub>SET</sub>

The external resistor $R_{SET}$ is used to adjust the peak current of the regulator. Maximum achievable peak current is 700mA and minimum achievable peak current is 100mA. The SET pin provides an internally fixed voltage level at typ.: 1.225V. Out of this considerations the equation is:

(8.1)

$$Ipeak = \left( \frac{1.225 \ V}{R_{SET}} \right) \cdot 5710$$

The factor 5710 is derived from following considerations:

- Ipeak, max = 700mA ($R_{SET}$ = 10kΩ)
- Ipeak,min = 100mA ($R_{SET}$ = 70kΩ)

Internal comparator voltage at SET pin = 1.225V.

The circuitry behind the SET pin is adjusting higher peak currents with lower RSET values.

The $R_{SET}$ value should be in the range from 10kΩ to 70kΩ to achieve the requested peak current range.

The following setup applies for the table displayed in **Figure 8-1**: $V_{REC}$=12V, $V_{LED}$=7.2V, $L_{SW}$=220µH.

| I<sub>PEAK</sub> [mA] | R<sub>SET</sub> [kΩ] |
|:---:|:---:|
| 100 | 70 |
| 200 | 35 |
| 300 | 23 |
| 400 | 18 |
| 500 | 14 |
| 600 | 12 |
| 700 | 10 |
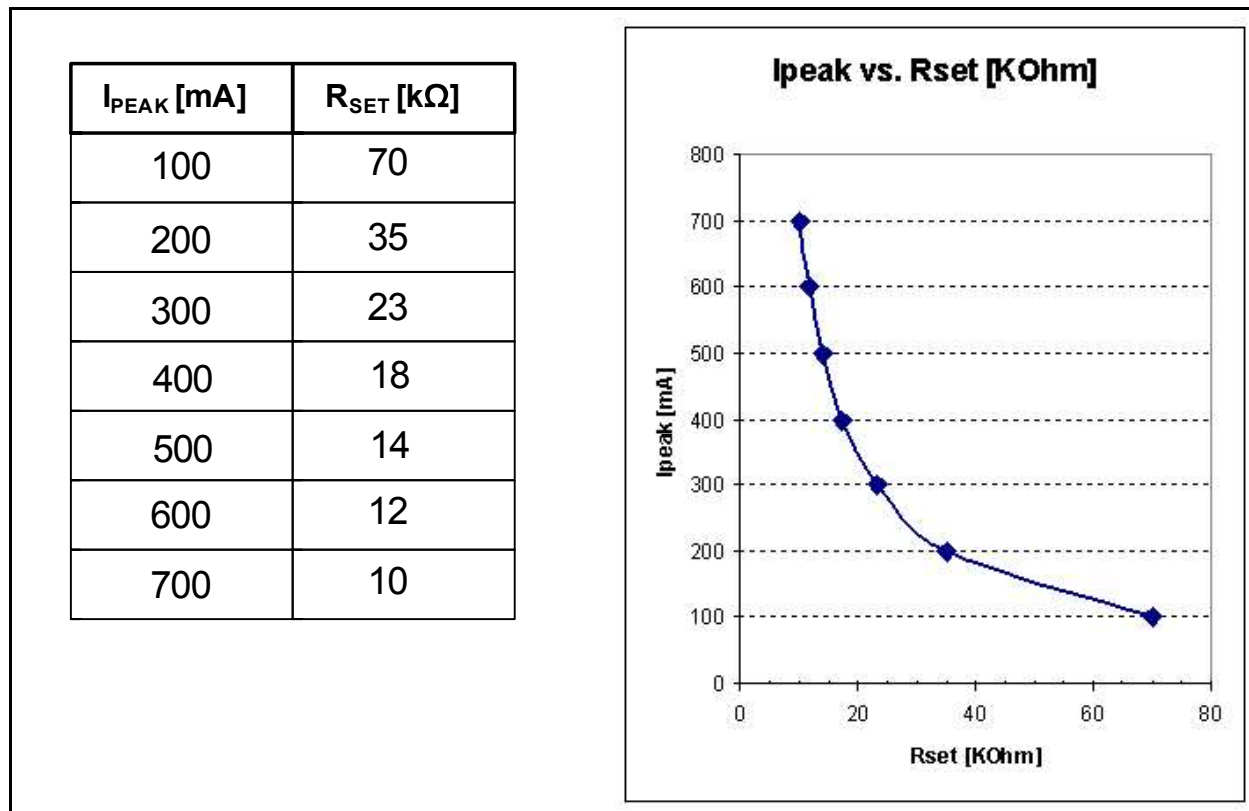


**Figure 8-1    R<sub>SET</sub> Resistor Selection**

## 8.2 Switching Frequency Determination

With the external $R_{FREQ}$, $C_{FREQ}$ and $R_{COMP}$ network, it is possible to adjust the switching frequency of the regulator. To ensure a stable frequency over a broad range of input voltage $V_{REC}$ an external resistor $R_{COMP}$ can be used.

The following setup applies for the table displayed in **Figure 8-3**: $V_{REC}$=12V, $V_{LED}$=7.2V, $L_{SW}$=220µH, $R_{SET}$=14kΩ.
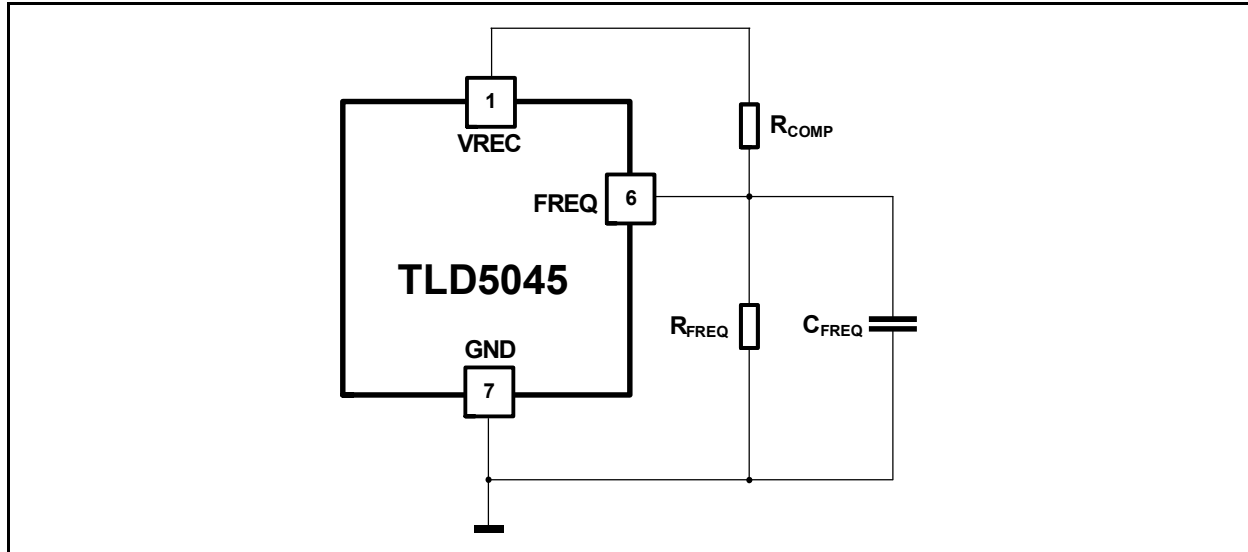


**Figure 8-2** Setting $t_{OFF}$ Time of Regulator with External $R_{FREQ}$, $C_{FREQ}$ Network

| $R_{comp}$ | $R_{freq}$ | $C_{freq}$ | $f_{sw}$ | $t_{off}$ |
|---|---|---|---|---|
| 255.8kΩ | 17.1kΩ | 220pF | 50kHz | 6.47µs |
| 115.8kΩ | 7.7kΩ | 220pF | 100kHz | 3.19µs |
| 69.7kΩ | 4.6kΩ | 220pF | 150kHz | 2.12µs |
| 46.8kΩ | 3.1kΩ | 220pF | 200kHz | 1.59µs |
| 72.8kΩ | 4.9kΩ | 100pF | 250kHz | 1.27µs |
| 52.7kΩ | 3.5kΩ | 100pF | 300kHz | 1.06µs |

**Figure 8-3** $R_{FREQ}$, $C_{FREQ}$ versus $f_{SW}$ Table
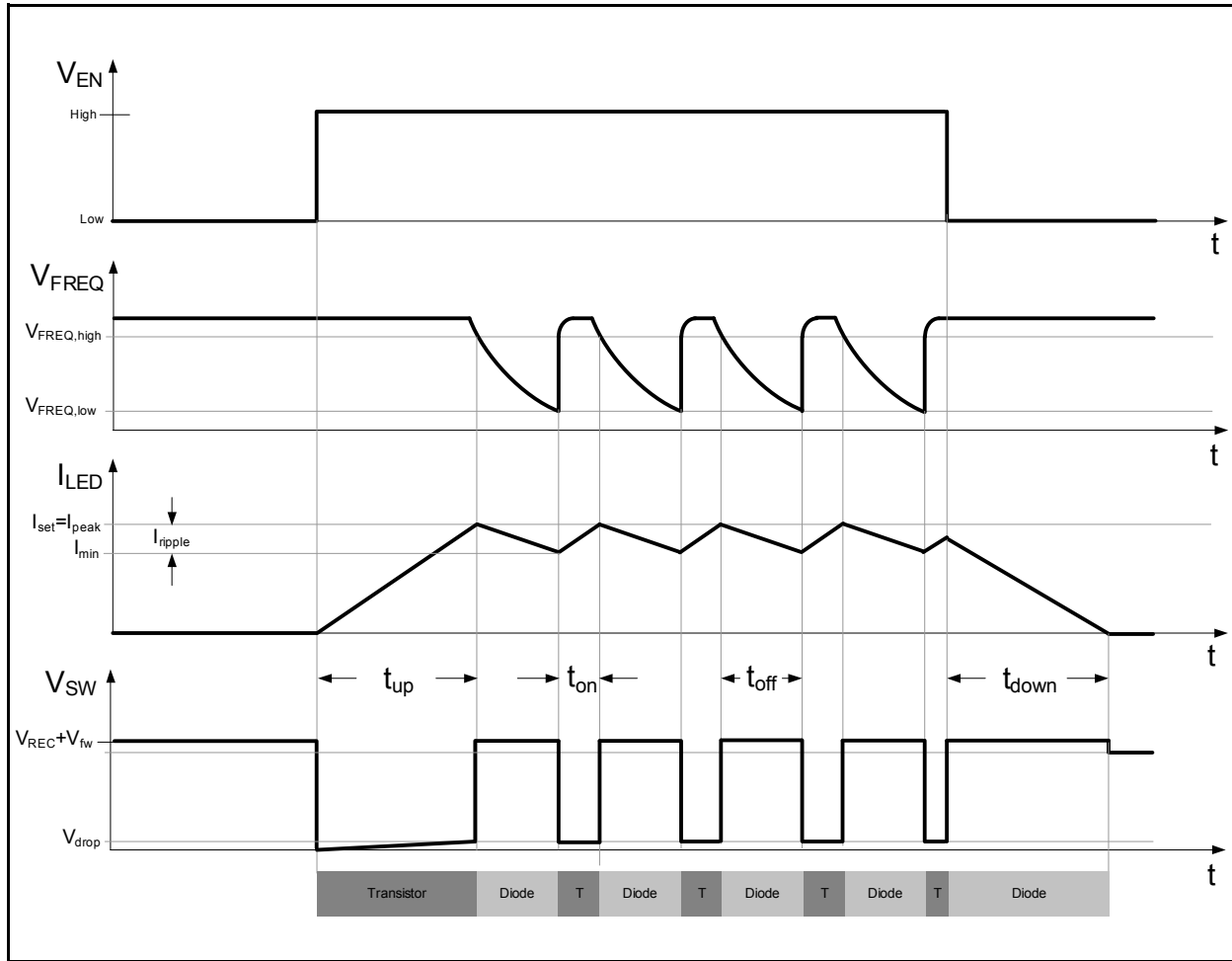
**Figure 8-4    Theoretical Operating Waveforms**

## 8.3 TLD5045EJ in different LED Applications

### 8.3.1 TLD5045EJ in a Body Control Module (BCM) with µC Interface

**Figure 8-5** provides a simplified application with two high brightness LEDs in series. A µC is controlling the EN pin to put the device into sleep/active mode. Also the PWMI pin can be directly controlled via a µC port if PWM dimming of the LED current is required. The open load ST pin monitors the load condition of the application and gives feedback to the µC. An external pull up resistor is recommended to achieve a logic HIGH signal during an open load error (internal status transistor is switched OFF and the ST pin is high ohmic an external pull up resistor ensures a logic HIGH signal).

The external low power resistor $R_{SET}$ is used to set the required peak current for the LED load (refer to **Figure 8-1** for more details).

To set the desired switching frequency of the buck regulator the external $R_{FREQ}$ and $C_{FREQ}$ network must be connected to GND (reference values are given in **Figure 8-3**).
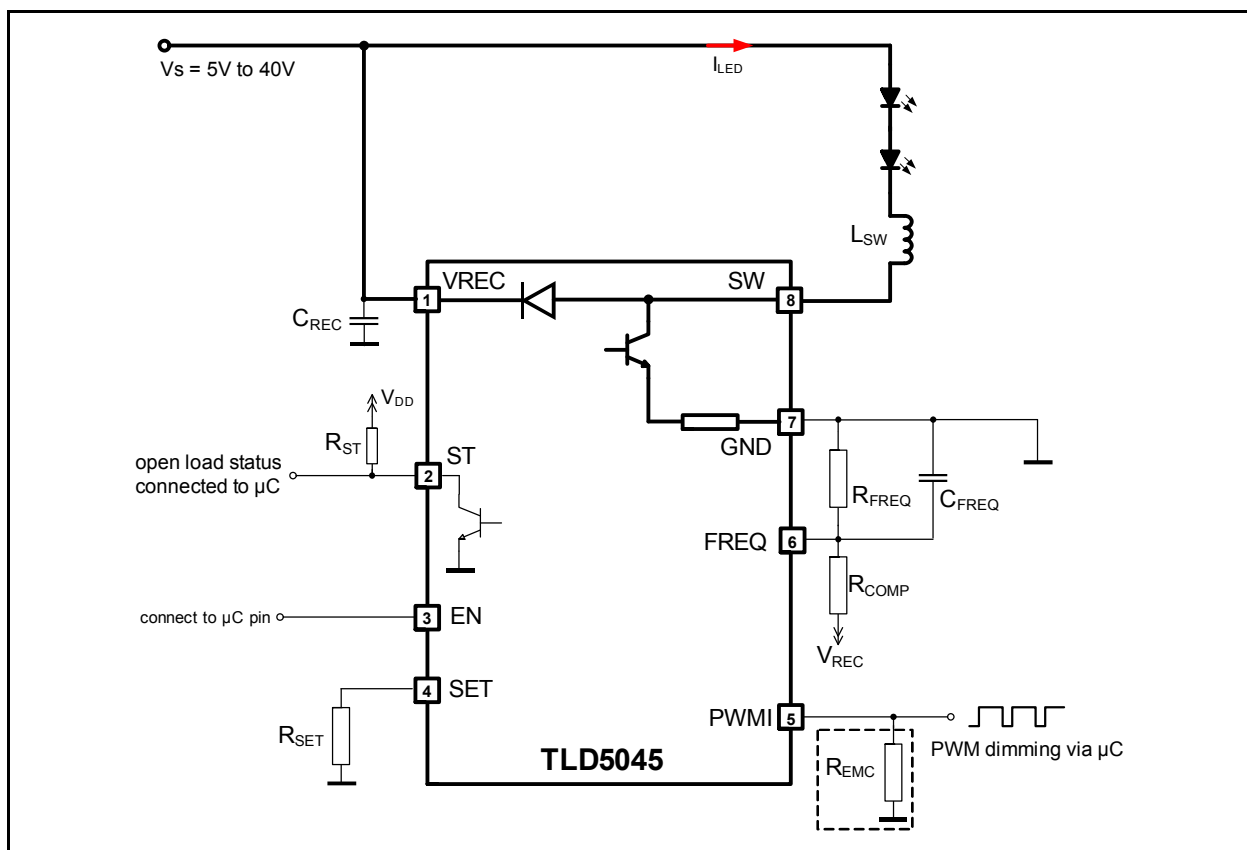


**Figure 8-5    Simplified Application Diagram TLD5045EJ**

*Note:    This is a very simplified example of an application circuit. The function must be verified in the real application*

## 8.3.2 Decentralized Light Module Application - DLM (Input configuration 1)

The connection between the Body Control Module (BCM) and the Decentralized Light Module is realized via one supply line and one GND connection.

The supply line could change between two different operation modes:

1. Light Function 1 - Daytime Running Light (DRL) mode: If the supply line is permanently ON, the DRL application which requires higher LED current (e.g. 400mA) is active. The proper $R_{SET}$ resistor should be placed to achieve the desired load current (e.g 18kΩ).

2. Light Function 2 - Position Light (PL) mode: During a PWM signal (e.g. 200Hz) on the supply line the mean LED current is reduced to a lower level (e.g. 50mA) and the application is entering into PL mode. The enable pin of the TLD5045EJ is a high voltage pin (max. 45V) and can be directly connected via a resistor REN before the reverse polarity protection diode of the module to achieve a fast capture of the PWM signal. The PWMI pin is connected to GND (inverse logic = ON).

To simulate a module current during light load conditions, the ST pin can be connected via a resistor to the supply voltage line. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without micro controller involvement the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction.
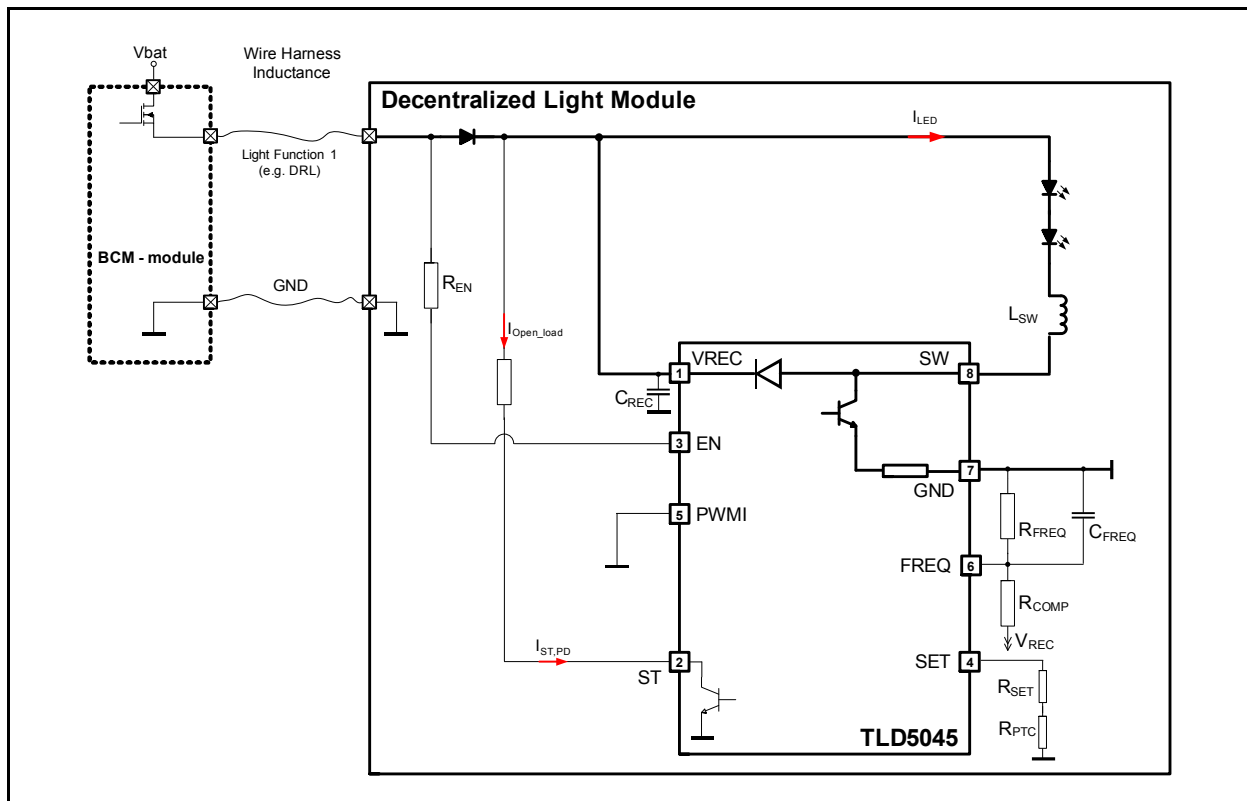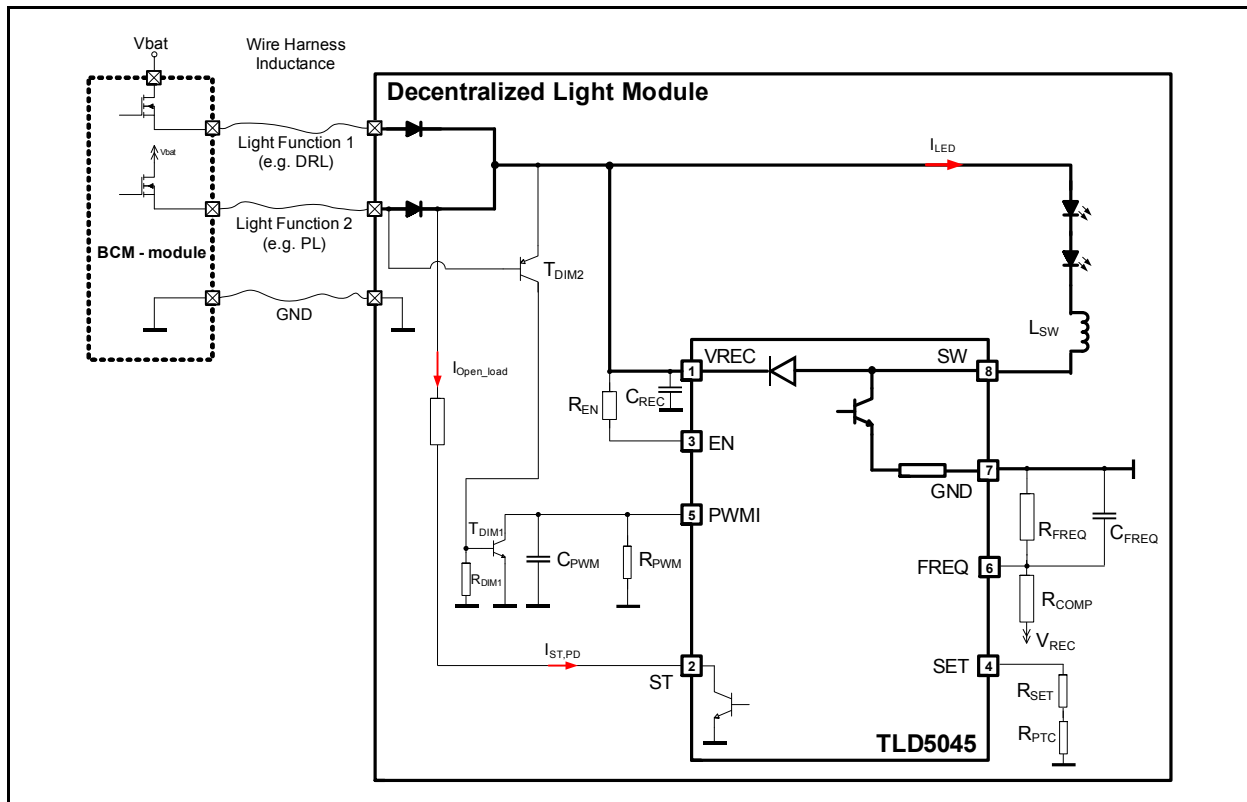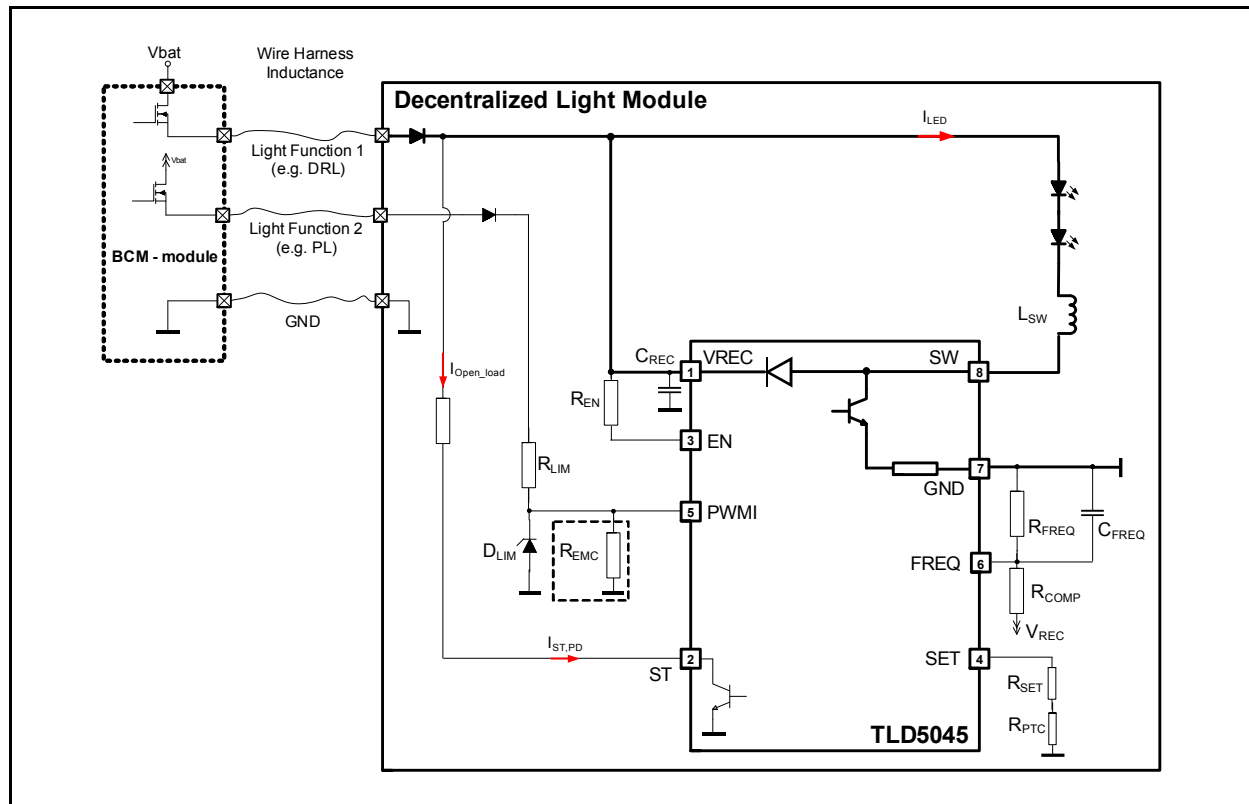


**Figure 8-6    Application Diagram of Decentralized Light Module without µC (input config 1)**

*Note:    This is a very simplified example of an application circuit. The function must be verified in the real application*

### 8.3.3 Decentralized Light Module Application - DLM (Input configuration 2)

In this particular input configuration two supply lines are tied together on the DLM. The following input states must be considered to distinguish between Light Function 1 (DRL mode) and Light Function 2 (PL mode).

1. 1) Condition: DRL = ON, PL = OFF. Desired function: DRL mode (e.g. 400mA LED load current)
2. 2) Condition: DRL = OFF, PL = ON. Desired function: PL mode (e.g. 50mA LED load current)
3. 3) Condition: DRL = ON, PL =ON. Desired function: PL mode (e.g. 50mA LED load current)

To achieve a lower mean LED load current during the PL mode the integrated PWM engine is a useful feature. The external RPWM and CPWM circuit predefines a dedicated PWM frequency and duty cycle. (for details refer to **Figure 8-2**)

To simulate a module current during light load conditions the ST pin can be connected via resistors to both supply voltage lines. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without micro controller involvement the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction.



**Figure 8-7    Application Diagram of Decentralized Light Module without µC (input config 2)**

*Note:    This is a very simplified example of an application circuit. The function must be verified in the real application*

## 8.3.4 Decentralized Light Module Application - DLM (Input configuration 3)

A permanent supply chooses the Light Function 1 (DRL mode) and a second dedicated PWM supply between 100Hz and 200Hz switches to Light Function 2 (PL mode). For this input configuration it is possible to connect the PWM dimming output of the BCM directly to the PWMI input of the TLD5045EJ. To simulate a module current during light load conditions the ST pin can be connected via a resistor to the permanent supply voltage line. (refer to **Chapter 7** for a detailed description of the ST behavior)

For a decentralized solution without micro controller involvement the possibility to connect a PTC resistor at the SET pin is a cost effective solution to protect the LED load from thermal destruction. (for details refer to **Figure 8-6**)



**Figure 8-8    Application Diagram of Decentralized Light Module without µC (input config 3)**

*Note:    This is a very simplified example of an application circuit. The function must be verified in the real application*

# 9 Package Outlines
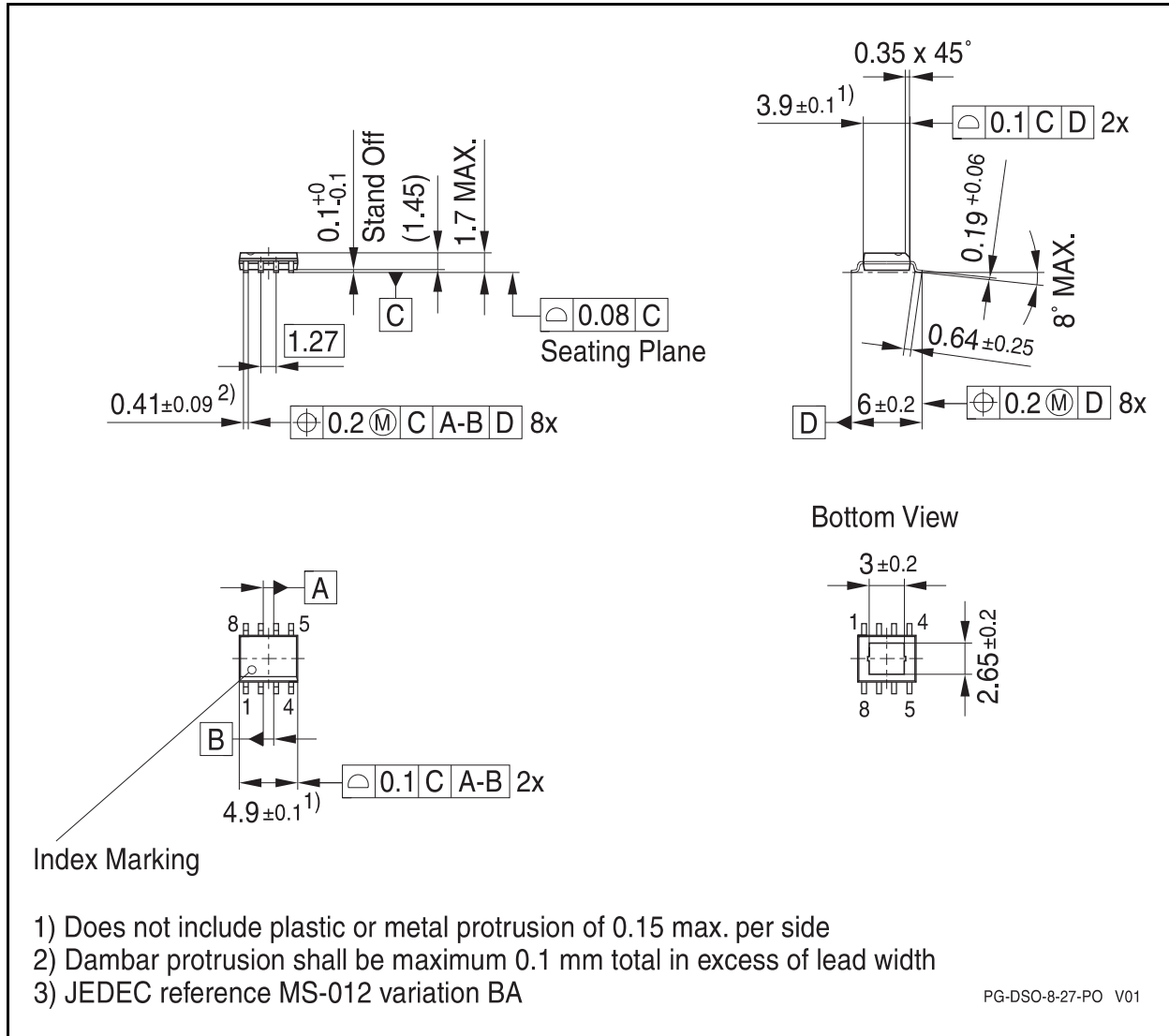


**Figure 9-1    Outline PG-DSO-8 EP**

**Green Product (RoHS Compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

| Revision History | | | |
|---|---|---|---|
| **Revision 1.0, 2015-05-28** | | | |
| **Page or Item** | **Subjects (major changes since previous revision)** | **Responsible** | **Date** |
| Rev1.0 | Initial Data Sheet for TLD5045EJ | | 2011-05-27 |
| | | | |

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