RClamp0524PQ
Low Capacitance RailClamp®
4-Line Surge and ESD Protection

PROTECTION PRODUCTS

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

RClamp0524PQ has a typical capacitance of only 0.3 pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz with no significant signal attenuation. ESD characteristics are highlighted by high ESD withstand voltage (+/-15kV per IEC 61000-4-2) and low dynamic resistance (0.43 Ohms typical). Each device will protect four lines operating at 5 volts

RClamp0524PQ is in a 10-pin SLP2510P8 package and is qualified to AEC-Q100, Grade 1 (-40 to +125 °C) for automotive applications. It measures 2.5 x 1.0 mm with a nominal height of only 0.58 mm. The leads are finished with lead-free NiPdAu. The flow- through package design simplifies PCB layout.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD) 25kV (Air), 15kV (Contact)
  - IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - IEC 61000-4-5 (Lightning) 5A (8/20µs)
  - ISO-10605 (ESD) 20kV (Air), 12kV (Contact)
- Qualified to AEC-Q100, Grade 1
- Protects four High-Speed Data Lines
- Working Voltage: 5V
- Low Capacitance: 0.8 pF Maximum (I/O to GND)
- Dynamic Resistance: 0.43 Ohms (Typ)
- Solid-State Silicon-Avalanche Technology

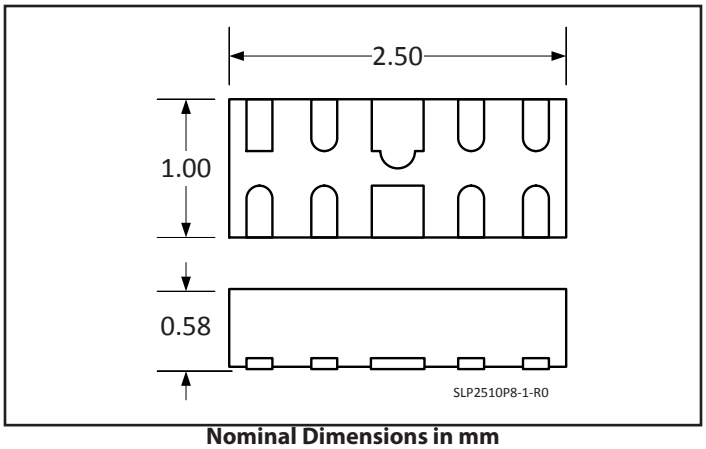
Mechanical Characteristics

- SLP2510P8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.5 x 1.0 x 0.58 mm
- Lead Finish: NiPdAu
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

Applications

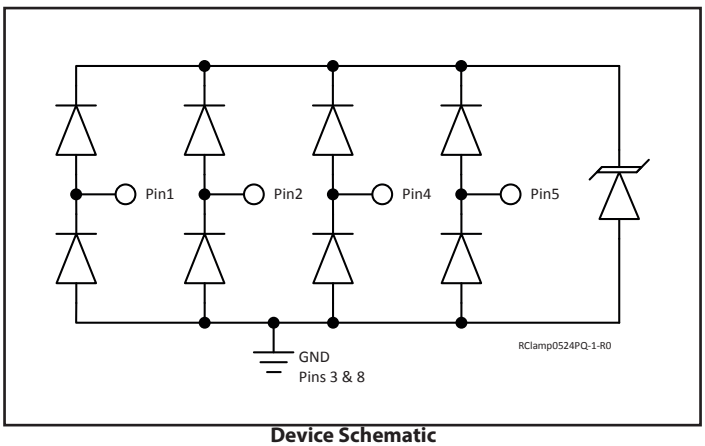
- Automotive Applications
- Industrial Equipment
- HDMI
- Digital Visual Interface
- MDDI Ports
- PCI Express

Nominal Dimension



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	75	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±15 ±25	kV
ESD per ISO-10605 (Contact)(2) ESD per ISO-10605 (Air)(2)	V_{ESD}	±12 ±20	kV
Operating Temperature	T_J	-40 to +125	^oC
Storage Temperature	T_{STG}	-55 to +150	^oC

Electrical Characteristics (T=25^{o}C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40^{o}C to 125^{o}C Any I/O pin to GND				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA, Any I/O pin to GND	-40^{o}C to 125^{o}C	6.5	9	11	V
Reverse Leakage Current	I_R	V_{RWM} = 5V	T = 25^{o}C			0.1	µA
			T = 125^{o}C			0.25	µA
Clamping Voltage(3)	V_C	I_{PP} = 1A, tp = 8/20µs, Any I/O pin to GND				12	V
Clamping Voltage(3)	V_C	I_{PP} = 5A, tp = 8/20µs, Any I/O pin to GND				15	V
ESD Clamping Voltage(4)	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Any I/O pin to GND			12		V
ESD Clamping Voltage(4)	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Any I/O pin to GND			17		V
Dynamic Resistance(4), (5)	R_{DYN}	tp = 0.2/100ns (TLP) Any I/O pin to GND			0.43		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Any I/O pin to GND	T = 25^{o}C		0.4	0.8	pF
			T=125^{o}C		1.2	1.5	
		V_R = 0V, f = 1MHz Between I/O pins	T = 25^{o}C		0.3	0.4	
			T = 125^{o}C		0.5	0.7	

Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP)

(2): ESD Gun return path to Horizontal Coupling Plane (HCP); Test conditions: 330pF, 330Ω.

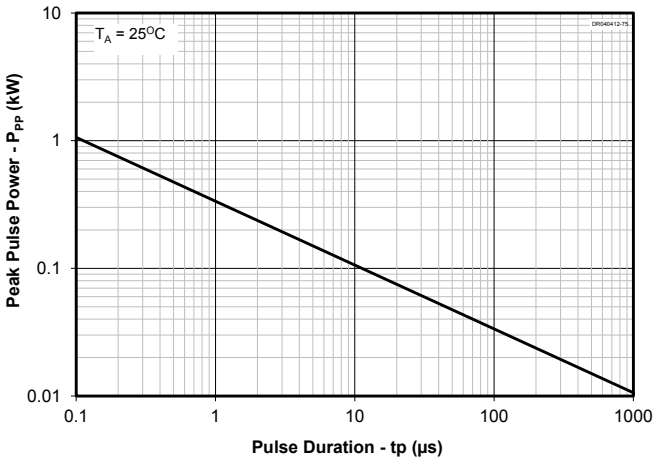
(3): Measured using an 8/20us constant current source.

(4): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

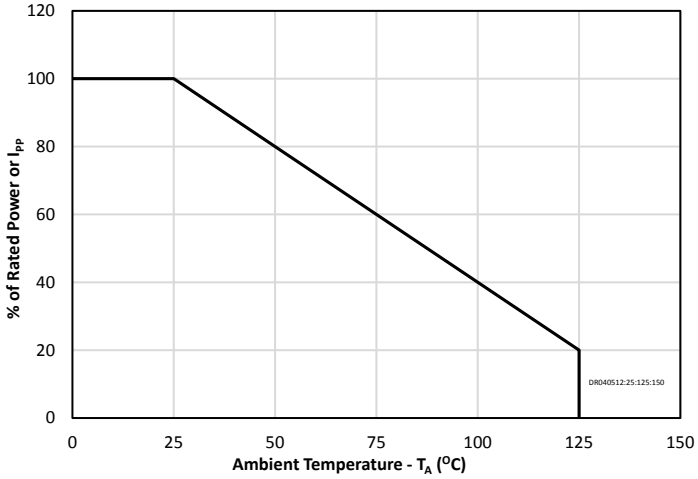
(5): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

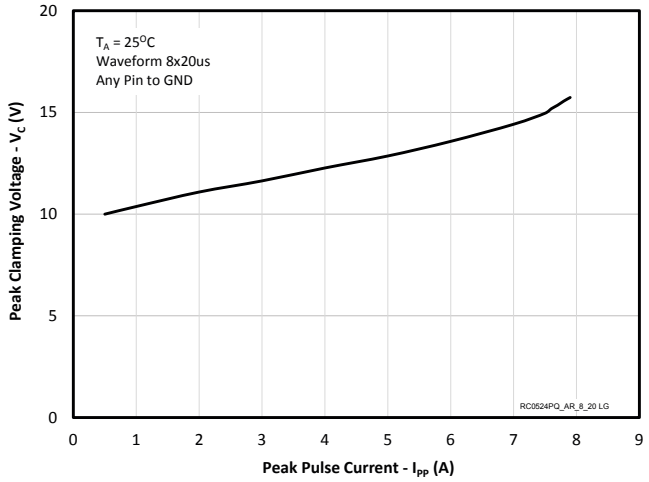
Non-Repetitive Peak Pulse Power vs. Pulse Time



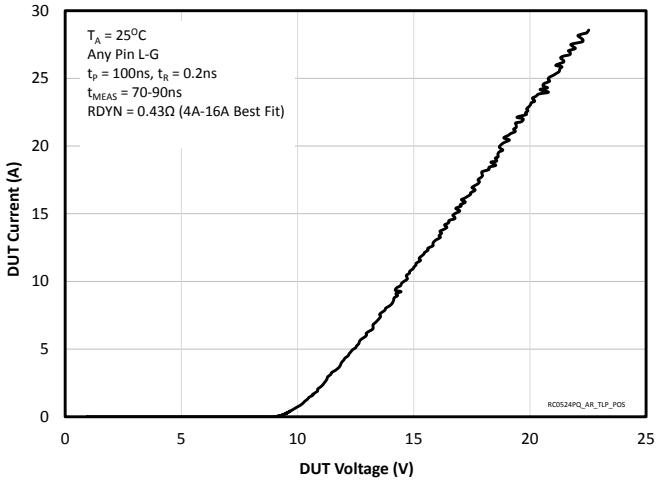
Power Derating Curve



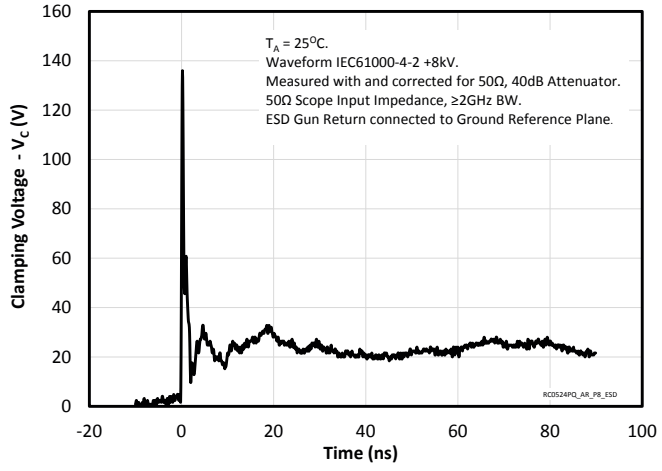
8/20us Surge Clamping Characteristic



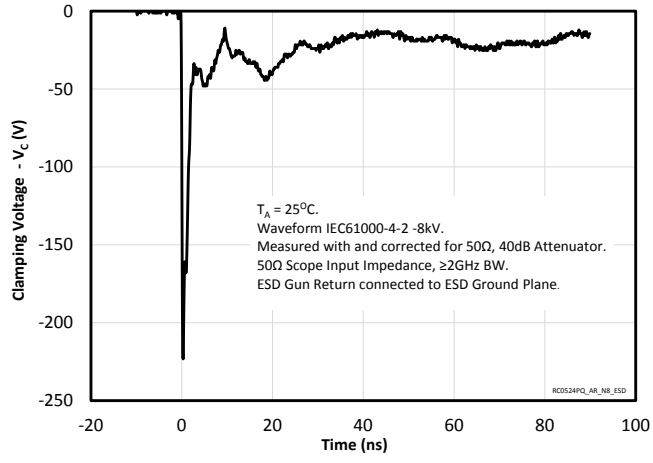
TLP IV Curve (Positive Pulse)



ESD Clamping (+8kV Contact per IEC 61000-4-2)

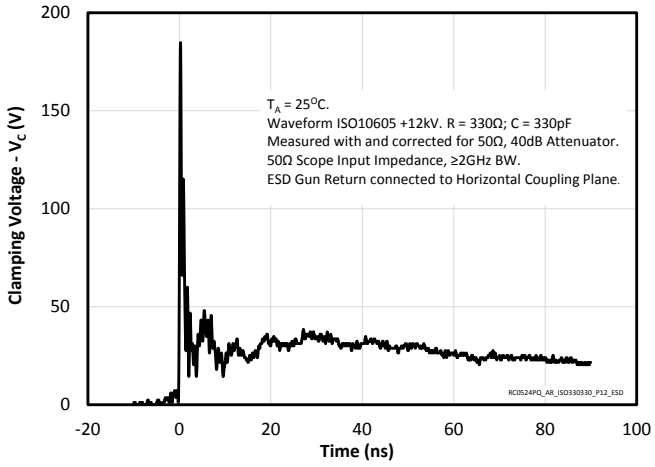


ESD Clamping (-8kV Contact per IEC 61000-4-2)

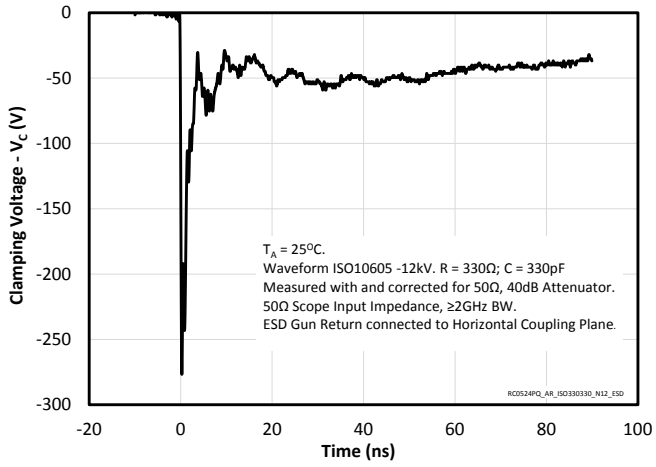


Typical Characteristics (Continued)

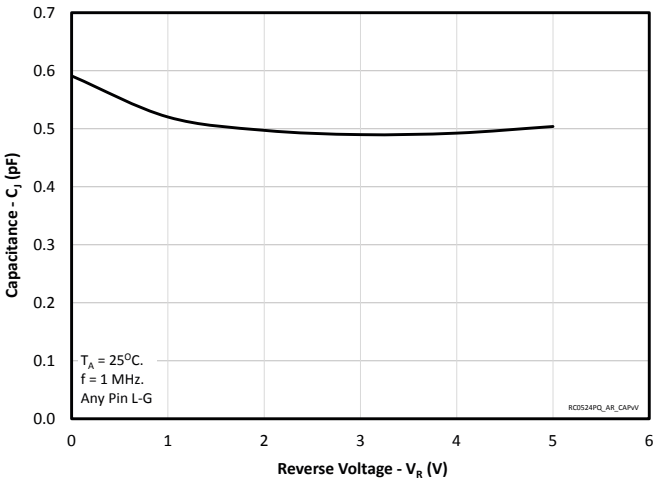
ESD Clamping (+12kV Contact per ISO-10605 330pF, 330Ω)



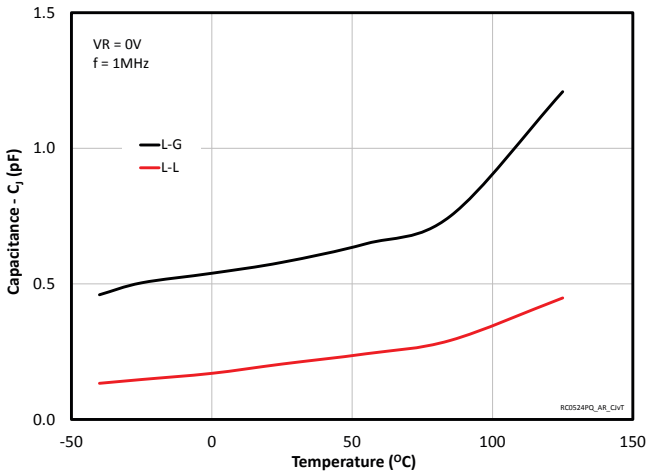
ESD Clamping (-12kV Contact per ISO-10605 330pF, 330Ω)



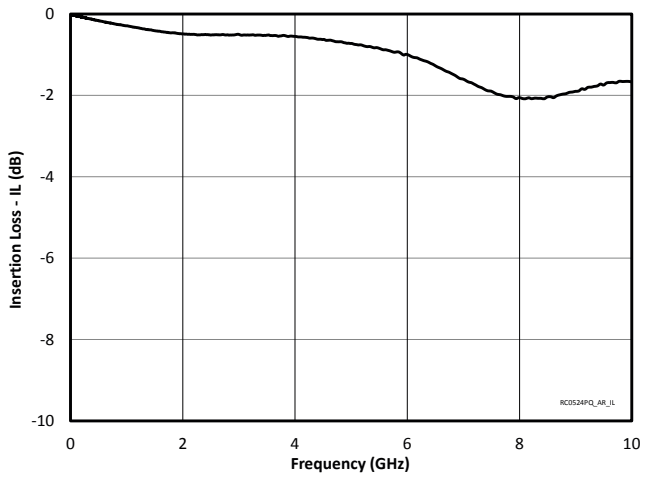
Capacitance vs. Reverse Voltage



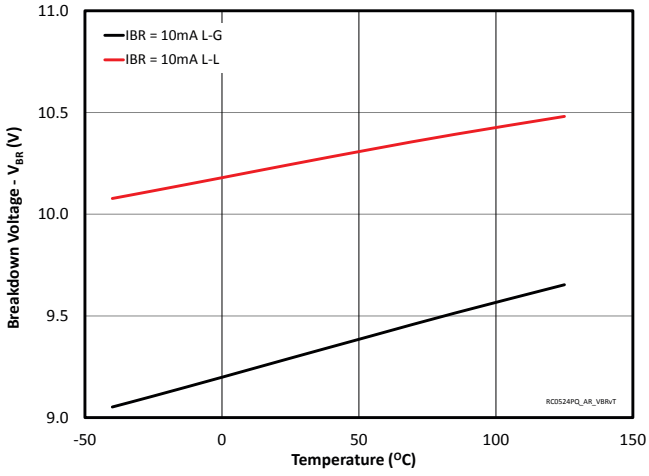
Capacitance vs. Temperature



Insertion Loss - S21



Breakdown Voltage (VBR) vs. Temperature



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm - 0.125mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles is recommended. Assuming a 125um thick stencil, the aperture dimensions shown will yield an area ratio of 0.72 for the small pads and 1.25 for the large.

Recommended Stencil Design

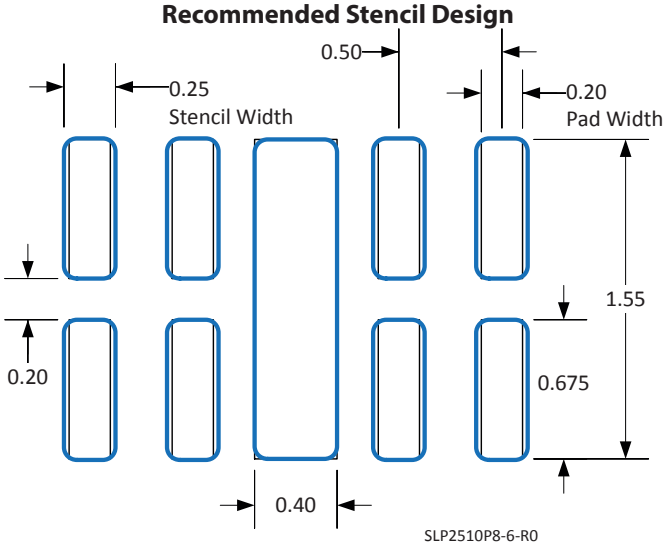


Table 2 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004") - 0.125mm (0.005")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Design Recommendations for HDMI Protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance and adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The RClamp0524PQ is specifically designed for protection of high-speed interfaces such as HDMI. It presents <0.4pF capacitance between the pairs while being rated to handle >±8kV ESD contact discharges (>±15kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. It is designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes more critical as signal speeds increase.

Applications Information

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the RClamp0524PQ. The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads.

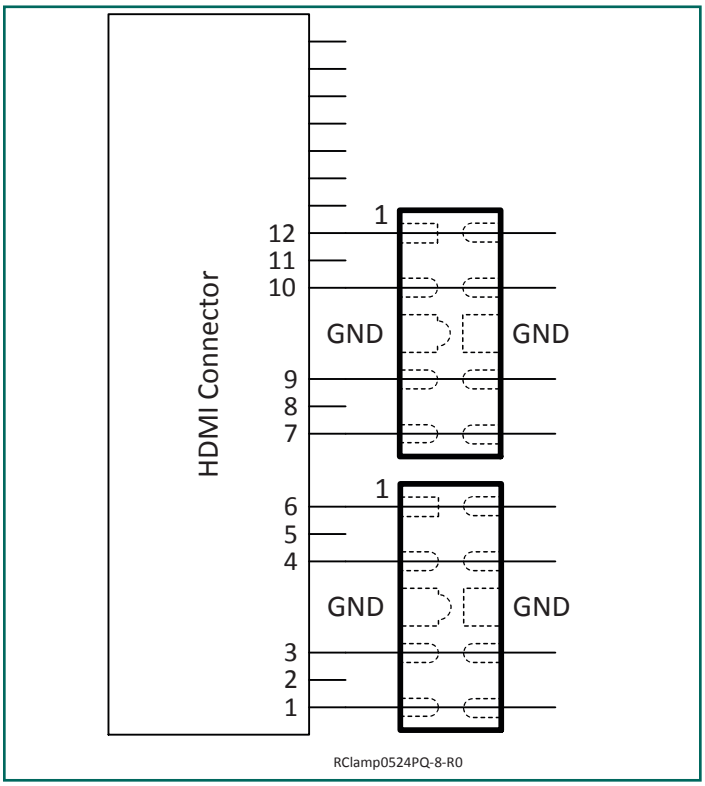


Figure 1. Flow through Layout Using RClamp0524PQ

TDR Measurements for HDMI

The combination of low capacitance, small package, and flow-through design means it is possible to use these devices to meet the HDMI impedance requirements of 100 Ohms ±15% without any PCB board modification. Figure 3 shows a typical impedance test result for a TDR risetime of 200ps using a Semtech evaluation board with 100 Ohm traces throughout. Measurements were taken using a TDR method as outlined in the HDMI Compliance Test Specification (CTS). In each case, the device meets the HDMI CTS requirement of 100 Ohm ±15% with plenty of margin (98.3Ω at 1.79 ns).

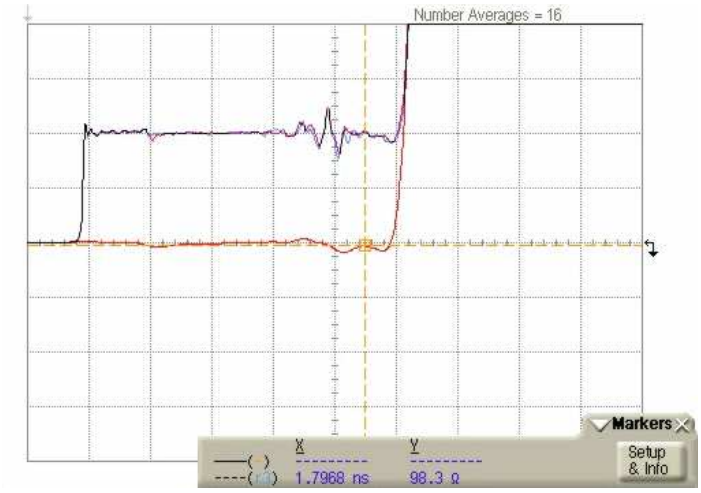


Figure 2 - TDR Measurement with 200ps risetime using Semtech Evaluation Board

Figure 3 shows a typical HDMI 1.4 eye pattern at 1080p resolution. As shown there are no violations of the eye pattern with RClamp0524PQ in the circuit. The RClamp0524PQ may also be used to protect the remaining lines (I2C, CEC, and hot plug).

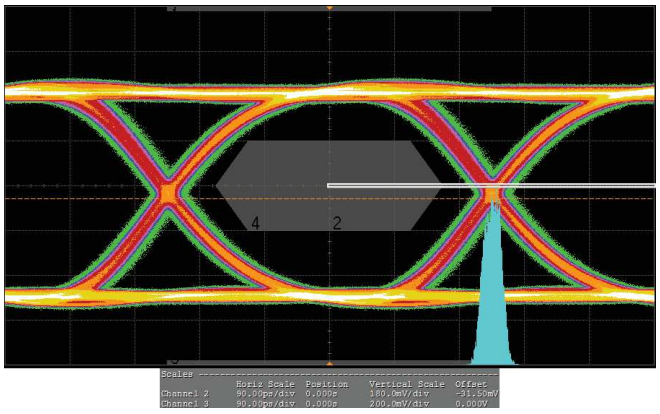


Figure 3 - HDMI 1.4 Eye Pattern with RClamp0524PQ

Applications Information

Layout Guidelines for Optimum ESD Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. this practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

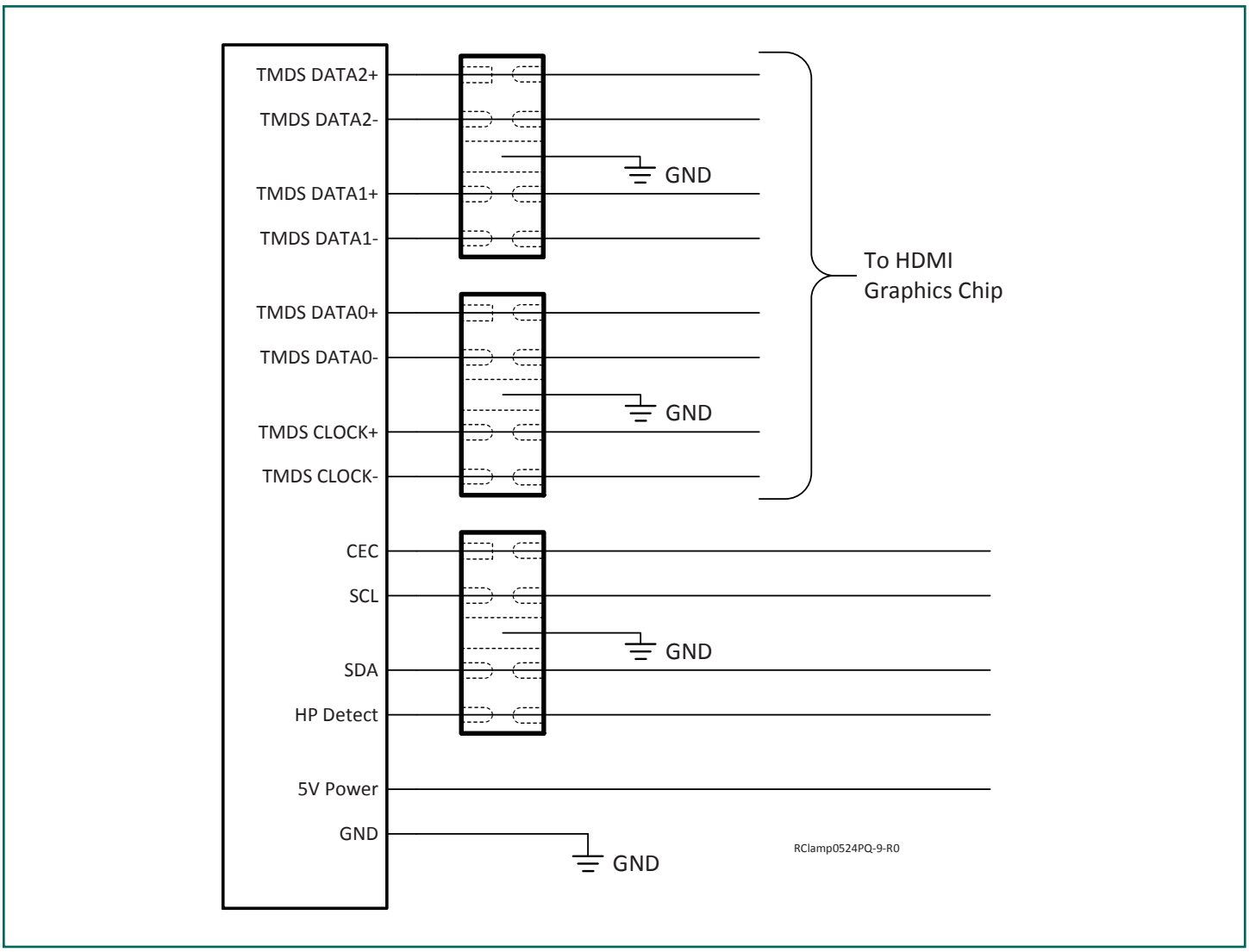
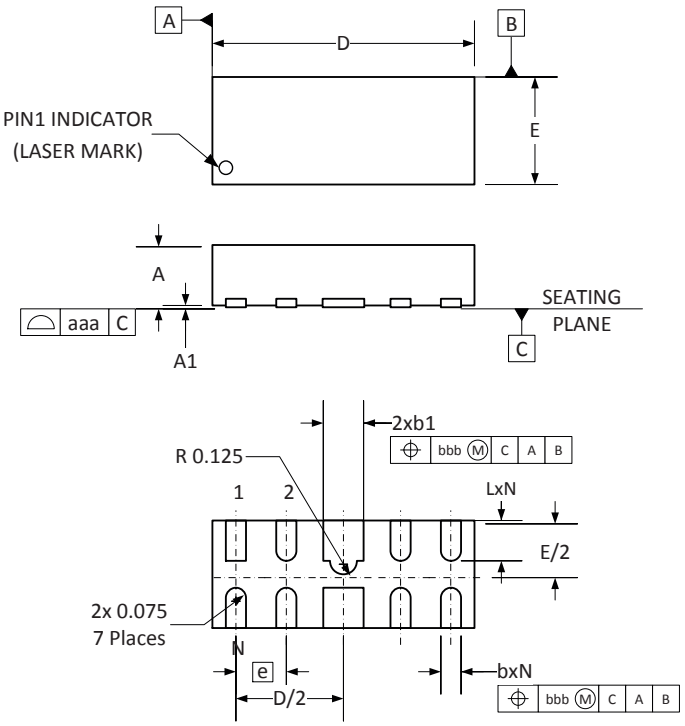


Figure 4. HDMI 1.4 Application using RClamp0524PQ

Outline Drawing - SLP2510P8

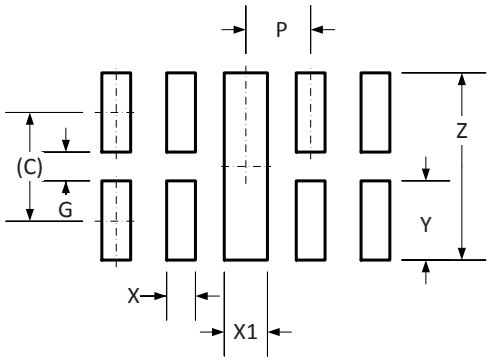


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.580	0.65
A1	0.00	0.03	0.05
A2		(0.13)	
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	2.40	2.50	2.60
E	0.90	1.00	1.10
e		0.50 BSC	
L	0.30	0.38	0.43
N		8	
aaa		0.08	
bbb		0.10	

SLP2510P8-2-R0

NOTES:
1 CONTROLLING DIMENSIONS ARE IN MILLIMETERS / ANGLES IN DEGREES

Land Pattern - SLP2510P8



DIMENSIONS	
DIM	MILLIMETERS
C	(0.875)
G	0.20
P	0.50
P1	1.00
X	0.20
X1	0.40
Y	0.675
Z	1.55

SLP2510P8-3-R0

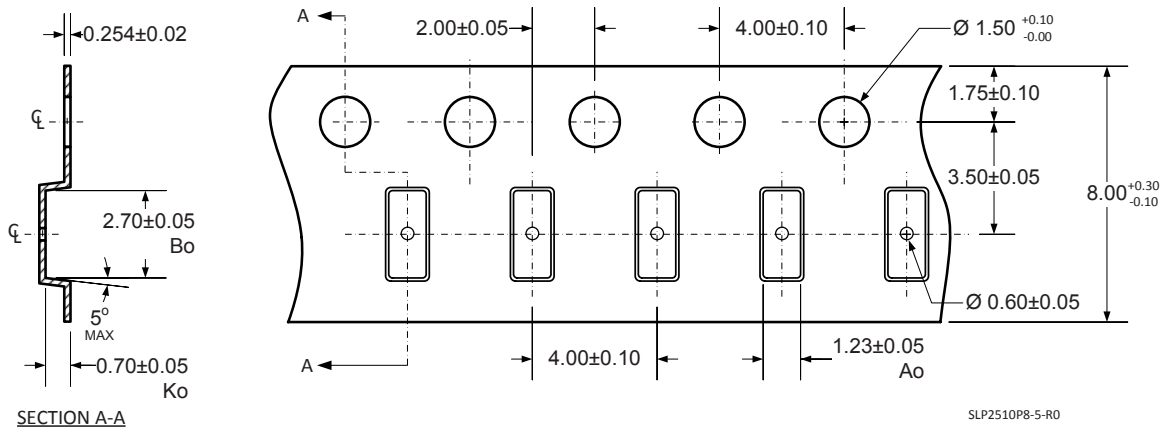
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

RClamp0524PQ-5-R0

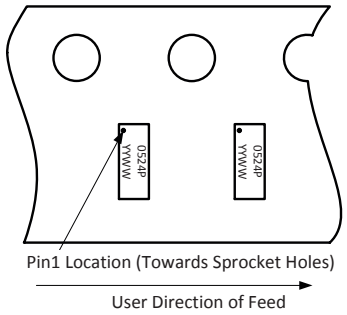
Notes: Dot indicates pin 1 location

Tape and Reel Specification



SLP2510P8-5-R0

NOTES: 1. ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED



RClamp0524PQ-6-R0

Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp0524PQTCT	3,000	7”

Contact Information

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