TEXAS INSTRUMENTS

**TPD4E1B06**

SLVSBQ8C – DECEMBER 2012 – REVISED JULY 2014
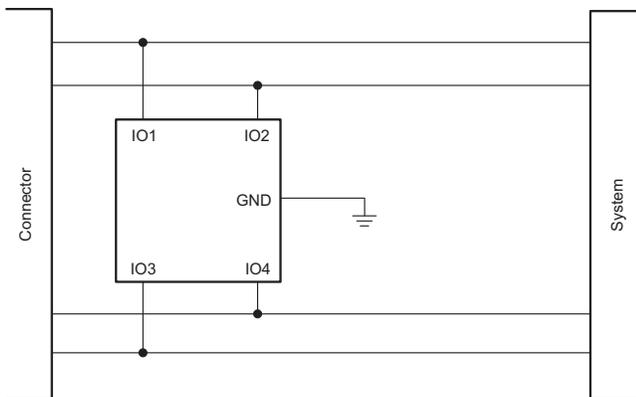
# TPD4E1B06 4-Channel Ultra Low Leakage ESD Protection Device

## 1 Features

- Ultra Low Leakage Current 0.5 nA (Max)
- Transient Protection for 4 I/O Lines
  - IEC 61000-4-2 Contact Discharge ±12 kV
  - IEC 61000-4-2 Air-Gap Discharge ±15 kV
  - IEC 61000-4-5 Surge 3.0 A (8/20 µs)
- I/O Capacitance 0.7 pF (Typ)
- Bi-directional TVS Diode Array
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to 125°C
- Small, Easy-to-Route DRL and DCK Packages

## 2 Applications

- Glucose Meter
- Tablets
- GPS
- Portable Media Players
- TV
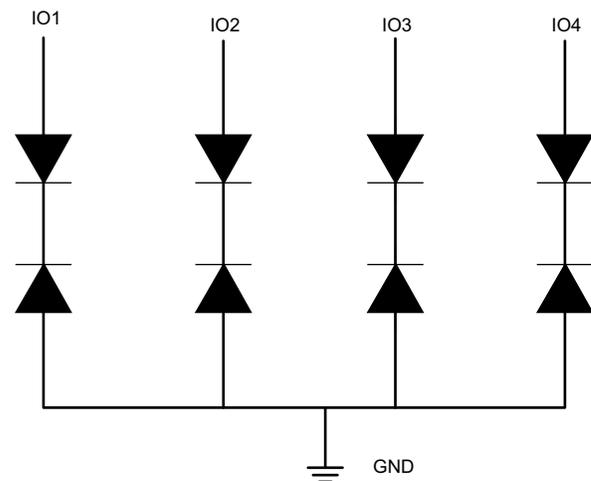- Set-top Box

## 3 Description

The TPD4E1B06 is a 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The ±12 kV contact and ±15 kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06's 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD4E1B06 | SC70 (6) | 2.00 mm × 2.10 mm |
| | SOT (6) | 1.60 mm x 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic



Functional Block Diagram

## Table of Contents

# 5 Revision History

**Changes from Revision B (May 2014) to Revision C**      **Page**
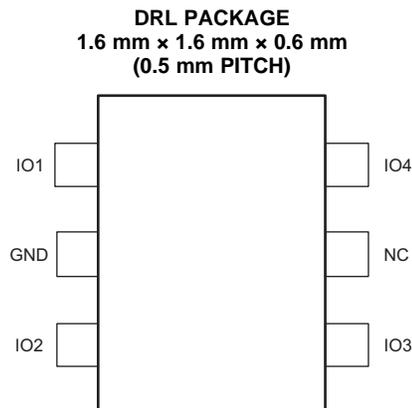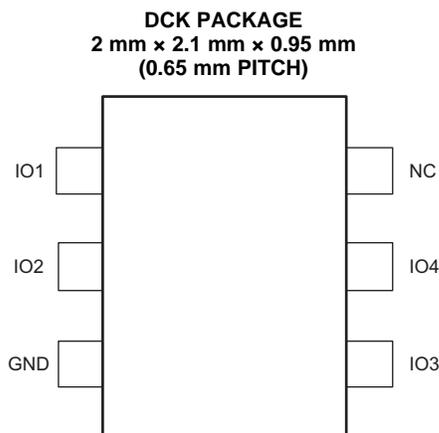
- Changed 2 device names from TPD4E6B06 to TPD4E1B06 .............................................................................. 8

**Changes from Revision A (January 2013) to Revision B**      **Page**

- Added DRL package to datasheet............................................................................................................ 1
- Changed $I_{PP}$, peak pulse current from 3.5 A to 3.0 A............................................................................ 4
- Added Handling Ratings table. ............................................................................................................. 4
- Added Recommended Operating Conditions table. ...................................................................................... 4
- Changed Electrical Characteristics table to reflect operating conditions at 25 °C. ................................................ 4
- Added MIN $V_{RWM}$ value of –5.5 V. ..................................................................................................... 4
- Changed $V_{CLAMP}$ at $I_{PP}$ = 1 A from 10.5 V to 10.9 V. ...................................................................... 4
- Changed Line Capacitance TYP value from 1 pF to 0.7 pF. ........................................................................... 4
- Added Line Capacitance MAX value of 0.95 pF. ........................................................................................ 4
- Changed $I_{LEAK}$ from MAX of 10 nA to 0.5 nA .................................................................................... 4

**Changes from Original (December 2012) to Revision A**      **Page**

- Fixed "f" units typo from GHz to MHz for $C_L$ parameter in ELECTRICAL CHARACTERISTICS table................................ 4

Product Folder Links: *TPD4E1B06*

# 6   Pin Configuration and Functions

**DCK PACKAGE**
**2 mm × 2.1 mm × 0.95 mm**
**(0.65 mm PITCH)**

IO1 —— NC
IO2 —— IO4
GND —— IO3

**DRL PACKAGE**
**1.6 mm × 1.6 mm × 0.6 mm**
**(0.5 mm PITCH)**

IO1 —— IO4
GND —— NC
IO2 —— IO3

## Pin Functions

| PIN | | | TYPE | DESCRIPTION |
|-----|-----|-----|------|-------------|
| NAME | NO. | | | |
| | DCK | DRL | | |
| IO1 | 1 | 1 | I/O | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO2 | 2 | 3 | I/O | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO3 | 4 | 4 | I/O | ESD protected channel. Connect to data line as close to the connector as possible. |
| IO4 | 5 | 6 | I/O | ESD protected channel. Connect to data line as close to the connector as possible. |
| GND | 3 | 2 | GND | Ground |
| NC | 6 | 5 | NC | Not internally connected |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Operating temperature range | | −40 | 125 | °C |
| $I_{PP}$, peak pulse current (tp = 8/20 μs), IO pin to GND | | | 3.0 | A |
| $P_{PP}$, peak pulse power (tp = 8/20 μs) | | | 45 | W |

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | −65 | 155 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | −4.0 | 4.0 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | −1.5 | 1.5 | |
| | | IEC 61000-4-2 contact ESD | −12 | 12 | |
| | | IEC 61000-4-2 air-gap ESD | −15 | 15 | |

(1)  JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 4 kV may actually have higher performance.
(2)  JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1.5 kV may actually have higher performance.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IO}$ | The voltage between any two device pins should not exceed 5.5 V | −5.5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | −40 | 125 | °C |

## 7.4 Thermal Information

| | | TPD4E1B06 | | UNIT |
|---|---|---|---|---|
| | | DCK | DRL | |
| | THERMAL METRIC[1] | 6 PINS | 6 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 227.3 | 233.4 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 79.5 | 95.5 | |
| $R_{θJB}$ | Junction-to-board thermal resistance | 72.1 | 68.1 | |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 3.6 | 7.6 | |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 70.4 | 67.9 | |

(1)  For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage | | −5.5 | | 5.5 | V |
| $V_{CLAMP}$ | Clamp voltage with ESD strike, IO to GND | $I_{PP}$ = 1 A, tp = 8/20 μSec, from I/O to GND or GND to I/O | | 10.9 | | V |
| | | $I_{PP}$ = 3 A, tp = 8/20 μSec, from I/O to GND or GND to I/O | | 14.5 | | V |
| $R_{DYN}$ | Dynamic resistance | $I_{TLP}$ = 10 A to 20 A, I/O to GND | | 1 | | Ω |
| | | $I_{TLP}$ = 10 A to 20 A, GND to I/O | | 0.8 | | |
| $C_L$ | Line capacitance | f = 1 MHz, $V_{BIAS}$ = 2.5 V | | 0.7 | 0.95 | pF |
| $V_{BR}$ | Break-down voltage | $I_{IO}$ = 1 mA, from I/O to GND or GND to I/O | 7 | | 9.5 | V |
| $I_{LEAK}$ | Leakage current | $V_{IO}$ = 2.5 V | | | 0.5 | nA |

## 7.6 Typical Characteristics
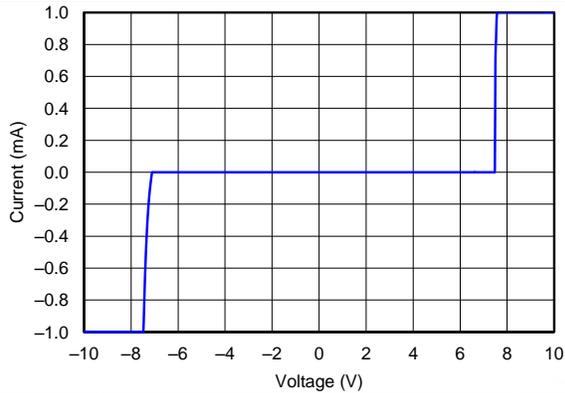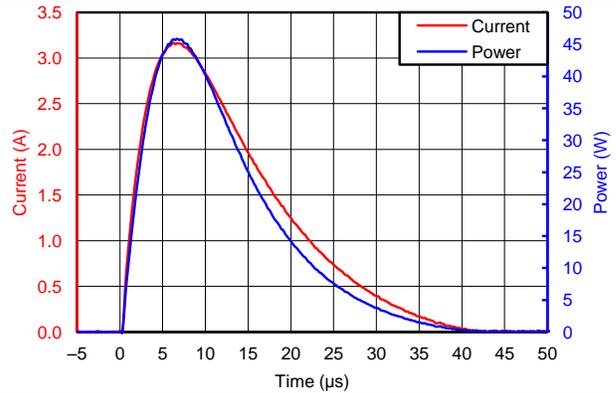
**Figure 1. DC Voltage Sweep I-V Curve**

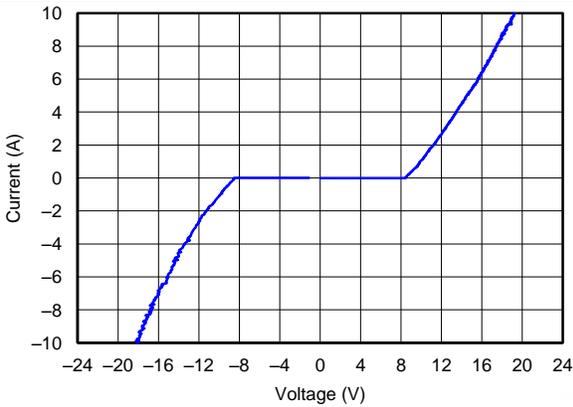**Figure 2. Surge Curve (tp = 8/20 μs), Pin IO to GND**
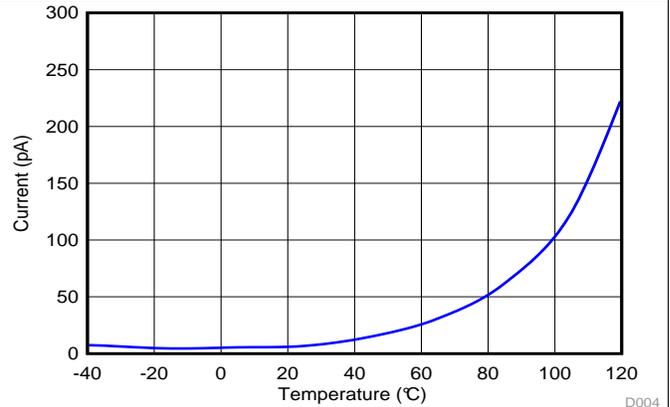
**Figure 3. TLP Plot IO to GND**

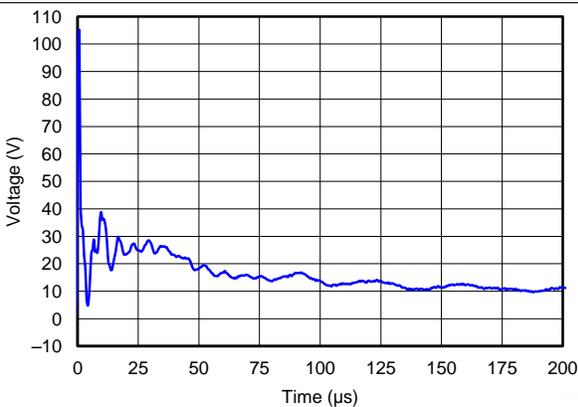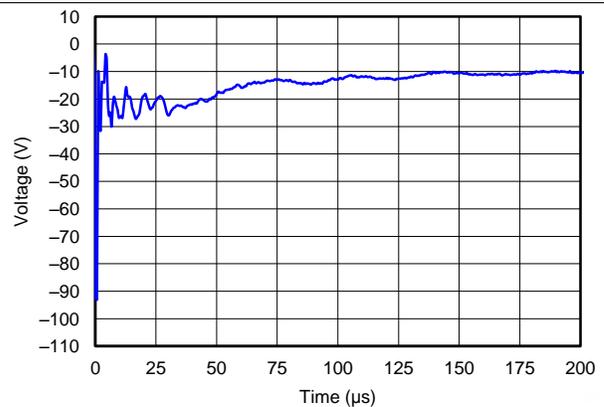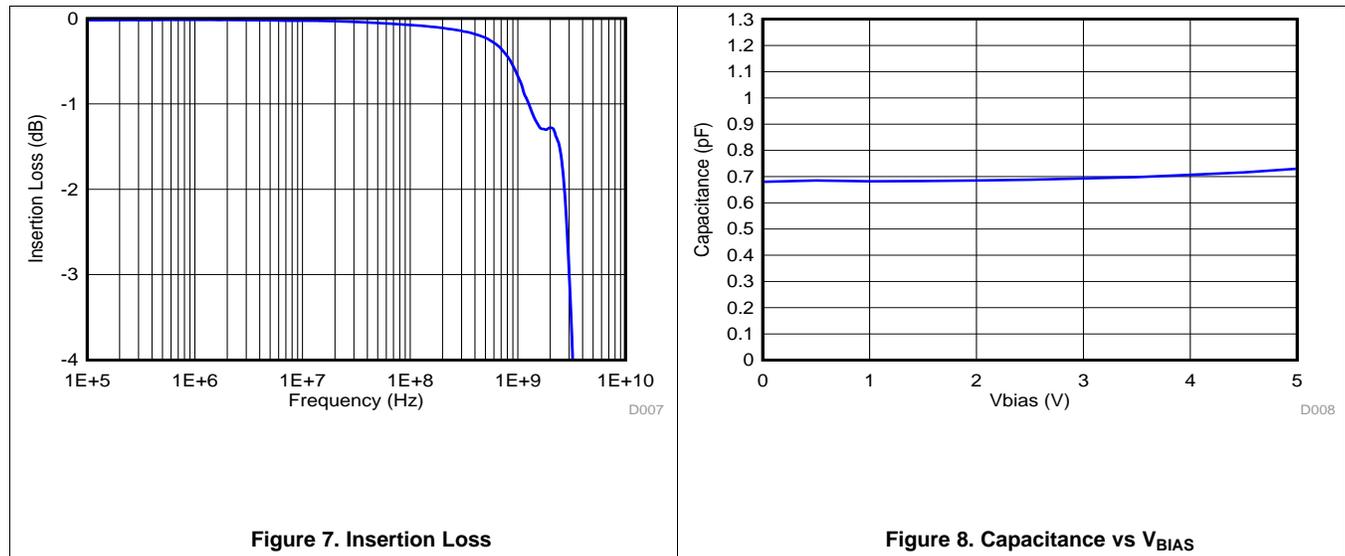**Figure 4. Leakage vs Temperature**

**Figure 5. +8 kV IEC Waveform**

**Figure 6. –8 kV IEC Waveform**

## Typical Characteristics (continued)



**Figure 7. Insertion Loss**



**Figure 8. Capacitance vs V$_{BIAS}$**

Product Folder Links: *TPD4E1B06*

# 8 Detailed Description

## 8.1 Overview

The TPD4E1B06 is a 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The ±12 kV contact and ±15 kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06's 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

## 8.2 Functional Block Diagram
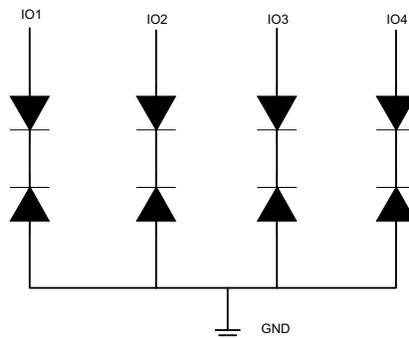


## 8.3 Feature Description

The TPD4E1B06 is a 4-channel bi-directional Transient Voltage Suppressor (TVS) diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The ±12 kV contact and ±15 kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06's 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

### 8.3.1 Ultra low Leakage Current 0.5 nA (Max)

TPD4E1B06 ultra-low leakage current supports long battery life and allows for precision analog measurements.

### 8.3.2 Transient Protection for 4 I/O Lines

The four I/O pins of TPD4E1B06 can withstand ESD events up to ±12 kV contact and ±15 kV air gap per IEC61000-4-2.

### 8.3.3 I/O Capacitance 0.7 pF (Typ)

TPD4E1B06 I/O pins present an ultra-low 0.7 pF capacitance to the protected signal lines, making it suitable for a wide range of applications.

### 8.3.4 Bi-directional TVS diode array

TPD4E1B06 diode array structure uses back to back diode topology to accommodate bi-directional signaling between −5.5 V and 5.5 V.

### 8.3.5 Low ESD Clamping Voltage

TPD4E1B06 clamps ESD events to a safe level to protect system components.

## 8.4 Device Functional Modes

TPD4E1B06 is a passive integrated circuit that activates whenever fast transient voltages above $V_{BR}$ or below −$V_{BR}$ are present on the circuit being protected. During ESD events, voltages as high as ±12 kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1B06 (usually within 10's of nano-seconds) the device reverts to passive.

# 9 Application and Implementation

## 9.1 Application Information

TPD4E1B06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS diode, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a safe level to the protected IC.

## 9.2 Typical Application
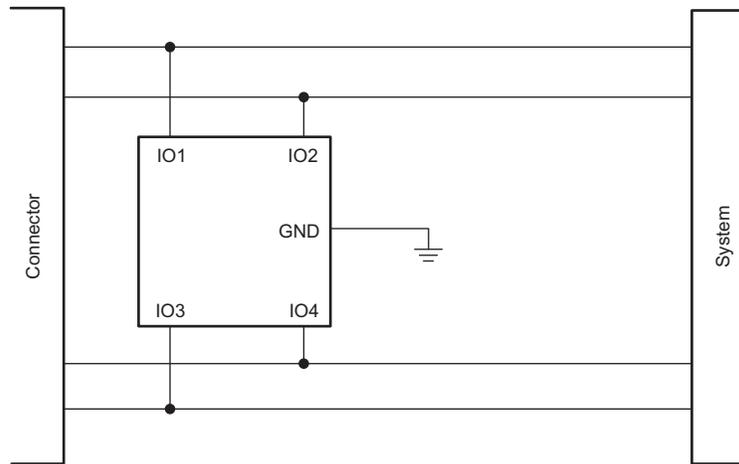


**Figure 9. Protecting a Pair of Bi-Directional Differential Data Lines**

The typical application of the TBD4E1B06 is to be placed in between the connector and the system. The low capacitance of the TBD4E1B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

### 9.2.1 Design Requirements

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Signal range on IO1, IO2, IO3, IO4 Pins | −5.5 V to 5.5 V |
| Operating frequency | 1.7 GHz |

### 9.2.2 Detailed Design Procedure

The designer needs to know the following:
- Signal range on all the protected lines
- Operating frequency

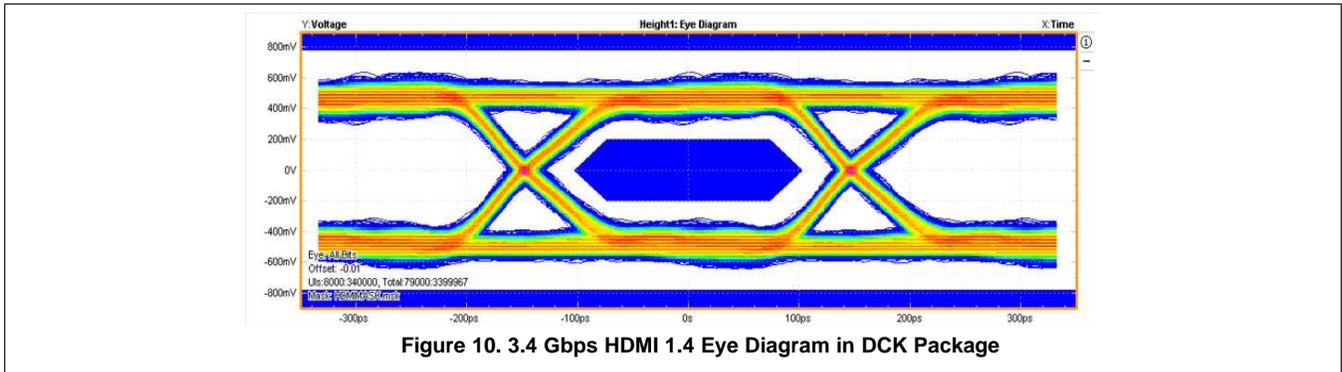#### 9.2.2.1 Signal Range on IO1, IO2, IO3, and IO4 Pins

TPD4E1B06 has 4 protection channels for signal lines. Any I/O will support a signal range of −5.5 V to 5.5 V.

#### 9.2.2.2 Operating Frequency

The 0.7 pF capacitance of each I/O channel supports data rates up to 3.4 Gbps.

Product Folder Links: *TPD4E1B06*

## 9.2.3 Application Curves



**Figure 10. 3.4 Gbps HDMI 1.4 Eye Diagram in DCK Package**

## 10 Layout

### 10.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer should minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 10.2 Layout Examples

Figure 11 shows a layout example for theTPD4E1B06DCK. Pins 1 & 2 and 4 & 5 are routed differentially. Pin 3 is routed to the ground plane. Pin 6 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 6 to the ground plane.

**Figure 11. DCK Layout Example Showing Two Data Pairs, D0 and D1**

Figure 12 shows a layout example for theTPD4E1B06DRL. Pins 1 & 6 and 3 & 4 are routed differentially. Pin 2 is routed to the ground plane. Pin 5 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 5 to the ground plane.
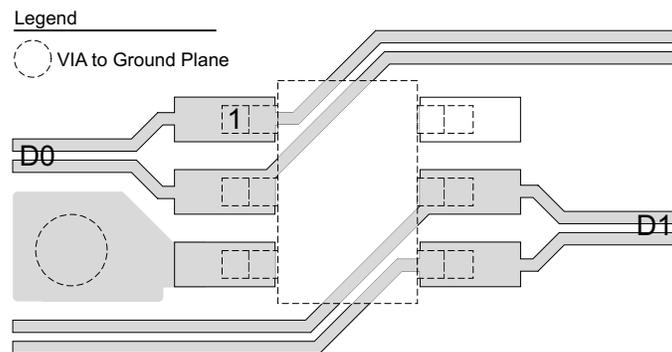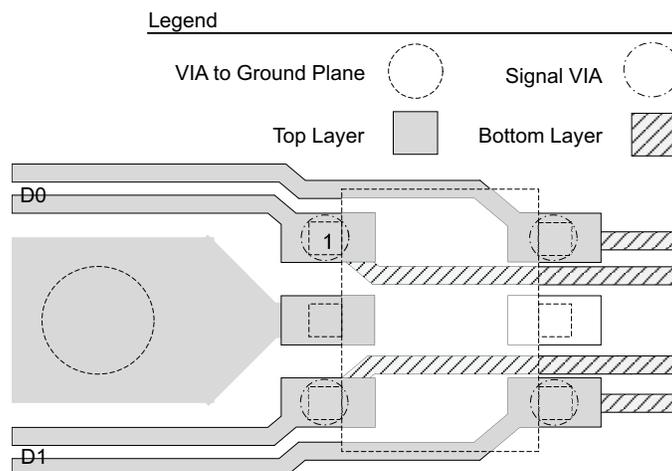
**Figure 12. DRL Layout Example Showing Two Data Pairs, D0 and D1**

Product Folder Links: *TPD4E1B06*

# 11 Device and Documentation Support

## 11.1 Trademarks

All trademarks are the property of their respective owners.

## 11.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4E1B06DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BYP | Samples |
| TPD4E1B06DRLR | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (BYG, BYH) | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | | |
|---|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4E1B06DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 8.4 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPD4E1B06DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**
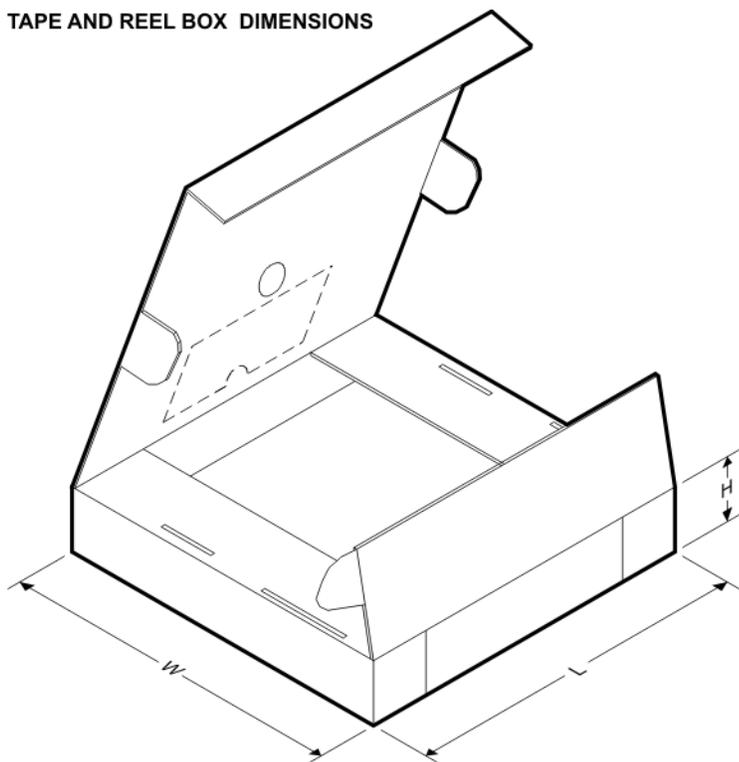


*All dimensions are nominal

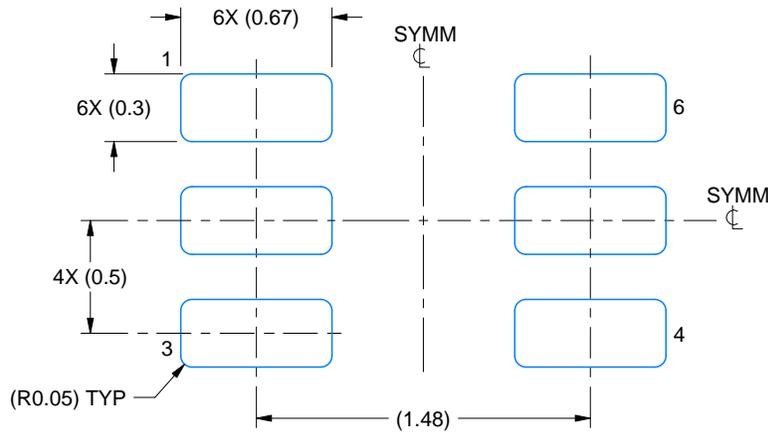| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD4E1B06DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPD4E1B06DRLR | SOT-5X3 | DRL | 6 | 4000 | 183.0 | 183.0 | 20.0 |
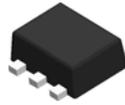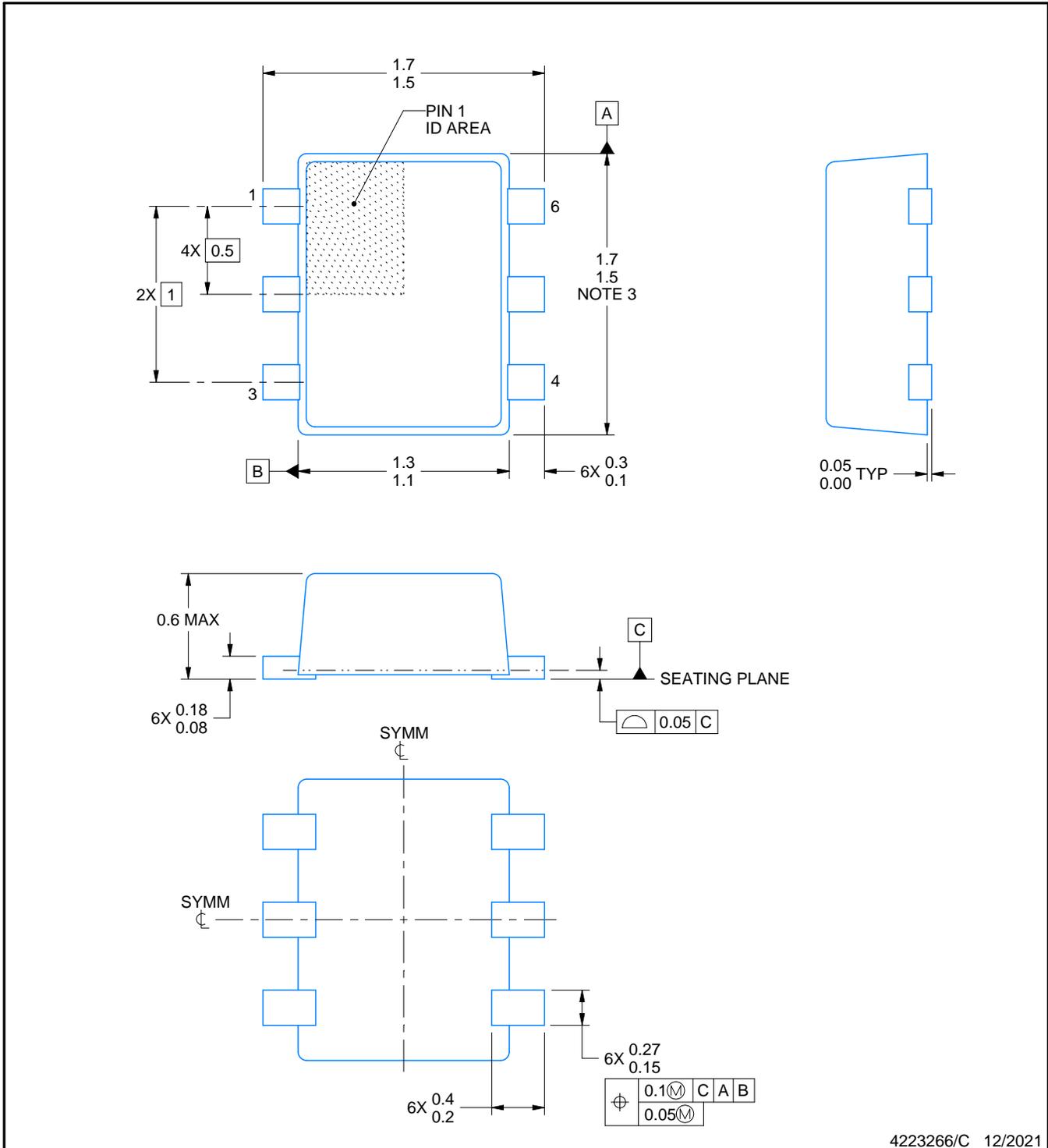
4223266/C   12/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

6X (0.67)

SYMM
₵

1
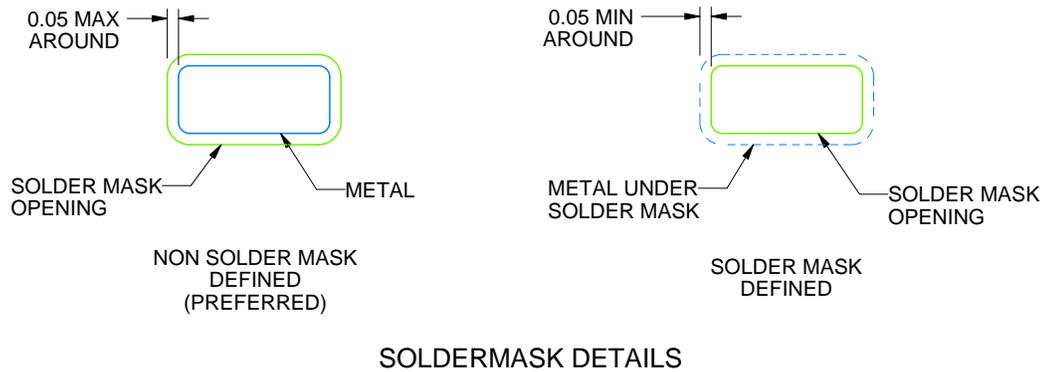
6X (0.3)

6

SYMM
₵

4X (0.5)

3

4

(R0.05) TYP

(1.48)

LAND PATTERN EXAMPLE
SCALE:30X

0.05 MAX
AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDERMASK DETAILS
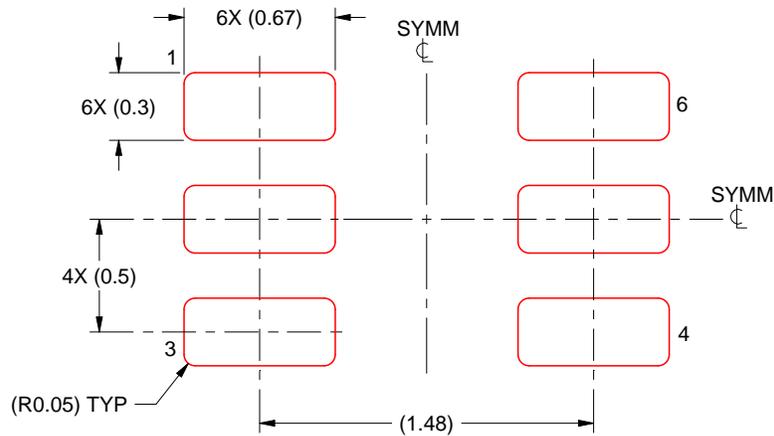
4223266/C   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

## DRL0006A

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
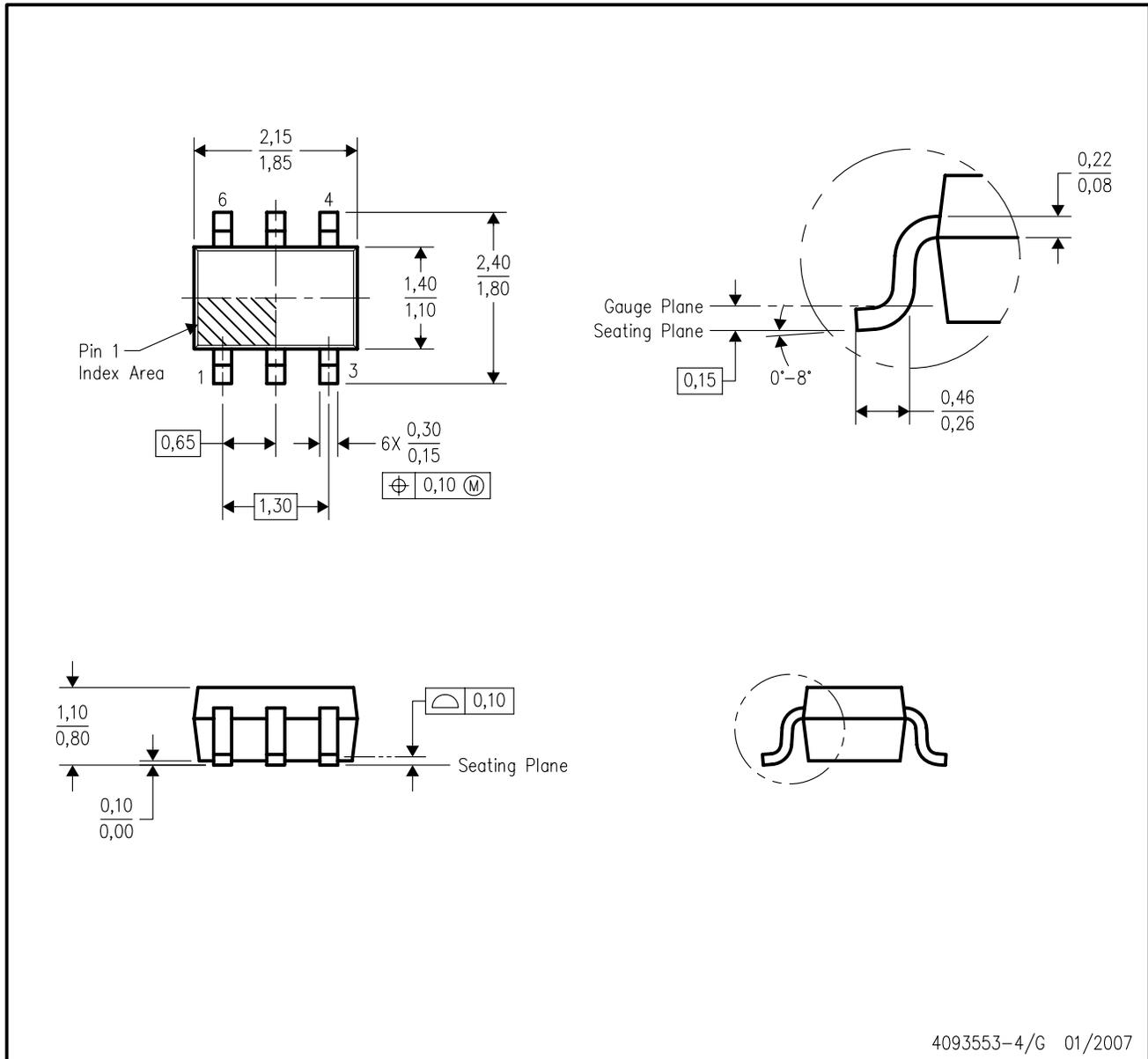BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C   12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R−PDSO−G6)                    PLASTIC SMALL−OUTLINE PACKAGE



4093553−4/G  01/2007

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AB.
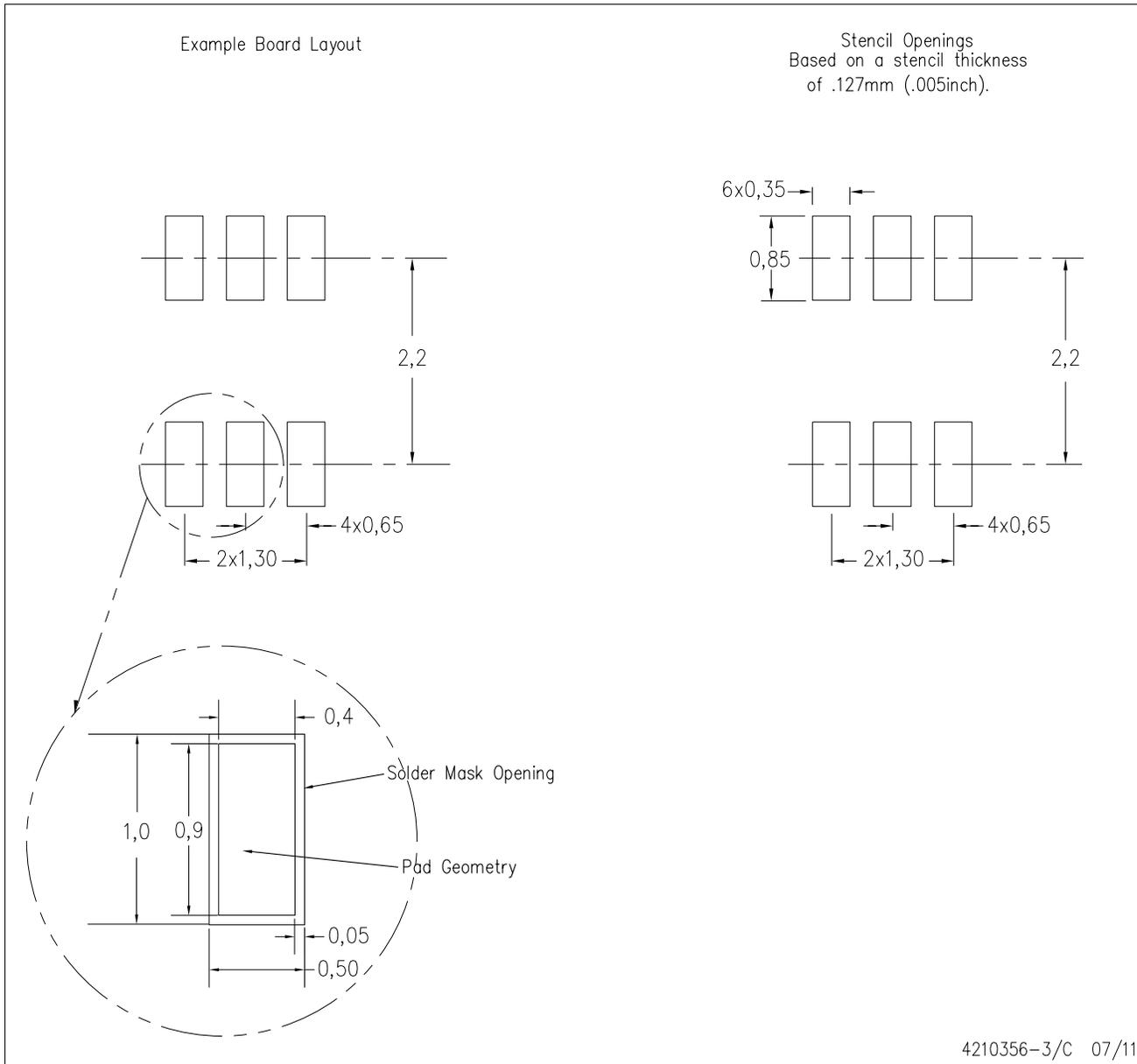
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DCK (R−PDSO−G6)                    PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

2,2

4x0,65

2x1,30

6x0,35

0,85

2,2

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0    0,9

Pad Geometry

0,05

0,50

4210356−3/C  07/11

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.  Publication IPC−7351 is recommended for alternate designs.
         E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
             metal load solder paste.  Refer to IPC−7525 for other stencil recommendations.

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