3V 140ksps 12-Bit Sampling A/D Converter with Reference

FEATURES

- **Single Supply 3V or ±3V Operation**
- **140ksps Throughput Rate**
- **12mW (Typ) Power Dissipation**
- On-Chip 25ppm/°C Reference
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- 69dB S/(N + D) and 77dB THD at Nyquist
- ±0.5LSB INL and ±0.75LSB DNL Max (A Grade)
- 2.7V Guaranteed Minimum Supply Voltage
- ESD Protected On All Pins
- 24-Pin SW Package
- 0V to 2.5V or ±1.25V Input Ranges

APPLICATIONS

- 3V Powered Systems
- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

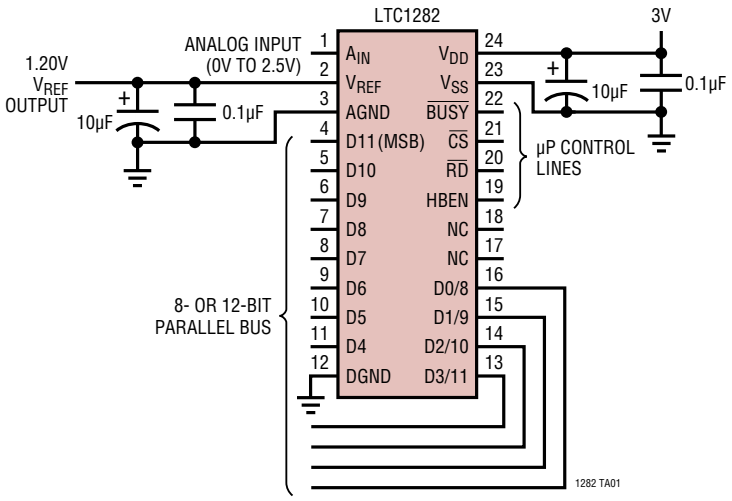
The LTC®1282 is a 6µs, 140ksps, sampling 12-bit A/D converter that draws only 12mW from a single 3V or dual ±3V supply. This easy-to-use device comes complete with 1.14µs sample-and-hold, precision reference and internally trimmed clock. Unipolar and bipolar conversion modes provide flexibility for various applications. They are built with LTBiCMOSTM switched capacitor technology.

The LTC1282 has a 25ppm/°C (max) internal reference and converts 0V to 2.5V unipolar inputs from a single 3V supply. With ±3V supplies its input range is ±1.25V with two's complement output format. Maximum DC specifications include ±0.5LSB INL, ±0.75LSB DNL and 25ppm/°C full-scale drift over temperature. Outstanding AC performance includes 69dB S/(N + D) and 77dB THD at the Nyquist input frequency of 70kHz.

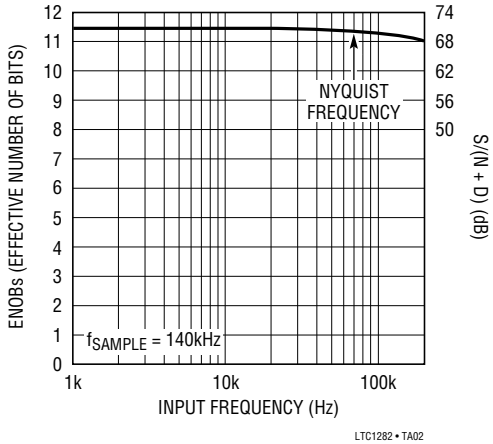
The internal clock is trimmed for 6µs maximum conversion time. The clock automatically synchronizes to each sample command eliminating problems with asynchronous clock noise found in competitive devices. A high speed parallel interface eases connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Single 3V Supply, 140ksps, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency



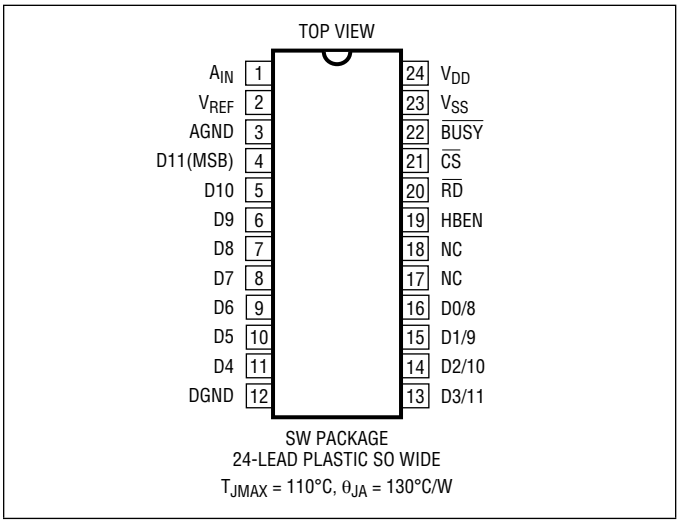
Rev. B

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{DD}) 12V
Negative Supply Voltage (V_{SS}) ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} – 0.3V to 12V
Digital Output Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Specified Temperature Range (Note 14) ..... 0°C to 70°C
Operating Temperature Range
LTC1282AC, LTC1282BC ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1282ACSW#PBF	LTC1282ACSW#TRPBF	LTC1282ACSW	24-Lead Plastic SO Wide	0°C to 70°C
LTC1282BCSW#PBF	LTC1282BCSW#TRPBF	LTC1282BCSW	24-Lead Plastic SO Wide	0°C to 70°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With Internal Reference (Notes 5 and 6)

PARAMETER	CONDITIONS		LTC1282A MIN	LTC1282A TYP	LTC1282A MAX	LTC1282B MIN	LTC1282B TYP	LTC1282B MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7) Commercial Military	● ● 			±1/2 ±1/2 ±3/4			±1 ±1 ±1	LSB LSB LSB
Differential Linearity Error	Commercial Military	● ●			±3/4 ±1			±1 ±1	LSB LSB
Offset Error	(Note 8)	●			±3 ±4			±4 ±6	LSB LSB
Gain Error					±10			±15	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±5	±25		±10	±45	ppm/°C
Power Supply Rejection	(Note 9) V_{DD} ±10% (Note 10) V_{SS} ±10%			±0.3 ±0.1			±0.3 ±0.1		LSB LSB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1282A/LTC1282B MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	10kHz/70kHz Input Signal		71/69		dB
THD	Total Harmonic Distortion	10kHz/70kHz Input Signal, Up to 5th Harmonic		–82/–77		dB
	Peak Harmonic or Spurious Noise	10kHz/70kHz Input Signal		–82/–77		dB
IMD	Intermodulation Distortion	f_{IN1} = 19.0kHz, f_{IN2} = 20.6kHz		–78		dB
	Full Power Bandwidth			4		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)			200		kHz

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 11)	2.7V ≤ V_{DD} ≤ 3.6V (Unipolar Mode) 3V ≤ V_{DD} ≤ 3.6V, –3.3V ≤ V_{SS} ≤ –2.5V (Bipolar Mode)			0 to 2.5 ±1.25		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			63 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Commercial Military	● ●		0.45	1.14 1.5	µs µs

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		1.1900	1.200	1.210	1.190	1.200	1.210	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±5	±25		±10	±45	ppm/°C
V_{REF} Line Regulation	2.7V ≤ V_{DD} ≤ 3.6V			0.55			0.55		LSB/V
	–3.6V ≤ V_{SS} ≤ –2.7V			0.02			0.02		LSB/V
V_{REF} Load Regulation	0V ≤ $\|I_{OUT}\|$ ≤ 1mA			3			3		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.7V	●			0.45	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 2.7V I_O = –10µA I_O = –200µA	 ●	 2.3	 2.6		 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.7V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High Z Output Leakage D11-D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High Z Output Capacitance D11-D0/8	$\overline{CS}$ High (Note 12)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–4.5		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			4.5		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	Unipolar Mode (Note 13) Bipolar Mode (Note 13)		2.7 3.0		3.6 3.6	V V
V_{SS}	Negative Supply Voltage	Bipolar Operation (Note 13)		–3.6		–2.5	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 140ksps	●		4	7.8	mA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 140ksps	●		0.03	0.15	mA
P_D	Power Dissipation	f_{SAMPLE} = 140ksps	●		12	24	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 1 and 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	Commercial (Note 13) Military (Note 13)	● ●	140 120			kHz kHz
t_{CONV}	Conversion Time	Commercial Military	● ●			6.0 6.5	µs µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time		●	0			ns
t_2	$\overline{RD}$↓ to $\overline{BUSY}$↓ Delay	C_L = 50pF Commercial Military	 ● ●		140	200 230 260	ns ns ns
t_3	Data Access Time After $\overline{RD}$↓	C_L = 20pF (Note 13) Commercial Military	 ● ●		100	180 200 220	ns ns ns
		C_L = 100pF (Note 13) Commercial Military	 ● ●		110	200 240 260	ns ns ns
t_4	$\overline{RD}$ Pulse Width	(Note 13)	●	t_3			ns
t_5	$\overline{CS}$ to $\overline{RD}$ Hold Time	(Note 13)	●	0			ns
t_6	Data Setup Time After $\overline{BUSY}$↑	(Note 13) Commercial Military	 ● ●		60	85 110 120	ns ns ns
t_7	Bus Relinquish Time	(Note 13) Commercial Military	 ● ●	40 40 40	60	120 130 150	ns ns ns
t_8	HBEN to $\overline{RD}$ Setup Time	(Note 13)	●	0			ns
t_9	HBEN to $\overline{RD}$ Hold Time	(Note 13)	●	0			ns
t_{10}	Delay Between $\overline{RD}$ Operations		●	40			ns
t_{11}	Delay Between Conversions	Commercial (Note 13) Military (Note 13)	● ●	1140 1500	450		ns ns
t_{12}	Aperture Delay of Sample-and-Hold				30		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 3V, V_{SS} = 0V for unipolar mode and V_{SS} = –3V for bipolar mode, f_{SAMPLE} = 140kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

TIMING CHARACTERISTICS (Note 5)

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the different voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Full-scale change when V_{SS} = 0V (Unipolar Mode) or –3V (Bipolar Mode).

Note 10: Full-scale change when V_{DD} = 3V.

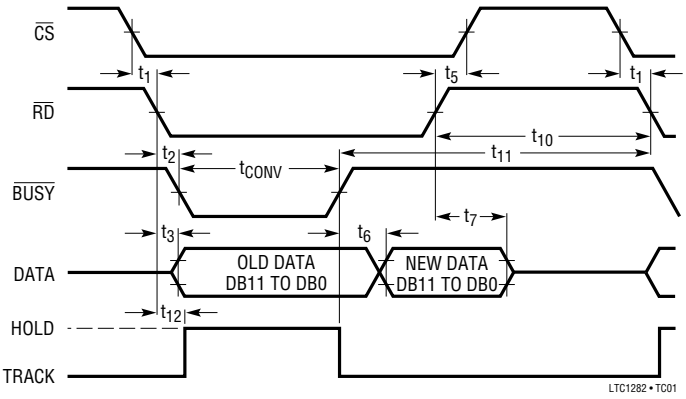
Note 11: The LTC1282 can perform unipolar and bipolar conversions. When V_{SS} is grounded (i.e. –0.1V ≤ V_{SS}), the ADC will convert in unipolar mode with input voltage of 0V to 2.5V. When V_{SS} is taken negative (i.e. V_{SS} ≤ –2.5V), the ADC will convert in bipolar mode with an input voltage of ±1.25V. A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy.

Note 12: Guaranteed by design, not subject to test.

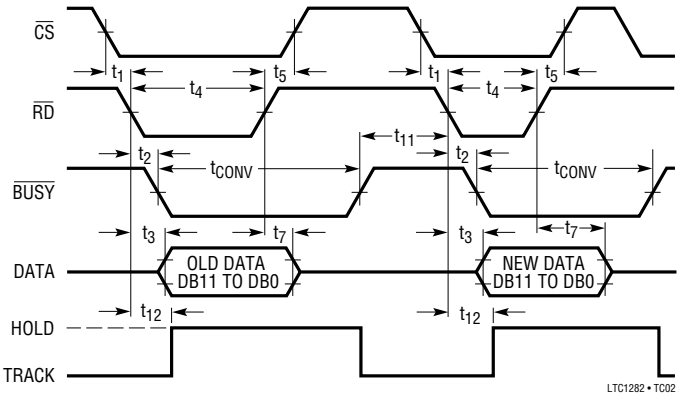
Note 13: Recommended operating conditions.

Note 14: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

Slow Memory Mode, Parallel Read Timing Diagram

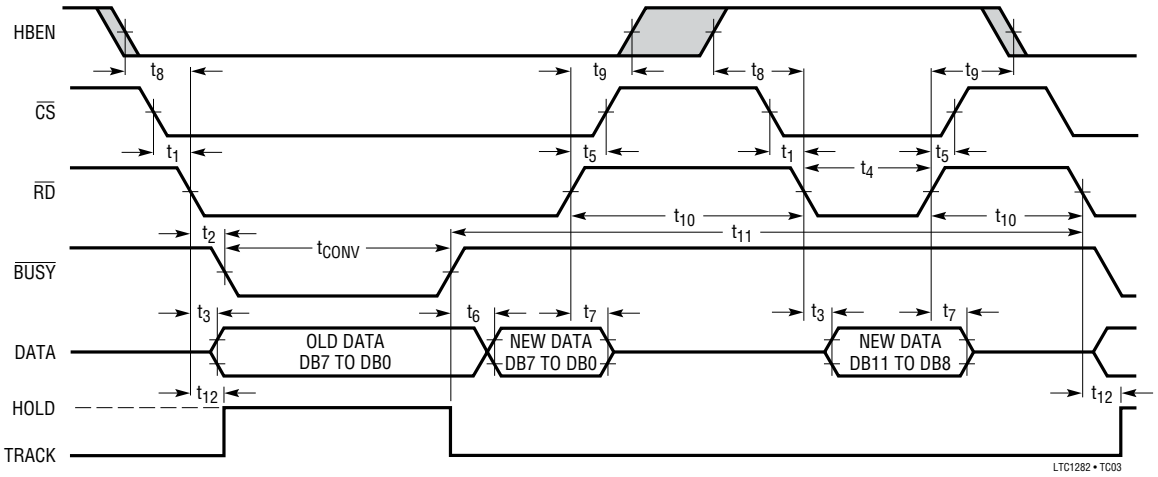


ROM Mode, Parallel Read Timing Diagram

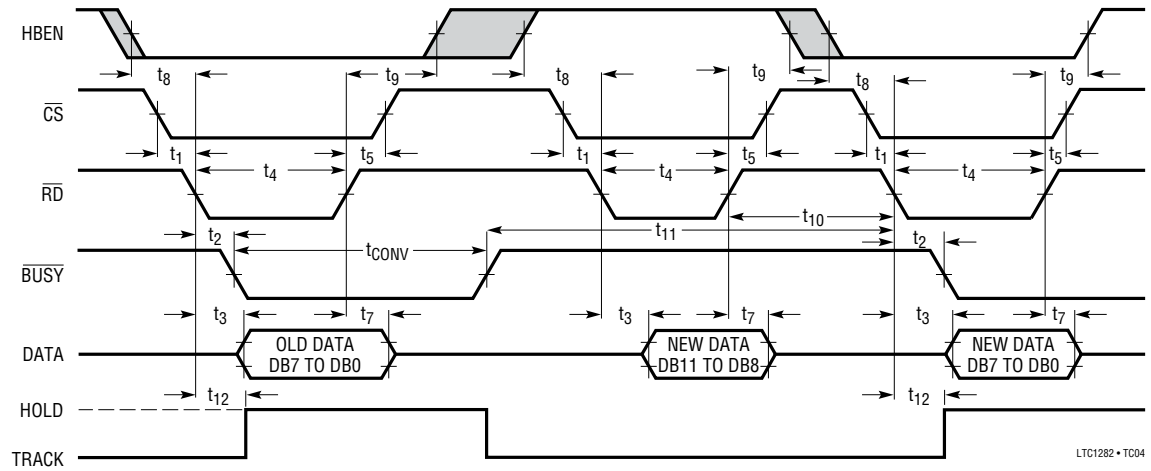


TIMING CHARACTERISTICS

Slow Memory Mode, Two Byte Read Timing Diagram

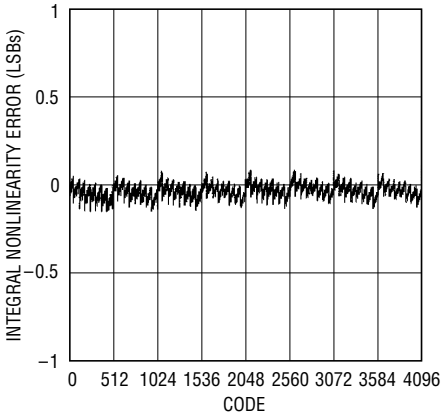


ROM Mode, Two Byte Read Timing Diagram



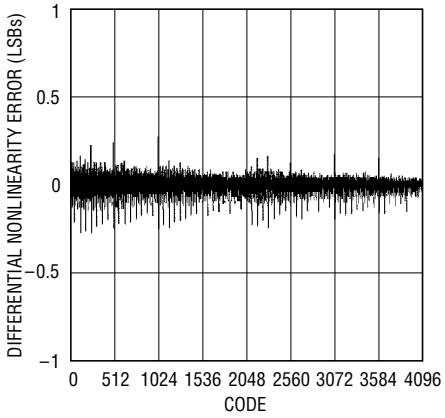
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity



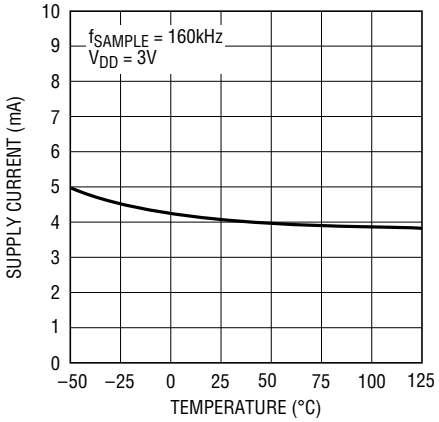
LTC1282 • TPC01

Differential Nonlinearity



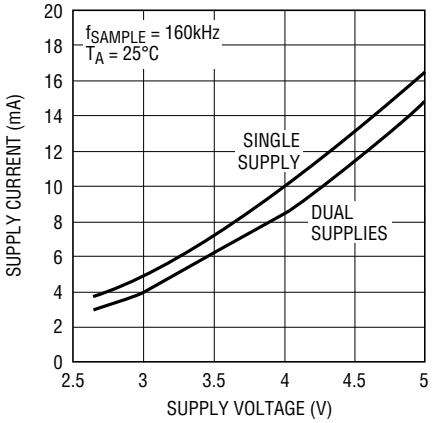
LTC1282 • TPC02

Supply Current (I_{DD}) vs Temperature



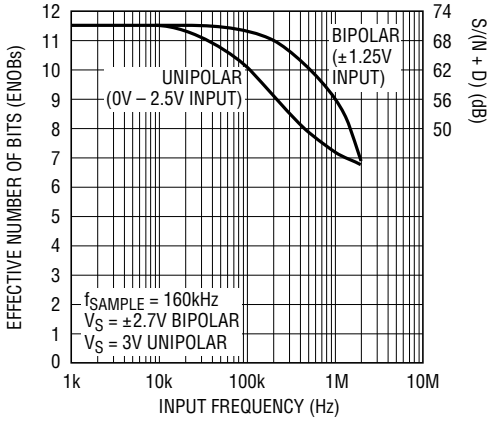
LTC1282 • TPC03

Supply Current (I_{DD}) vs Supply Voltage



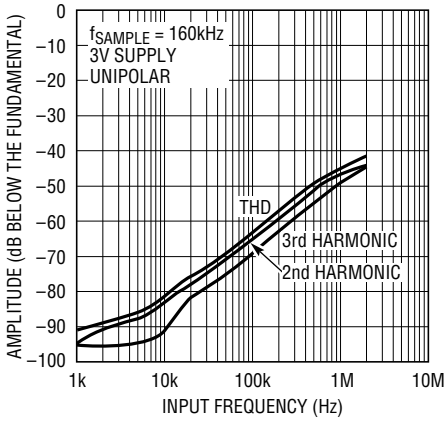
LTC1282 • TPC04

ENOBs and S/(N + D) vs Input Frequency



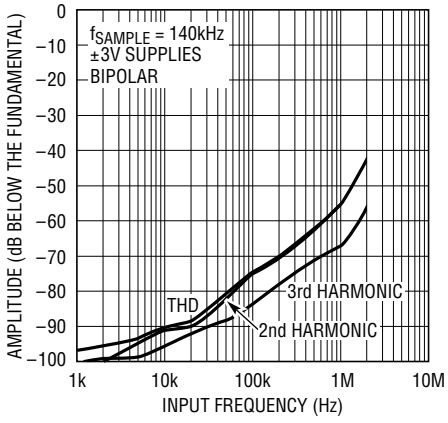
LTC1282 • TPC05

Distortion vs Input Frequency (Unipolar)



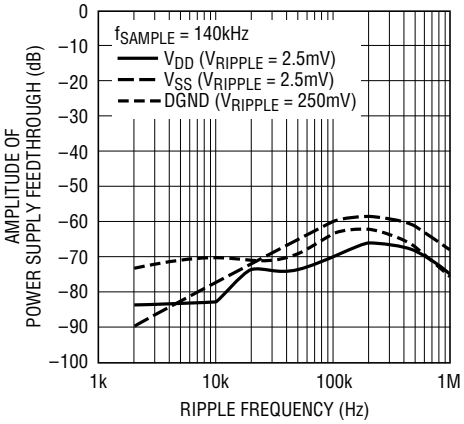
LTC1282 • TPC06

Distortion vs Input Frequency (Bipolar)



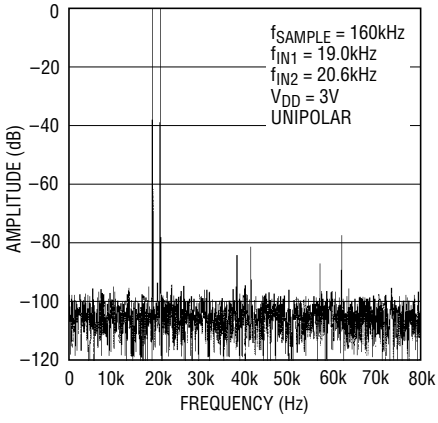
LTC1282 • TPC07

Power Supply Feedthrough vs Ripple Frequency



LTC1282 • TPC08

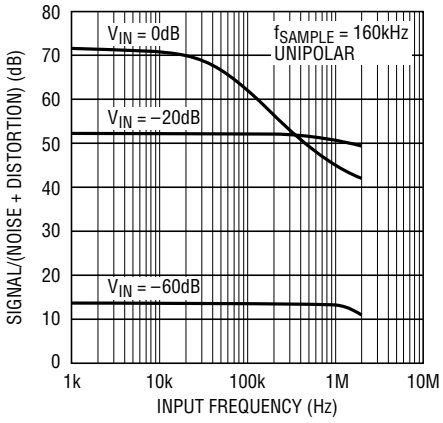
Intermodulation Distortion Plot



LTC1282 • TPC09

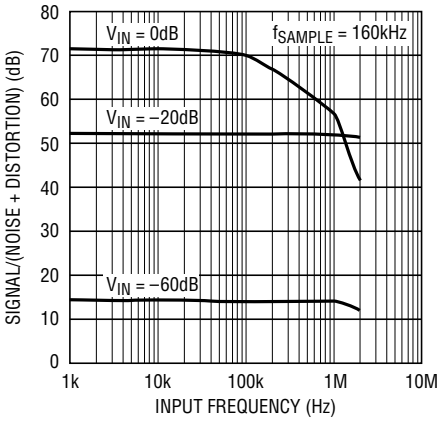
TYPICAL PERFORMANCE CHARACTERISTICS

S/(N + D) vs Input Frequency and Amplitude (Unipolar, V_{DD} = 3V)



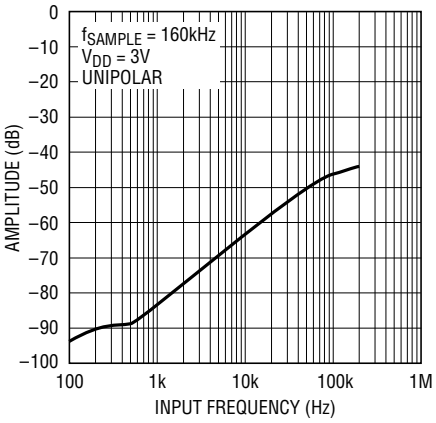
LTC1282 • TPC10

S/(N + D) vs Input Frequency and Amplitude (Bipolar, ±3V Supplies)



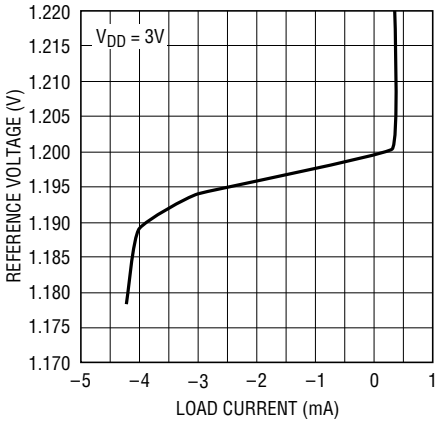
LTC1282 • TPC10

Spurious Free Dynamic Range vs Input Frequency



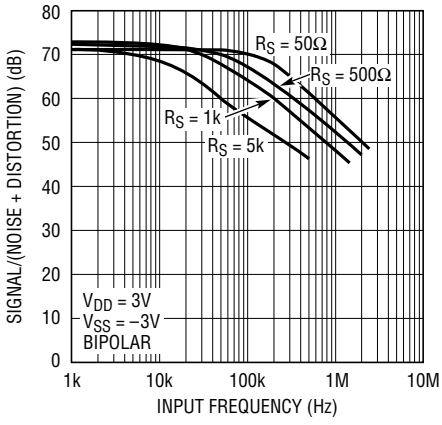
LTC1282 • TPC12

Reference Voltage vs Load Current



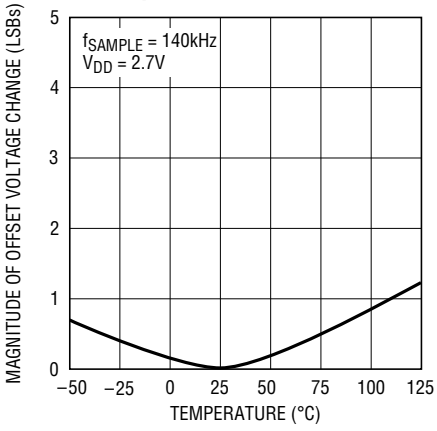
LTC1282 • TPC13

S/(N +D) vs Input Frequency vs Source Resistance (Bipolar)



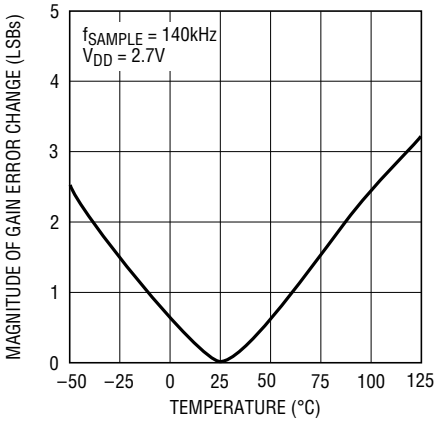
LTC1282 • TPC14

Change in Offset Voltage vs Temperature



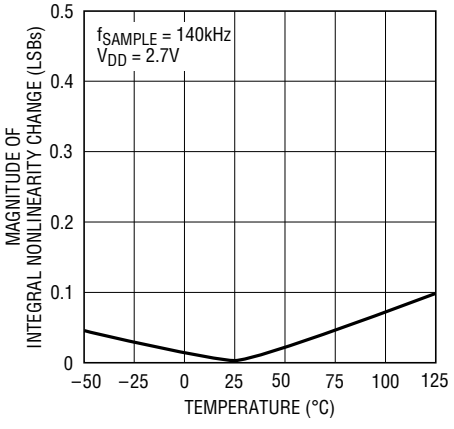
LTC1282 • TPC15

Change in Gain Error vs Temperature



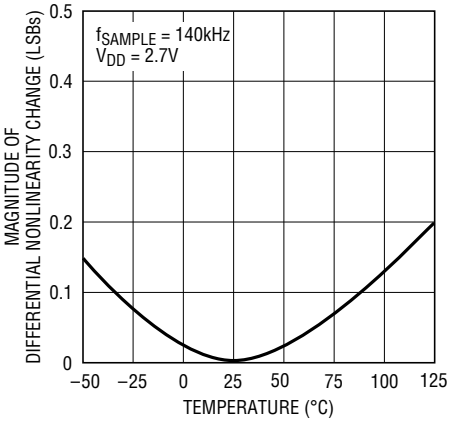
LTC1282 • TPC16

Change in Integral Nonlinearity (INL) vs Temperature



LTC1282 • TPC17

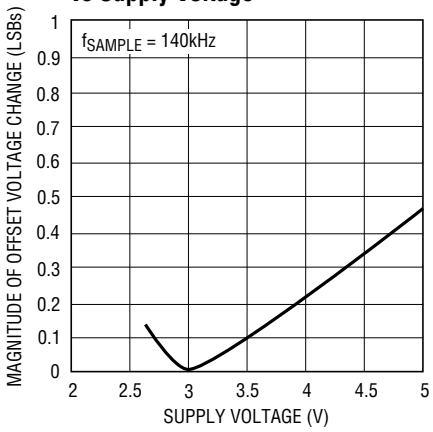
Change in Differential Nonlinearity (DNL) vs Temperature



LTC1282 • TPC18

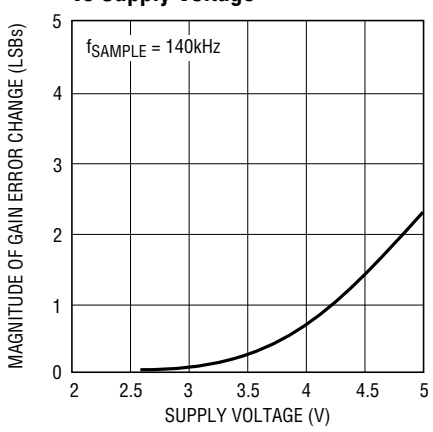
TYPICAL PERFORMANCE CHARACTERISTICS

Change in Offset Voltage vs Supply Voltage



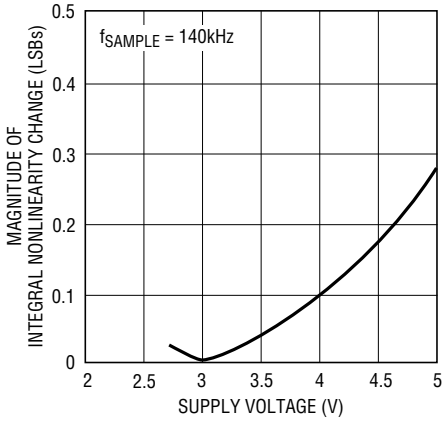
LTC1282 • TPC19

Change in Gain Error vs Supply Voltage



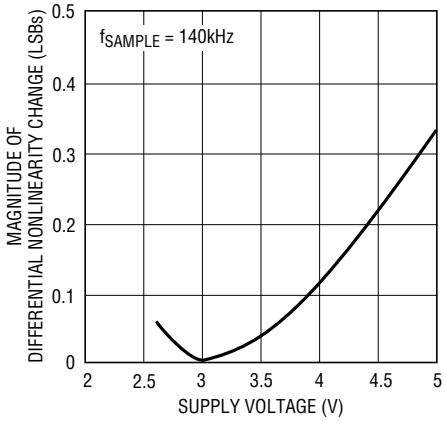
LTC1282 • TPC20

Change in Integral Nonlinearity (INL) vs Supply Current



LTC1282 • TPC21

Change in Differential Nonlinearity (DNL) vs Supply Current



LTC1282 • TPC22

PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 2.5V (Unipolar), ±1.25V (Bipolar).

V_{REF} (Pin 2): +1.20V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11-D4 (Pins 4 to 11): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3/11-D0/8 (Pins 13 to 16): Three-State Data Outputs.

NC (Pins 17 and 18): No Connection.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7 and D0/8). See Table 1. HBEN also disables conversion start when HIGH.

$\overline{RD}$ (Pin 20): READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output shows the converter status. It is low when a conversion is in progress.

V_{SS} (Pin 23): Bipolar Mode — Negative Supply, –3V. Bypass to AGND with 0.1µF ceramic.

Unipolar Mode — Tie to DGND.

V_{DD} (Pin 24): Positive Supply, 3V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

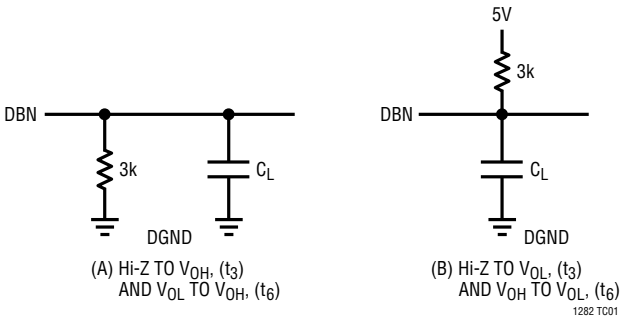
Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

TEST CIRCUITS

Load Circuits for Access Time

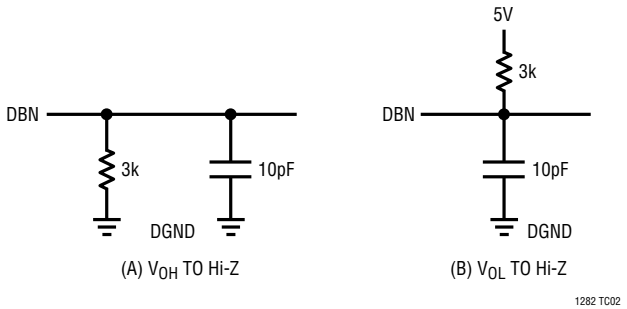


(A) Hi-Z TO V_{OH}, (t_3) AND V_{OL} TO V_{OH}, (t_6)

(B) Hi-Z TO V_{OL}, (t_3) AND V_{OH} TO V_{OL}, (t_6)

1282 TC01

Load Circuits for Output Float Delay

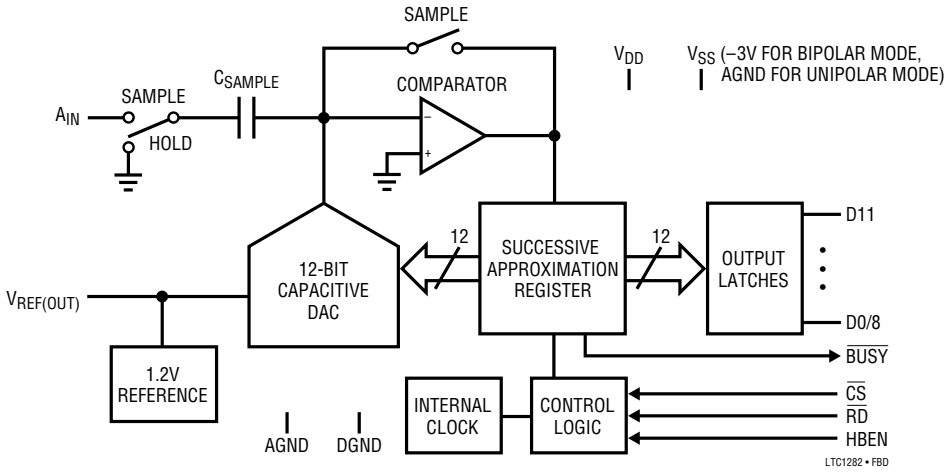


(A) V_{OH} TO Hi-Z

(B) V_{OL} TO Hi-Z

1282 TC02

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1282 uses a successive approximation and an internal sample-and-hold circuitry to convert an analog signal to a 12-bit parallel or 2-byte output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. Please refer to the Digital Interface section for the data format.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the sample phase, and the comparator offset is nulled by the feedback switch. In this sample phase, a minimum delay of 1.14µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge to the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit latch.

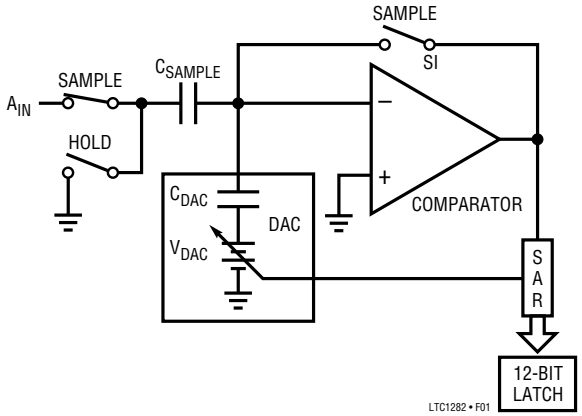


Figure 1. A_{IN} Input

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

The LTC1282 has exceptionally high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1282 FFT plot.

Signal-to-(Noise + Distortion) Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical LTC1282 FFT plot.

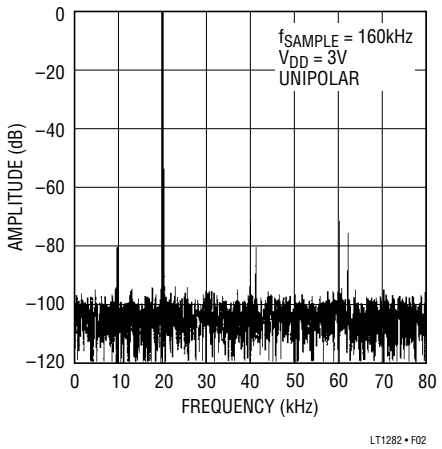


Figure 2. LTC1282 Nonaveraged, 1024 Point FFT Plot

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 140kHz the LTC1282 maintains 11.3 ENOBs at 70kHz input frequency. Refer to Figure 3.

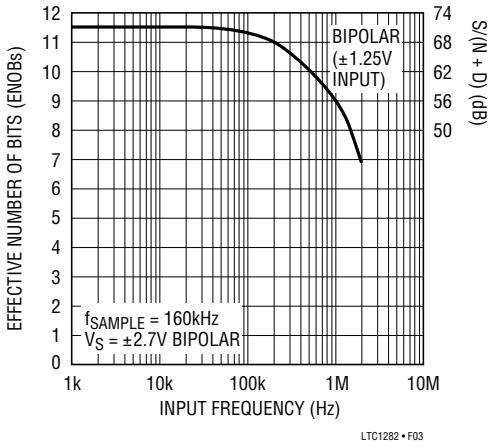


Figure 3. ENOBs and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 70kHz input signal, the LTC1282 has a typical –82dB THD as shown in Figure 4.

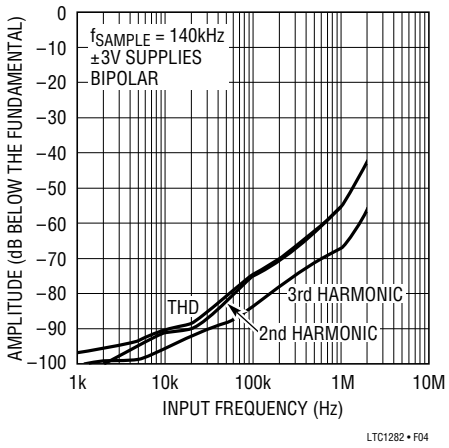


Figure 4. Distortion vs Input Frequency (Bipolar)

APPLICATIONS INFORMATION

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb) if the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order. IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log\frac{Amplitude\ at\ (fa \pm fb)}{Amplitude\ at\ fa}$$

Figure 5 shows the IMD performance at a 20kHz input.

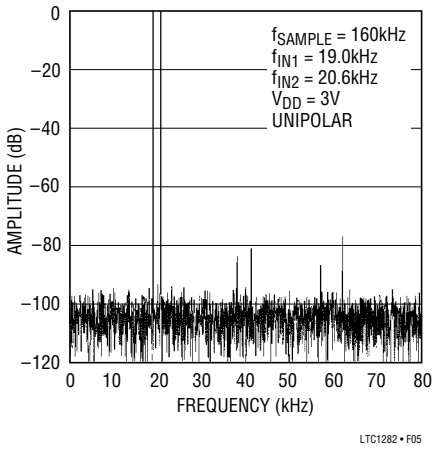


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1282 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency.

Driving the Analog Input

The analog input of the LTC1282 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 1.14µs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT®1190/LT1191, LT1007, LT1220, LT1223 and LT1224 op amps.

The analog input tolerates source resistance very well. Here again, the only requirement is that the analog input must settle before the next conversion starts. For larger source resistance, full accuracy can be obtained if more time is allowed between conversions.

Internal Reference

The LTC1282 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 1.20V. It is internally connected to the DAC and is available at pin 2 to provide up to 0.3mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

APPLICATIONS INFORMATION

Overdriving the Internal Reference

The V_{REF} pin can be driven above its normal value with a DAC or other means to provide input span adjustment. Figure 6 shows an LT1006 op amp driving the reference pin. The V_{REF} pin must be driven to at least 1.25V to prevent conflict with the internal reference. The reference should be driven to no more than 1.44V in unipolar mode or 2.88V for bipolar mode to keep the input span within the single 3V or ±3V supplies.

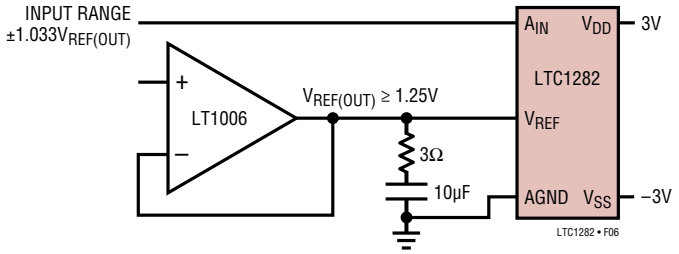


Figure 6. Driving the V_{REF} with the LT1006 Op Amp

Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1282 operating in bipolar mode. This will provide an improved drift (due to the 5ppm/°C of the LT1019A-2.5) and a ±2.604V full scale.

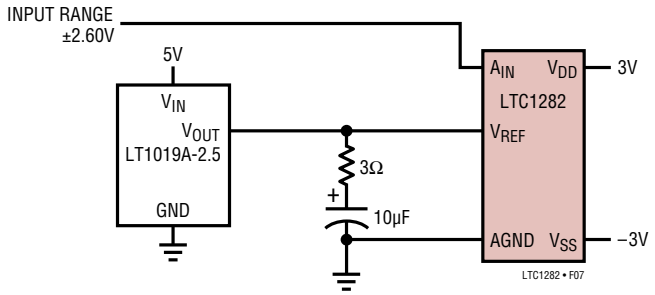


Figure 7. Supplying a 2.5V Reference Voltage to the LTC1282 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1282. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSBs, 2.5LSBs, FS – 1.5LSBs). The output code is natural binary with 1LSB = FS/4096 = 2.5V/4096 = 0.61mV. Figure 9 shows the input/output transfer characteristics for the LTC1282 in bipolar operation. The full scale for LTC1282 in bipolar mode is still 2.5V and 1LSB = 0.61mV.

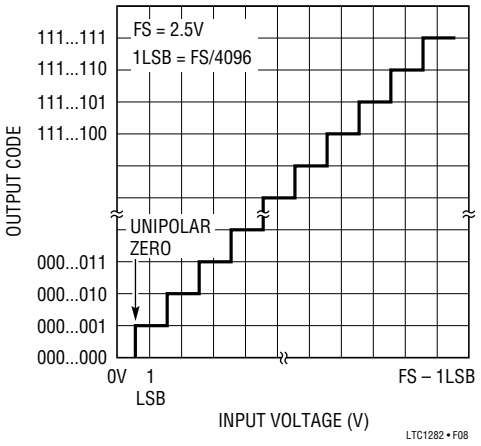


Figure 8. LTC1282 Unipolar Transfer Characteristic

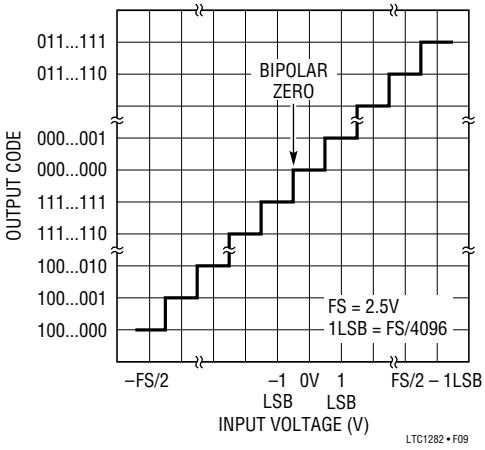


Figure 9. LTC1282 Bipolar Transfer Characteristic

Unipolar Offset and Full-Scale Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Figure 10 shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 11 can be used. Offset should be adjusted before full scale. To adjust offset, apply 0.305mV (i.e., 0.5LSB) at V1 and

APPLICATIONS INFORMATION

adjust the op amp offset voltage until the LTC1282 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 2.49909V (i.e., FS – 1.5LSBs or last code transition) at the input and adjust the full-scale trim until the LTC1282 output code flickers between 1111 1111 1110 and 1111 1111 1111.

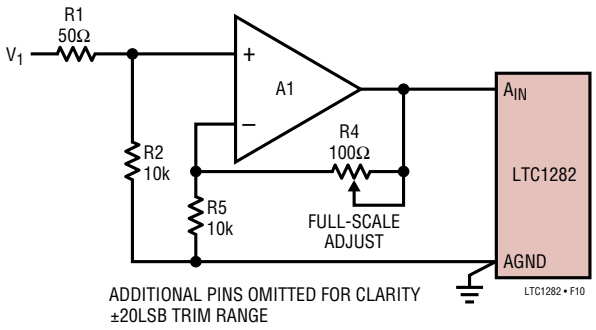


Figure 10. Full-Scale Adjust Circuit

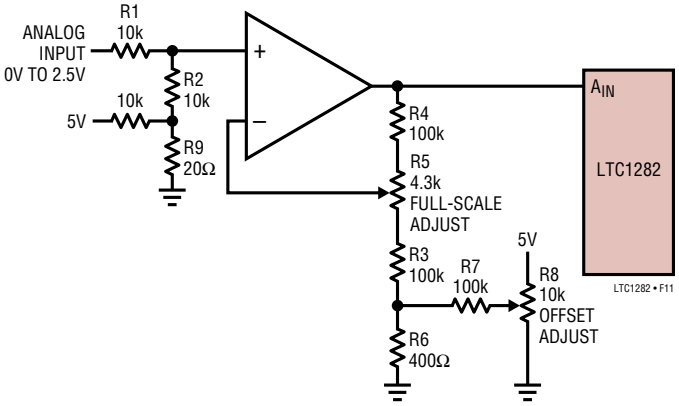


Figure 11. Unipolar Offset and Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Adjustment

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Figure 10 shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 12 can be used. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset

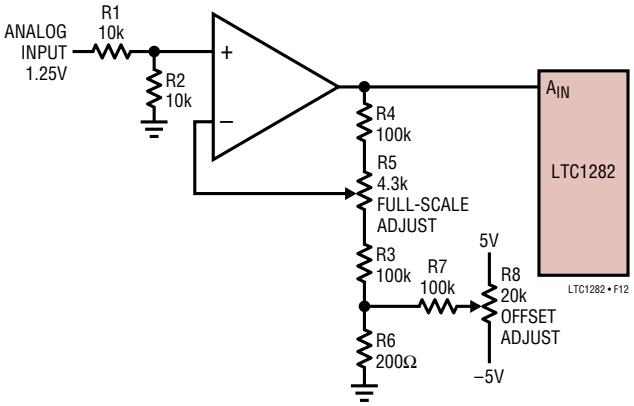


Figure 12. Bipolar Offset and Full-Scale Adjust Circuit

adjustment of Figure 12 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.305mV (–0.5LSB for LTC1282) to the input in Figure 12 and adjusting R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 1.24909V (FS – 1.5LSBs for LTC1282) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

The LTC1282 is easy to use. To obtain the best performance from the device, a printed circuit board is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 13. In bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

APPLICATIONS INFORMATION

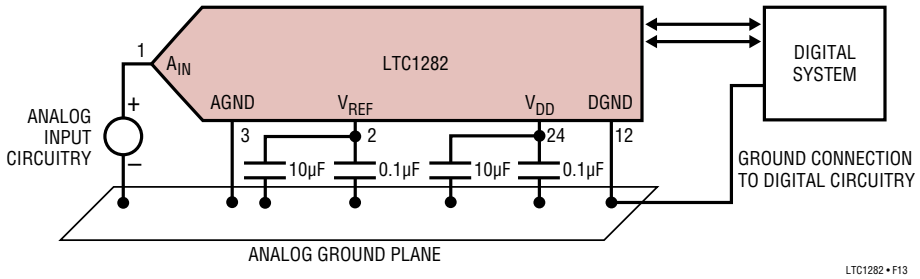


Figure 13. Power Supply Grounding Practice

Noise: Input signal leads to A_{IN} and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the ADC, as shown in Figure 13. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADC is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally either connected to the microprocessor address bus or grounded.

Connecting to 5V Logic Systems

The LTC1282 interfaces well to 5V logic because the ESD clamps on the inputs do not clamp to the positive supply (see Figure 14). Inputs of 0V to 5V do not bother the ADC at all. In addition, the 0V to 3V outputs of the 3V ADC are more than adequate to meet TTL input levels in the 5V logic. (5V logic with CMOS input levels requires a level shift.)

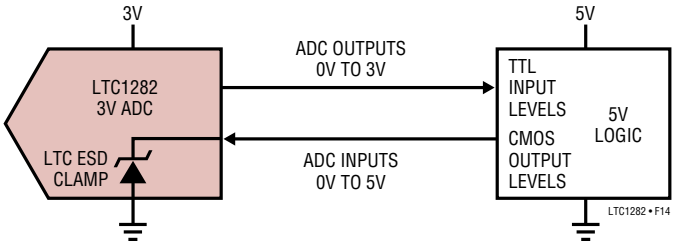


Figure 14. 3V ADC ESD Protection Handles 0V to 5V Swings Easily

APPLICATIONS INFORMATION

Internal Clock

The LTC1282 has an internal clock that eliminates the need for synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 5.5µs, and a maximum conversion time over the full operating temperature range of 6.0µs. No external adjustments are required and, with the guaranteed maximum acquisition time of 1.14µs, throughput performance of 140ksps is assured.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 15 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

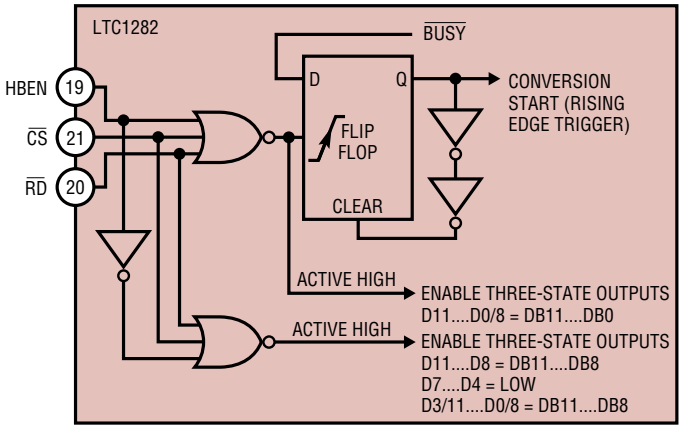


Figure 15. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

There are two modes of operation as outlined by the timing diagrams of Figures 16 to 19. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

Data Format

The output format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7...D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7...D0/8 outputs (4MSBs or 8MSBs) where it can be read in two read cycles. The 4MSBs always appear on D11...D8 whenever the three-state output drivers are turned on.

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 16 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low trigger a conversion and the ADC acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11...D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only 8 data outputs D7...D0/8 are used. Conversion start procedure and data output status for the first read operation are identical to Slow Memory Mode, Parallel Read. See Figure 17 timing diagram and Table 3 data bus status. At the end of the conversion, the low data byte (D7...D0/8) is read from the ADC. A second READ operation with the HBEN high, places the high byte on data outputs D3/11...D0/8 and disables conversion start. Note the 4MSBs appear on data output D11...D8 during the two READ operations.

APPLICATIONS INFORMATION

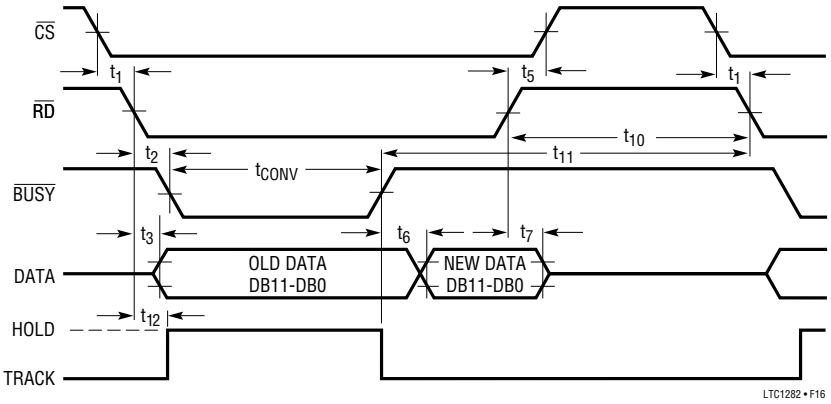


Figure 16. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	Db11	Db10	Db9	Db8	Db7	Db6	Db5	Db4	Db3	Db2	Db1	Db0

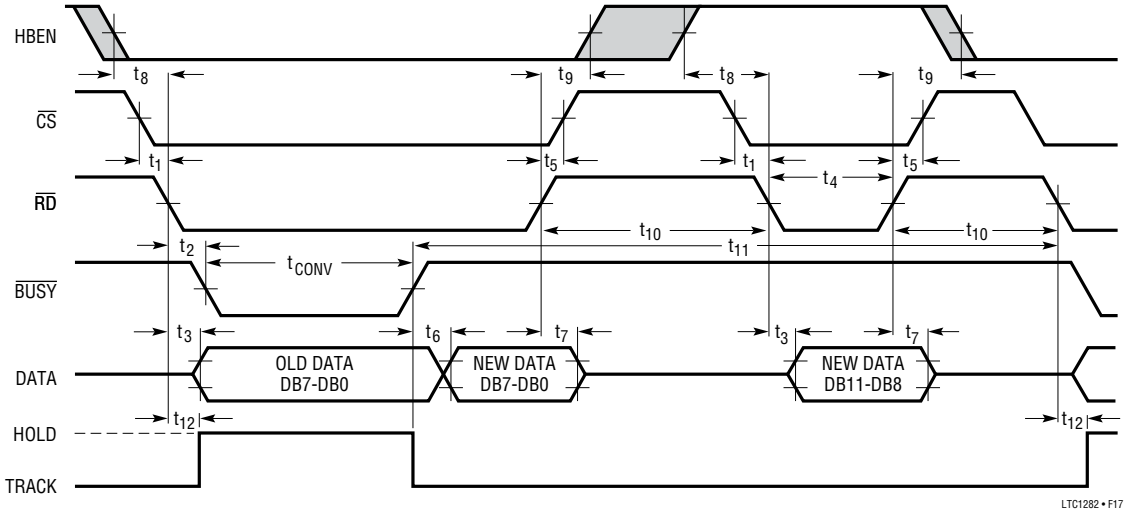


Figure 17. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

APPLICATIONS INFORMATION

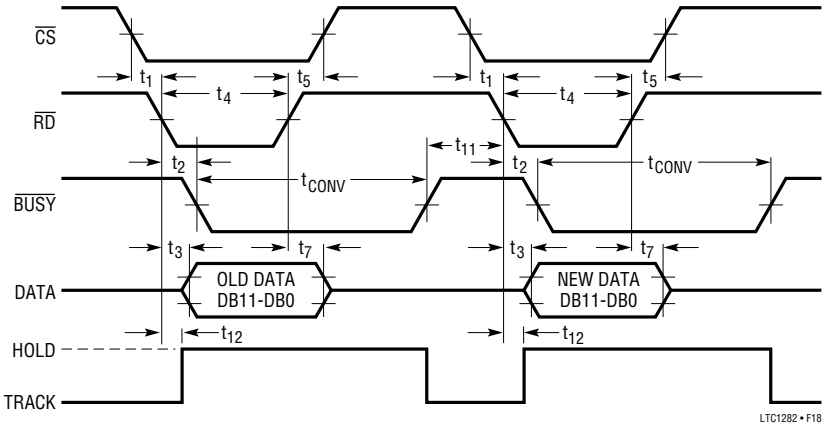


Figure 18. ROM Mode, Parallel Read Timing Diagram (HBEN = LOW)

Table 4. Rom Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	Db11	Db10	Db9	Db8	Db7	Db6	Db5	Db4	Db3	Db2	Db1	Db0
Second Read	Db11	Db10	Db9	Db8	Db7	Db6	Db5	Db4	Db3	Db2	Db1	Db0

ROM Mode, Parallel Read (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a WAIT state. A conversion is started with a READ operation, and the 12 bits of data from the previous conversion are available on data outputs D11...D0/8 (see Figure 18 and Table 4). This data may be disregarded if not required. A second READ operation reads the new data (DB11...DB0) and starts another conversion. A delay at least as long as the ADC's conversion time plus the 1.0µs minimum delay between conversions must be allowed between READ operations.

ROM Mode, Two Byte Read

As previously mentioned for a two byte read, only data outputs D7...D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM mode, Parallel Read (see Figure 19 timing diagram and Table 5 data bus status). Two more READ operations are required to access the new conversion result. A delay equal to the ADC's conversion time must be allowed between conversion start and the second data READ operation. The second READ operation with HBEN high disables conversion start and places the high byte (4MSBs) on data outputs D3/11...D0/8. A third read operation accesses the low data byte (DB7... DB0) and starts another conversion. The 4MSBs appear on data outputs D11...D8 during all three read operations.

MICROPROCESSOR INTERFACING

The LTC1282 allows easy interfacing to digital signal processors as well as modern high speed, 8-bit or 16-bit microprocessors. Here are several examples.

TMS320C25

Figure 20 shows an interface between the LTC1282 and the TMS320C25.

The R/$\overline{W}$ signal of the DSP initiates a conversion and conversion results are read from the LTC1282 using the following instruction:

IN D, PA

APPLICATIONS INFORMATION

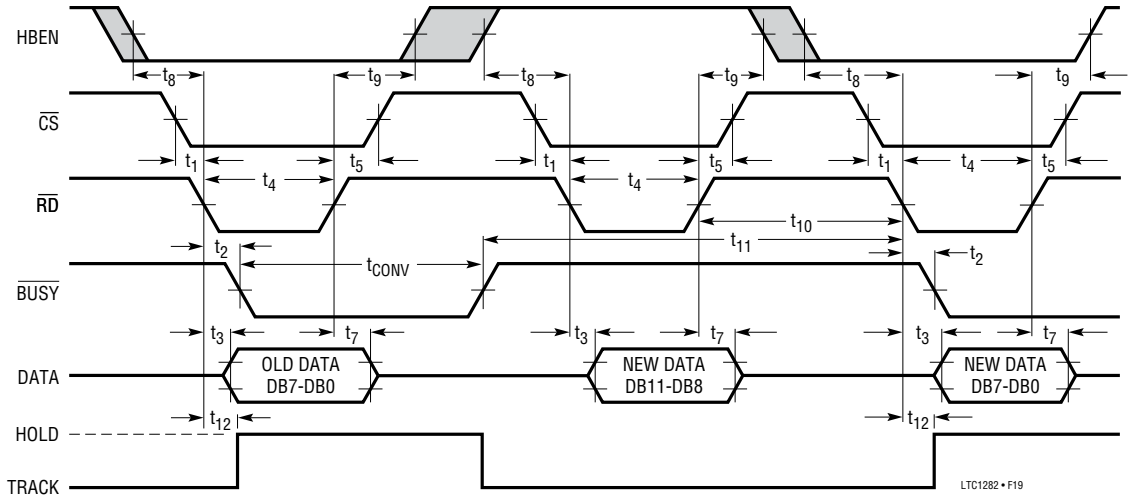


Figure 19. ROM Mode Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read (New Data)	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read (New Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

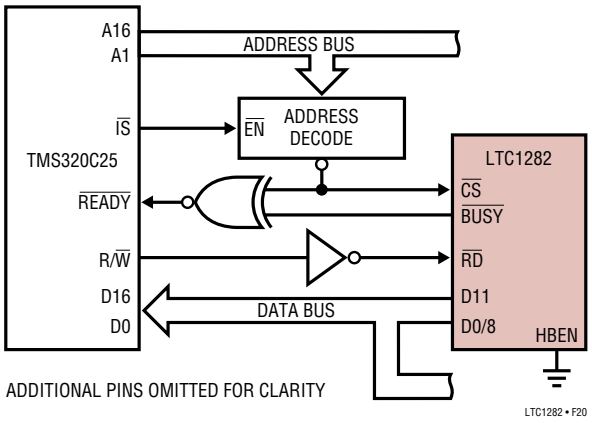


Figure 20. TMS320C25 Interface

where D is Data Memory Address and PA is the PORT ADDRESS.

MC68000 Microprocessor

Figure 21 shows a typical interface for the MC68000. The LTC1282 is operating in the Slow Memory Mode. Assuming the LTC1282 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result:

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$ so that the MC68000 is forced into a WAIT state. At the end of conversion, $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the microprocessor.

APPLICATIONS INFORMATION

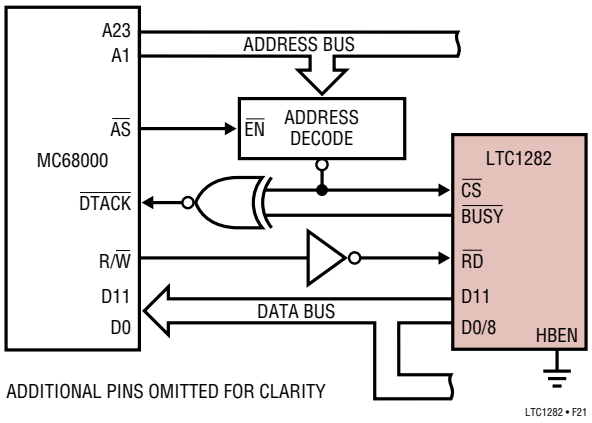


Figure 21. MC68000 Interface

8085A/Z80 Microprocessor

Figure 22 shows an LTC1282 interface for the Z80 and 8085A. The LTC1282 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN so that an even address (HBEN = LOW) to the LTC1282 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A	LHLD (B000)
For the Z80	LDHL, (B000)

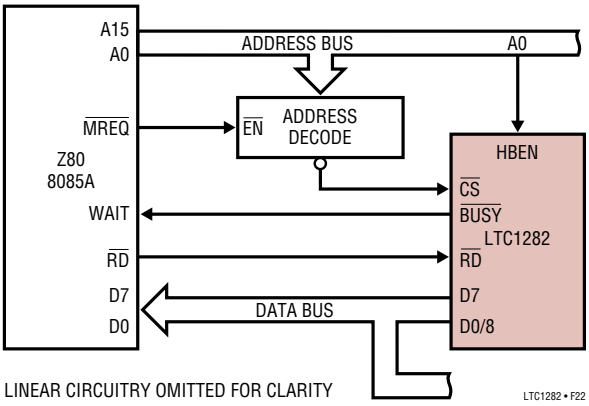


Figure 22. 8085A and Z80 Interface

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the LTC1282 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 23 shows an LTC1282/TMS32010 interface. The LTC1282 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The LTC1282 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

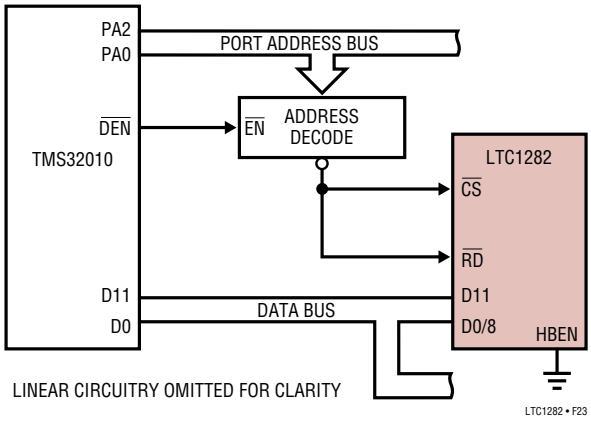


Figure 23. TMS32010 Interface

APPLICATIONS INFORMATION

MUXing with CD4051

The high input impedance of the LTC1282 provides an easy, cheap, fast, and accurate way to multiplex many channels of data through one converter. Figure 24 shows a low cost CD4051, one of the most common multiplexers connected to the LTC1282. The LTC1282's input draws no DC input current so it can be accurately driven by the unbuffered MUX. The CD4520 counter increments the MUX channel after each sample is taken.

100ps Resolution ΔTime Measurement with LTC1282

Figure 25 shows a circuit that precisely measures the difference in time between two events. It has a 400ns full scale and 100ps resolution. The start signal releases the ramp generator made up of the PNP current source and the 500pF capacitor. The circuit ramps until the stop signal shuts off the current source. The final value of the ramp represents the time between the start and stop events. The LTC1282 digitizes this final value and outputs the digital data.

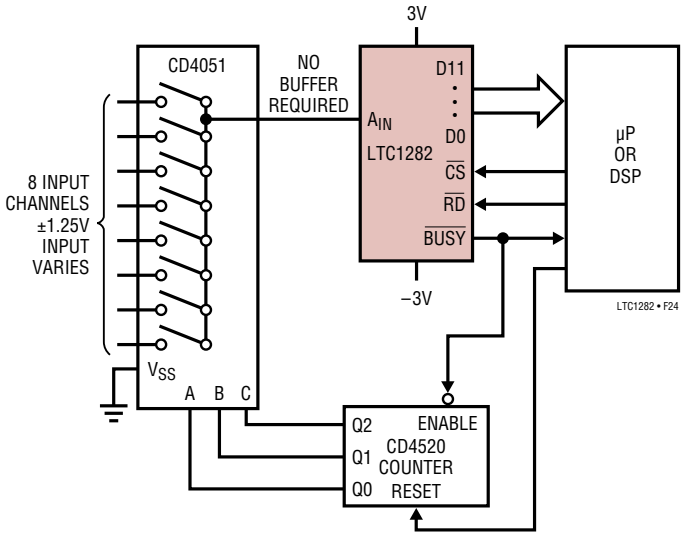


Figure 24. MUXing the LTC1282 with CD4051

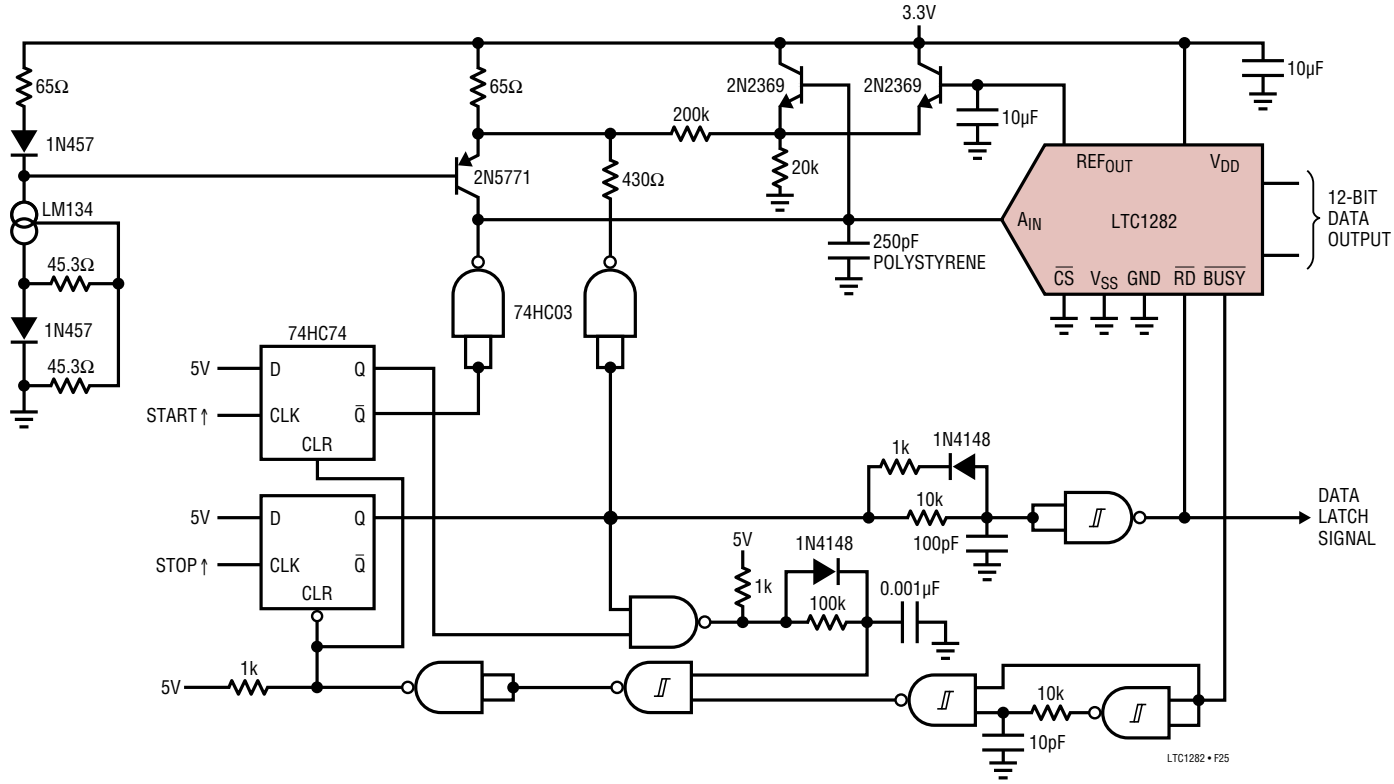


Figure 25. Δ Time Measurement with the LTC1282

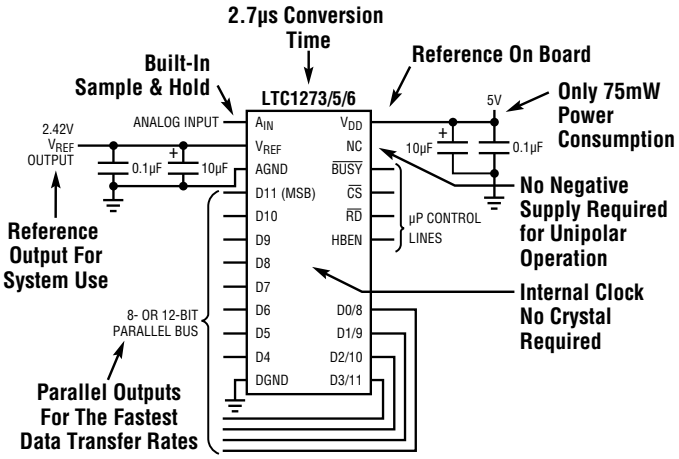
Rev. B

APPLICATIONS INFORMATION

Other High Speed A/D Converters

LTC makes a family of high speed sampling ADCs for a variety of applications. Both single 5V and ±5V supply devices are available at high speeds. The high speed 12-bit family is summarized below.

300ksps and 500ksps 12-Bit Sampling A/D Converters



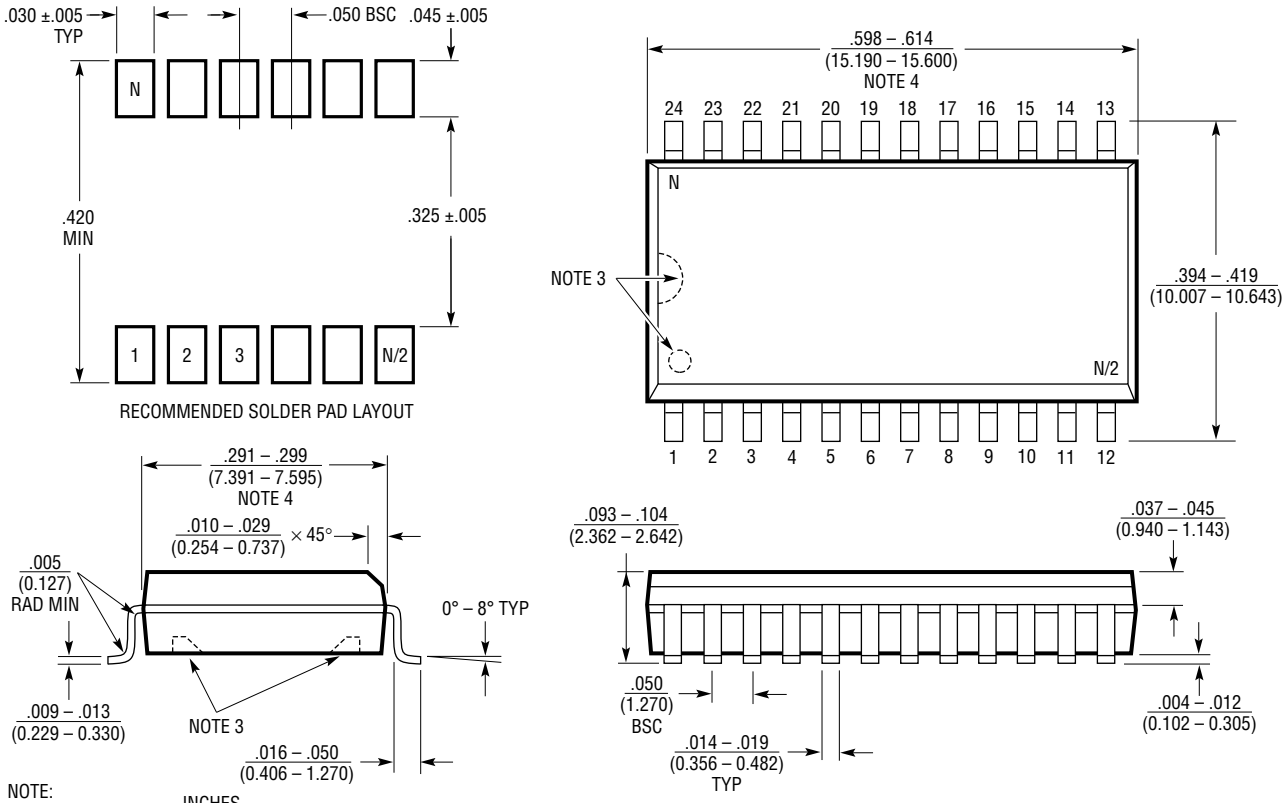
Comparison of Specifications and Features

DEVICE TYPE	SAMPLING FREQ	S/(N + D) @ NYQUIST	INPUT RANGE	POWER SUPPLY	POWER DISSIPATION
LTC1272	250kHz	65dB	0V-5V	5V	75mW
LTC1273	300kHz	70dB	0V-5V	5V	75mW
LTC1275	300kHz	70dB	±2.5V	±5V	75mW
LTC1276	300kHz	70dB	±5V	±5V	75mW
LTC1278	500kHz	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 6mW*
LTC1282	**140kHz**	**68dB**	**0V-2.5V or ±1.25V**	**3V or ±3V**	**12mW**

*6mW power shutdown with instant wake up

PACKAGE DESCRIPTION

SW Package
24-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	09/19	Removed 24-Pin Narrow PDIP package option.	1, 2, 23

RELATED PARTS

PART NUMBER	RESOLUTION	SPEED	COMMENTS
16-Bit			
LTC1604	16	333ksps	±2.5V Input Range, ±5V Supply
LTC1605	16	100ksps	±10V Input Range, Single 5V Supply
14-Bit			
LTC1419	14	800ksps	150mW, 81.5dB SINAD and 95dB SFDR
LTC1416	14	400ksps	75mW, Low Power with Excellent AC Specs
LTC1418	14	200ksps	15mW, Single 5V, Serial/Parallel I/O
12-Bit			
LTC1410	12	1.25Msps	150mW, 71.5dB SINAD and 84dB THD
LTC1415	12	1.25Msps	55mW, Single 5V Supply
LTC1409	12	800ksps	80mW, 71.5dB SINAD and 84dB THD
LTC1279	12	600ksps	60mW, Single 5V or ±5V Supply
LTC1404	12	600ksps	High Speed Serial I/O in SO-8 Package
LTC1278-5	12	500ksps	75mW, Single 5V or ±5V Supply
LTC1278-4	12	400ksps	75mW, Single 5V or ±5V Supply
LTC1400	12	400ksps	High Speed Serial I/O in SO-8 Package