STS4DNF30L

Dual N-channel 30 V, 0.039 Ω, 4 A SO-8 STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max.	I_D
STS4DNF30L	30 V	< 0.050 Ω	4 A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

Applications

Switching application

Description

The STS4DNF60L is a dual N-channel STripFET™ Power MOSFET realized with the second generation of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.
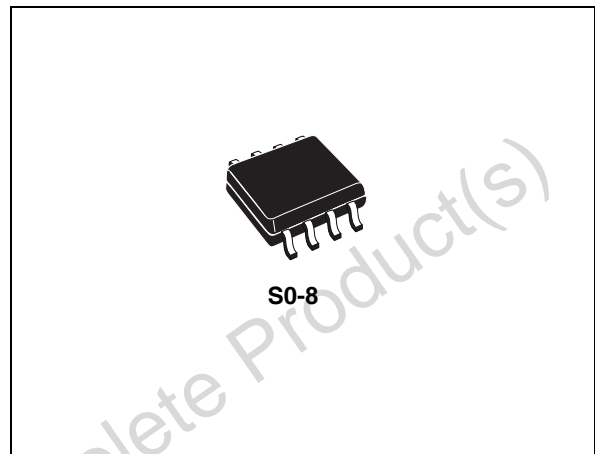

SO-8
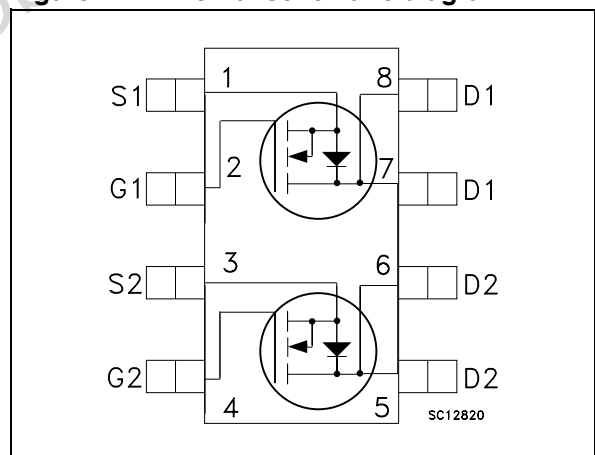
Figure 1. Internal schematic diagram

SC12820

Table 1. Device summary

Order code	Marking	Package	Packaging
STS4DNF30L	4DF30L	SO-8	Tape and reel

Contents

1   Electrical ratings

Table 2.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{gs} = 0$)	30	V
V_{GS}	Gate- source voltage	±16	V
I_D	Drain current (continuos) at $T_C = 25°C$	4	A
I_D	Drain current (continuos) at $T_C = 100°C$	2.5	A
I_{DM} [1]	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at $T_C = 25°C$ dual operating	2	W

1.   Pulse width limited by safe operating area

Table 3.   Thermal data

Symbol	Parameter	Value	Unit
R_{thj-a} [1]	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Junction temperature	- 55 to 150	°C
T_{stg}	Storage temperature range	150	°C

1.   Mounted on FR-4 board (t ≤ 10 sec)

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4.   On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating			1	µA
		V_{DS}= Max rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2 A		0.039	0.050	Ω
		V_{GS} = 4.5 V, I_D = 2 A		0.046	0.060	Ω

Table 5.   Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	330		pF
C_{oss}	Output capacitance			90		pF
C_{rss}	Reverse transfer capacitance			40		pF
Q_g	Total gate charge	V_{DD} = 24 V, I_D = 4 A, V_{GS} = 10 V	-	6.5	9	nC
Q_{gs}	Gate-source charge			3.6		nC
Q_{gd}	Gate-drain charge			2		nC

Table 6.   Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 4.5 V (see *Figure 13*)	-	11 100	-	ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=15 V, I_D=2 A, R_G=4.7 Ω, V_{GS}= 4.5 V (see *Figure 13*)	-	25 22	-	ns ns

Table 7.   Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} [1]	Source-drain current Source-drain current (pulsed)		-		4 16	A A
V_{SD} [2]	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0	-		1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4 A, V_{DD} = 20 V di/dt = 100 A/μs, T_j = 150 °C (see *Figure 15*)	-	30 18 1.2		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

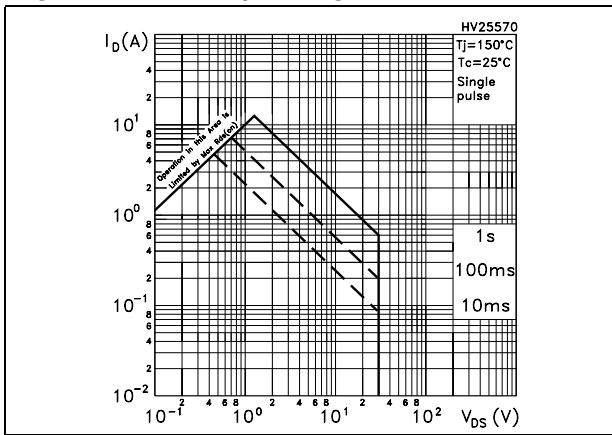## 2.1 Electrical characteristics (curves)

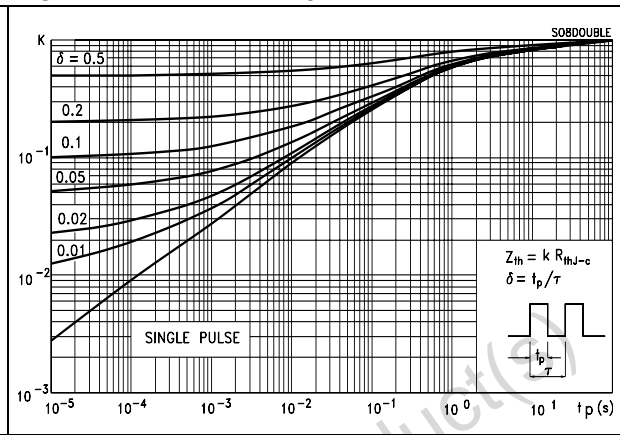**Figure 2. Safe operating area**

Figure 3. Thermal impedance
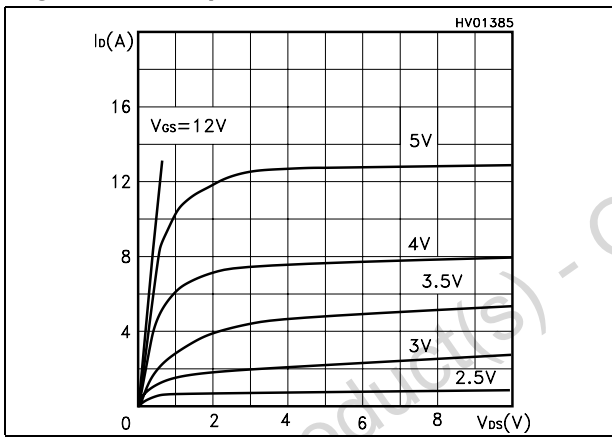

Figure 4. Output characterisics

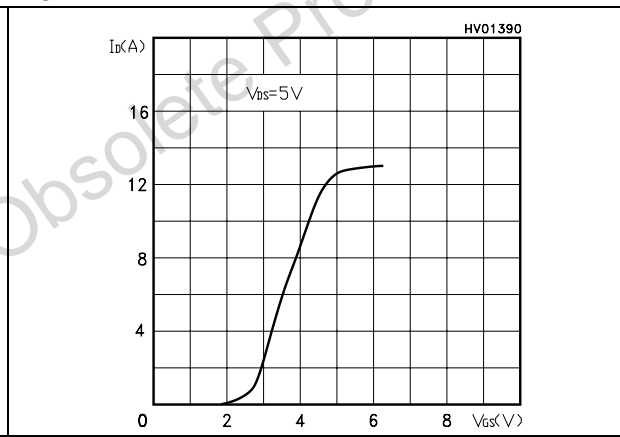**Figure 5. Transfer characteristics**

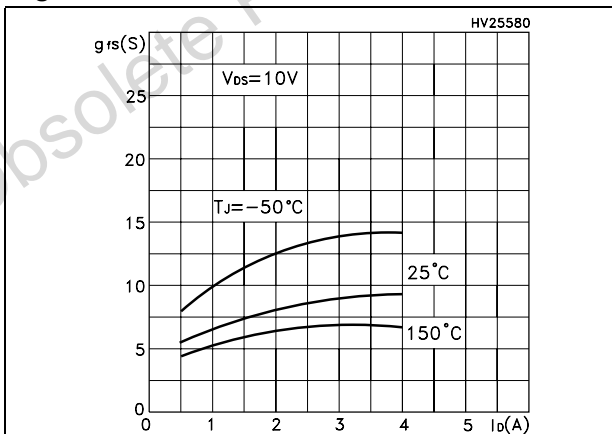**Figure 6. Transconductance**

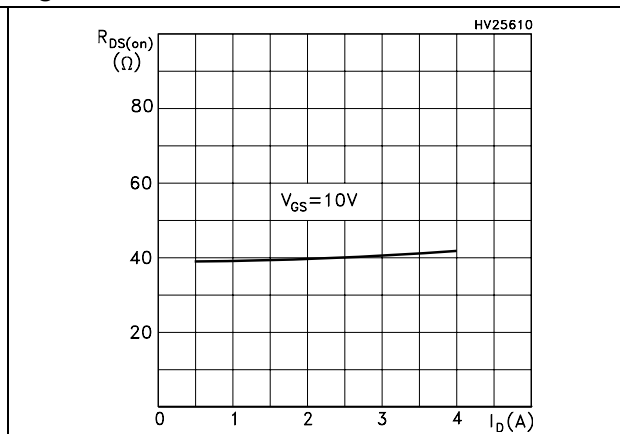**Figure 7. Static drain-source on resistance**

Figure 8.   Gate charge vs gate-source voltage

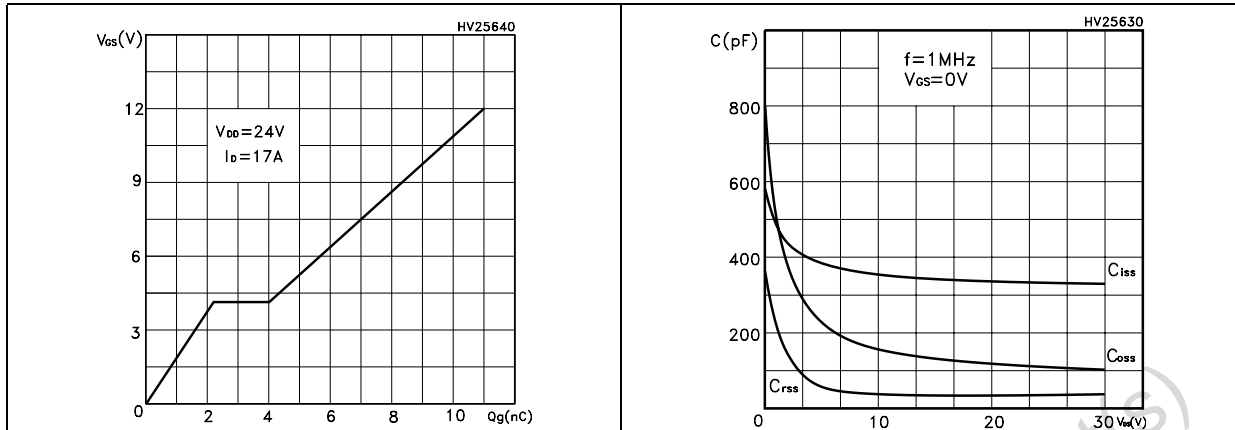**Figure 9.   Capacitance variations**

Figure 10.   Normalized gate threshold voltage vs temperature

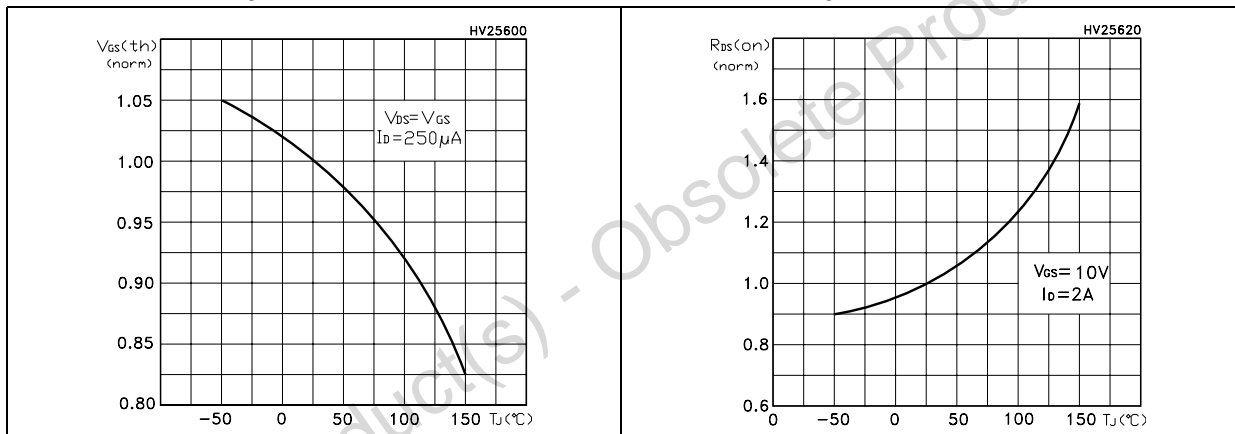**Figure 11.   Normalized on resistance vs temperature**
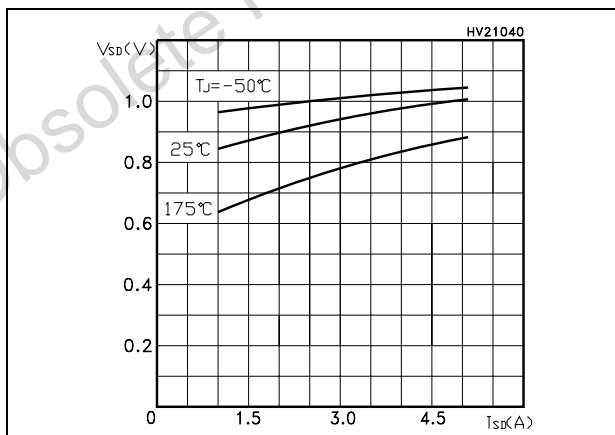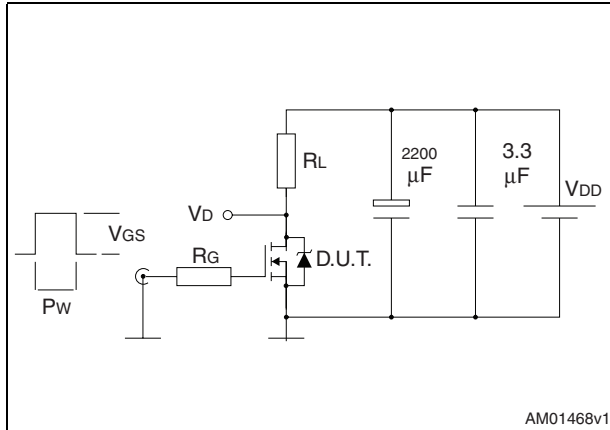
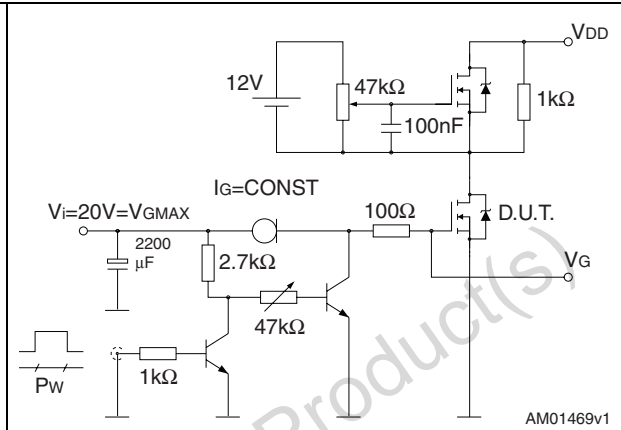

Figure 12.   Source-drain diode forward characteristics

3   Test circuits

Figure 13.   Switching times test circuit for resistive load

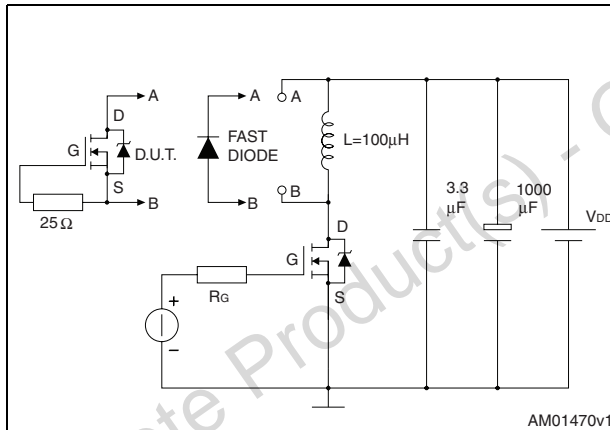**Figure 14.   Gate charge test circuit**

Figure 15.   Test circuit for inductive load switching and diode recovery times

Figure 16.   Unclamped Inductive load test circuit

Figure 17.   Unclamped inductive waveform

Figure 18.   Switching time waveform

4 Package mechanical data

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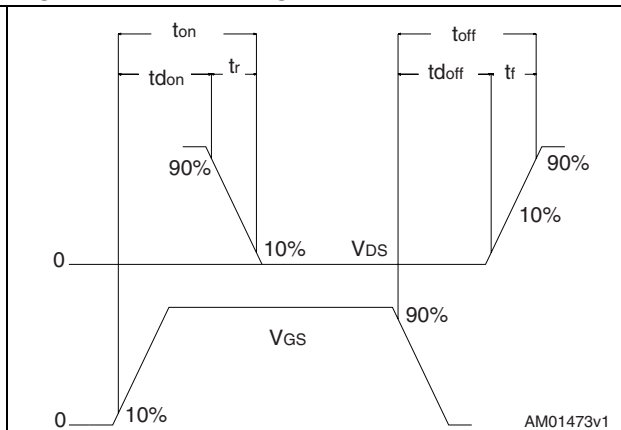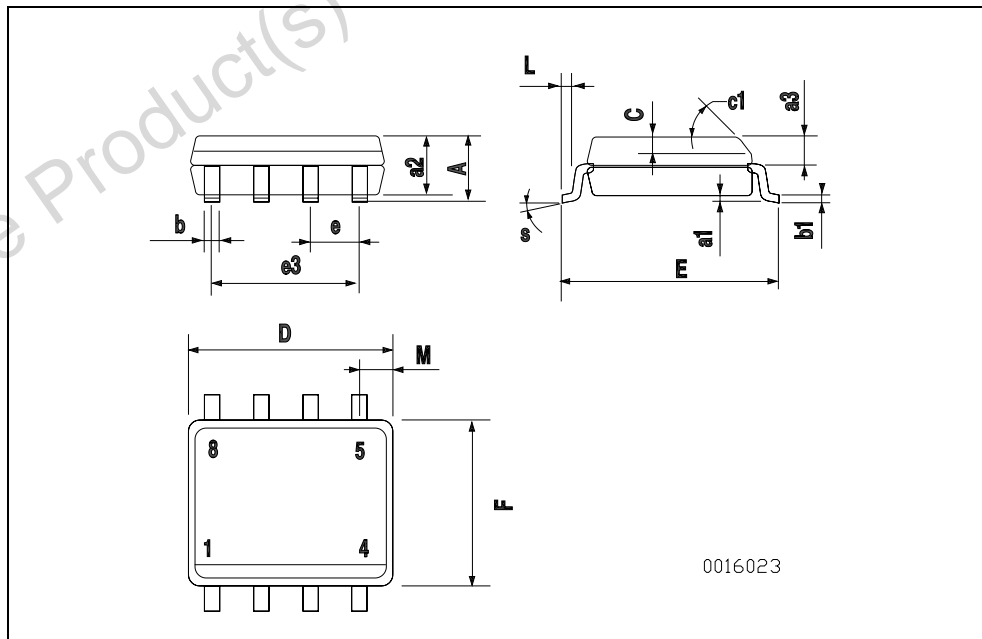| DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					

Title row: **SO-8 MECHANICAL DATA**

0016023

5 Revision history

Table 8.   Revision history

Date	Revision	Changes
11-Sep-2006	1	First version
15-Nov-2006	2	The document has been reformated
17-Jun-2010	3	Marking in *Table 1: Device summary* has been corrected

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