Motion SPM® 3 Series

FSBB30CH60C

General Description

FSBB30CH60C is an advanced Motion SPM 3 module providing a fully−featured, high−performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts, over−current shutdown, and fault reporting. The built−in, high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to the high−voltage, high−current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- 600 V − 30 A 3−Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low−Loss, Short−Circuit Rated IGBTs
- Very Low Thermal Resistance Using AlN DBC Substrate
- Built−in Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open−Emitter Pins from Low−Side IGBTs for Three−Phase Current Sensing
- Single−Grounded Power Supply
- Isolation Rating of 2500 Vrms/min.
- This is a Pb−Free Device

Applications

- Motion Control − Home Appliance / Industrial Motor

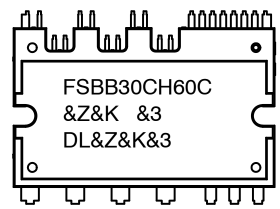
Related Resources

- AN−9044 Motion SPM® 3 Series Users Guide

3D Package Drawing
(Click to Activate 3D Content)

SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE
CASE MODFJ

MARKING DIAGRAM



&Z	= Assembly Plant Code
&K	= 2−Digits Lot Run Traceability Code
&3	= 3−Digit Date Code
FSBB30CH60C	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Integrated Power Functions

- 600 V − 30 A IGBT Inverter for Three−Phase DC/AC Power Conversion (Please Refer to Figure 2)

Integrated Drive, Protection and System Control Functions

- For Inverter High−Side IGBTs:
  Gate drive circuit, High voltage isolated high − speed level shifting Control circuit under−voltage Lock−Out Protection (UVLO)
  Note: Available bootstrap circuit example is given in Figures 11 and 12.
- For Inverter Low−side IGBTs:
  Gate drive circuit, Short−Circuit Protection (SCP) control supply circuit Under−Voltage Lock−Out Protection (UVLO)
- Fault Signaling:
  Corresponding to UVLO (low−side supply) and SC faults
- Input Interface:
  Active−HIGH interface, works with 3.3 / 5 V logic, Schmitt−trigger input

Pin Configuration

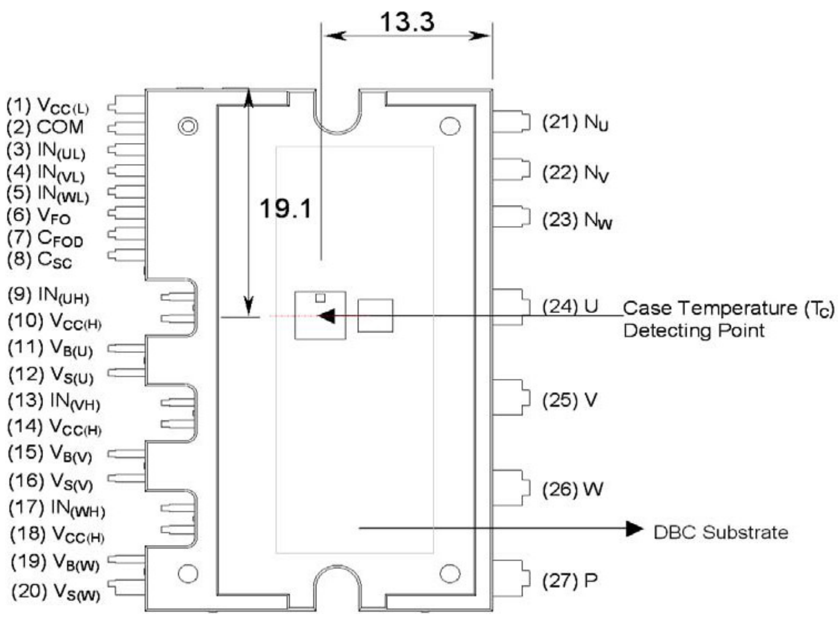
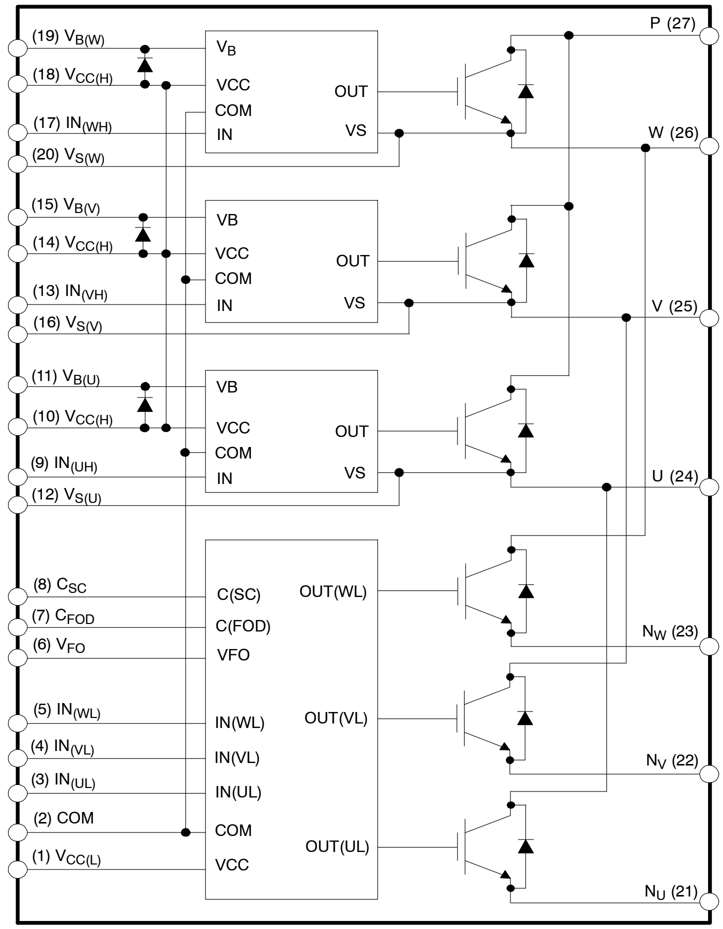


Figure 1. Pin Configuration (Top View)

PIN DESCRIPTION

Pin No.	Symbol	Description
1	$V_{CC(L)}$	Low−Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low−Side U−Phase
4	$IN_{(VL)}$	Signal Input for Low−Side V−Phase
5	$IN_{(WL)}$	Signal Input for Low−Side W−Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low−Pass Filter) for Short−Circuit Current Detection Input
9	$IN_{(UH)}$	Signal Input for High−Side U−Phase
10	$V_{CC(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
11	$V_{B(U)}$	High−Side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High−Side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High−Side V Phase
14	$V_{CC(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
15	$V_{B(V)}$	High−Side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High−Side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High−Side W Phase
18	$V_{CC(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
19	$V_{B(W)}$	High−Side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High−Side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC−Link Input for U−Phase
22	N_V	Negative DC−Link Input for V−Phase
23	N_W	Negative DC−Link Input for W−Phase
24	U	Output for U−Phase
25	V	Output for V−Phase
26	W	Output for W−Phase
27	P	Positive DC−Link Input

Internal Equivalent Circuit and Input/Output Pins



NOTES:

1. Inverter low−side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.
3. Inverter high−side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Condition	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P − N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P − N_U, N_V, N_W	500	V
V_{CES}	Collector − Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C, T_J ≤ 150°C	30	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, T_J ≤ 150°C, under 1 ms pulse width	60	A
P_C	Collector Dissipation	T_C = 25°C per chip	106	W
T_J	Operating Junction Temperature	(Note 4)	−40 ~ 150	°C
CONTROL PART				
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ − COM	20	V
V_{BS}	High−Side Control Bias Voltage	Applied between $V_{B(U)}$ − $V_{S(U)}$, $V_{B(V)}$ − $V_{S(V)}$, $V_{B(W)}$ − $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ − COM	−0.3 ~ V_{CC} + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} − COM	−0.3 ~ V_{CC} + 0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	5	mA
V_{SC}	Current−Sensing Input Voltage	Applied between C_{SC} − COM	−0.3 ~ V_{CC} + 0.3	V
BOOTSTRAP DIODE PART				
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C = 25°C, T_J ≤ 150°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, T_J ≤ 150°C, under 1 ms pulse width	2.0	A
T_J	Operating Junction Temperature		−40 ~ 150	°C
TOTAL SYSTEM				
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	V_{CC} = V_{BS} = 13.5 ~ 16.5 V, T_J = 150°C, non−repetitive, less than 2 μs	600	V
T_C	Module Case Operation Temperature	−40°C ≤ T_J ≤ 150°C, see Figure 1	−40 ~ 125	°C
T_{STG}	Storage Temperature		−40 ~ 125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, connect pins to heat sink plate	2500	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. The maximum junction temperature rating of the power chips integrated within the Motion SPM 3 product is 150°C (@T_C ≤ 125°C).

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part (per 1/6 module)	−	−	1.17	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	−	−	1.87	°C/W

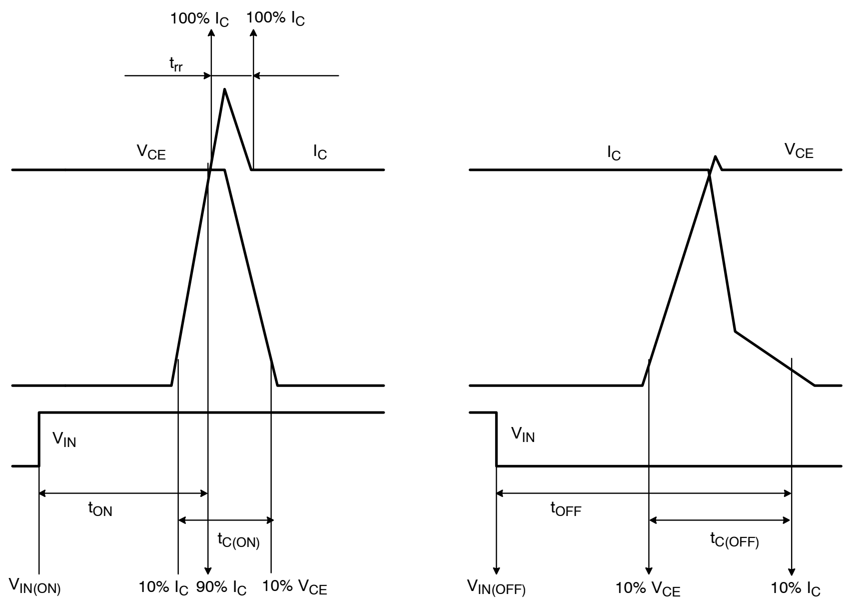
5. For the measurement point of case temperature (T_C), please refer to Figure 1.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol		Parameter	Test Condition		Min	Typ	Max	Unit
INVERTER PART								
$V_{CE(SAT)}$		Collector − Emitter Saturation Voltage	V_{CC} = V_{BS} = 15 V, V_{IN} = 5 V	I_C = 20 A, T_J = 25°C	–	–	2.0	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V	I_F = 20 A, T_J = 25°C	–	–	2.1	V
HS	t_{ON}	Switching Times	V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_C = 30 A, V_{IN} = 0 V ↔ 5 V, Inductive load (Note 6)		–	0.75	–	μs
	$t_{C(ON)}$				–	0.2	–	μs
	t_{OFF}				–	0.4	–	μs
	$t_{C(OFF)}$				–	0.1	–	μs
	t_{rr}				–	0.1	–	μs
LS	t_{ON}		V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_C = 30 A, V_{IN} = 0 V ↔ 5 V, Inductive load (Note 6)		–	0.55	–	μs
	$t_{C(ON)}$				–	0.35	–	μs
	t_{OFF}				–	0.4	–	μs
	$t_{C(OFF)}$				–	0.1	–	μs
	t_{rr}				–	0.1	–	μs
I_{CES}		Collector − Emitter Leakage Current	V_{CE} = V_{CES}		–	–	1	mA
CONTROL PART								
I_{QCCL}		Quiescent V_{CC} Supply Current	V_{CC} = 15 V, $IN_{(UL, VL, WL)}$ = 0 V	$V_{CC(L)}$ − COM	–	–	23	mA
I_{QCCH}			V_{CC} = 15 V, $IN_{(UH, VH, WH)}$ = 0 V	$V_{CC(H)}$ − COM	–	–	600	μA
I_{QBS}		Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH, VH, WH)}$ = 0 V	$V_{B(U)}$ − $V_{S(U)}$, $V_{B(V)}$ − $V_{S(V)}$, $V_{B(W)}$ − $V_{S(W)}$	–	–	500	μA
V_{FOH}		Fault Output Voltage	V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		4.5	–	–	V
V_{FOL}			V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		–	–	0.8	V
$V_{SC(ref)}$		Short Circuit Current Trip Level	V_{CC} = 15 V (Note 7)		0.45	0.5	0.55	V
TSD		Over−Temperature Protection	Temperature at LVIC		–	160	–	°C
ΔTSD		Over−Temperature Protection Hysteresis	Temperature at LVIC		–	5	–	°C
UV_{CCD}		Supply Circuit Under−Voltage Protection	Detection Level		10.7	11.9	13.0	V
UV_{CCR}			Reset Level		11.2	12.4	13.4	V
UV_{BSD}			Detection Level		10	11	12	V
UV_{BSR}			Reset Level		10.5	11.5	12.5	V
t_{FOD}		Fault−Out Pulse Width	C_{FOD} = 33 nF (Note 8)		1.0	1.8	–	ms
$V_{IN(ON)}$		ON Threshold Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ − COM		2.8	–	–	V
$V_{IN(OFF)}$		OFF Threshold Voltage			–	–	0.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 3.
7. Short−circuit current protection is functioning only at the low−sides.
8. The fault−out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation: $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$ [F]



(a) turn−on **(b) turn−off**

Figure 3. Switching Time Definition

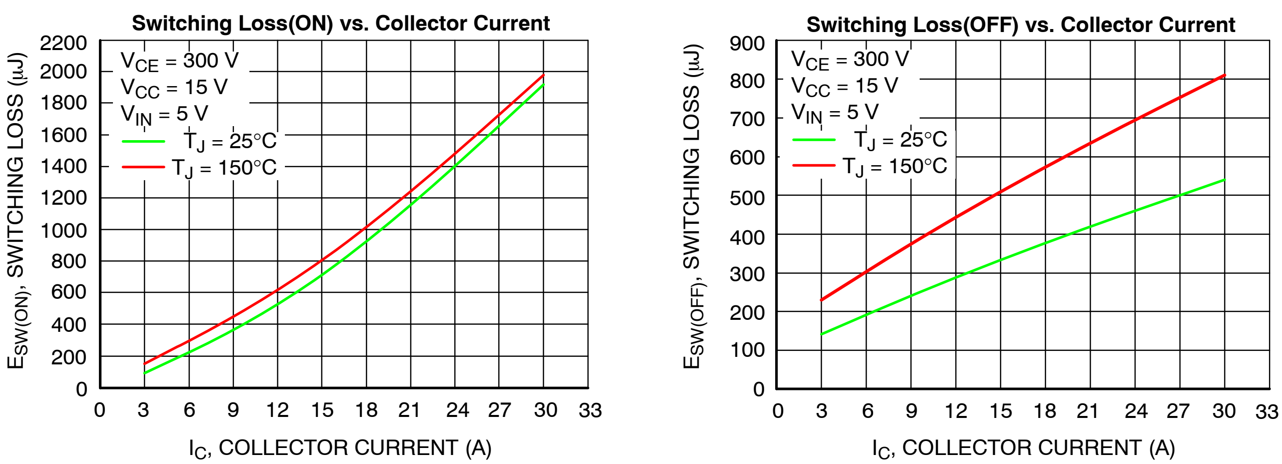
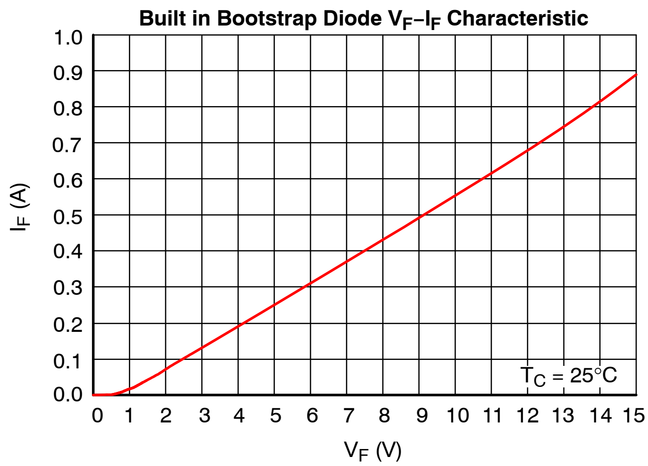


Figure 4. Switching Loss Characteristics

BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_F	Forward Voltage	I_F = 0.1 A, T_C = 25°C	–	2.5	–	V
t_{rr}	Reverse−Recovery Time	I_F = 0.1 A, T_C = 25°C	–	80	–	ns



NOTE:
9. Built−in bootstrap diode includes around 15 Ω resistance characteristic.

Figure 5. Built in Bootstrap Diode Characteristics

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	–	300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ – COM	13.5	15	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		−1	–	1	V/μs
t_{dead}	Blanking Time for Preventing Arm−Short	For Each Input Signal	2	–	–	μs
f_{PWM}	PWM Input Signal	−40°C ≤ T_C ≤ 125°C, −40°C ≤ T_J ≤ 150°C	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including surge voltage)	−4	–	4	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Min	Typ	Max	Unit
Mounting Torque	Mounting Screw: M3	Recommended 0.62 N•m	0.51	0.62	0.80	N•m
Device Flatness		Note Figure 6	0	–	+120	μm
Weight			–	15.00	–	g

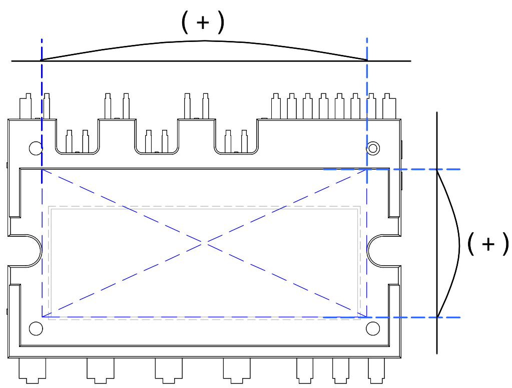
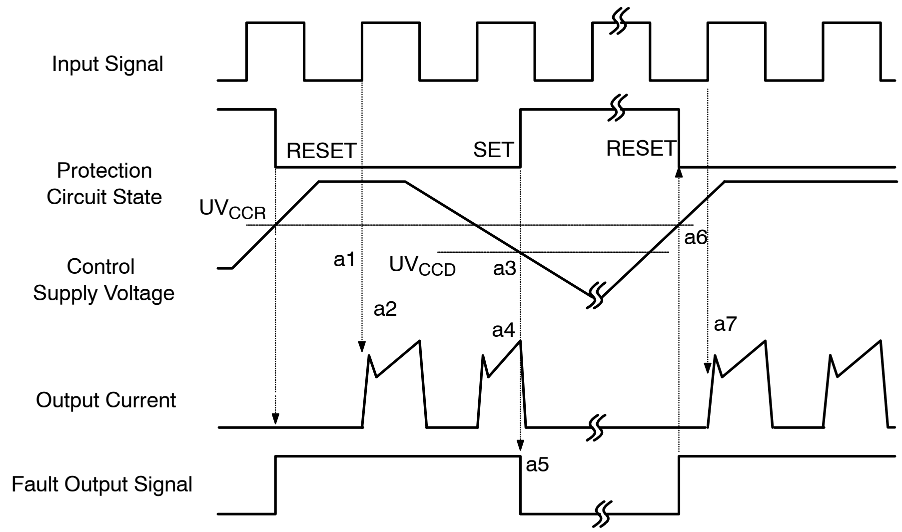


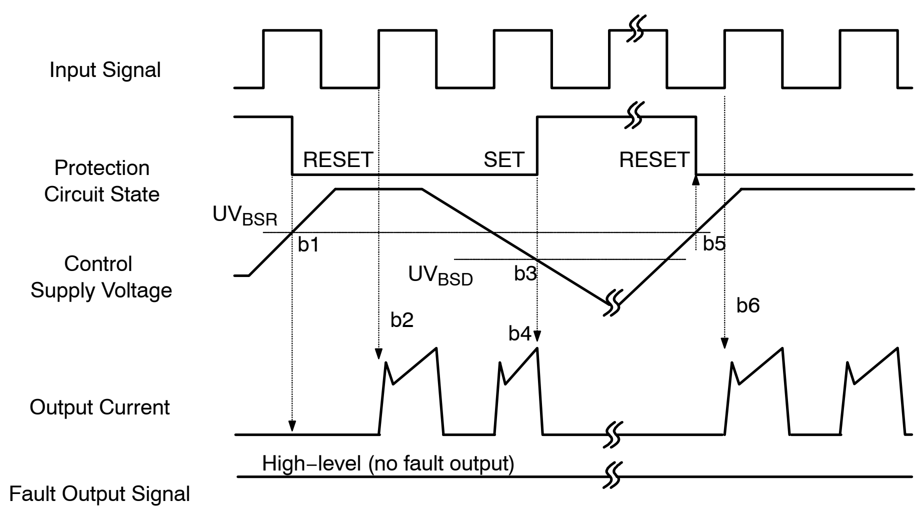
Figure 6. Flatness Measurement Position

Time Charts of Protective Function



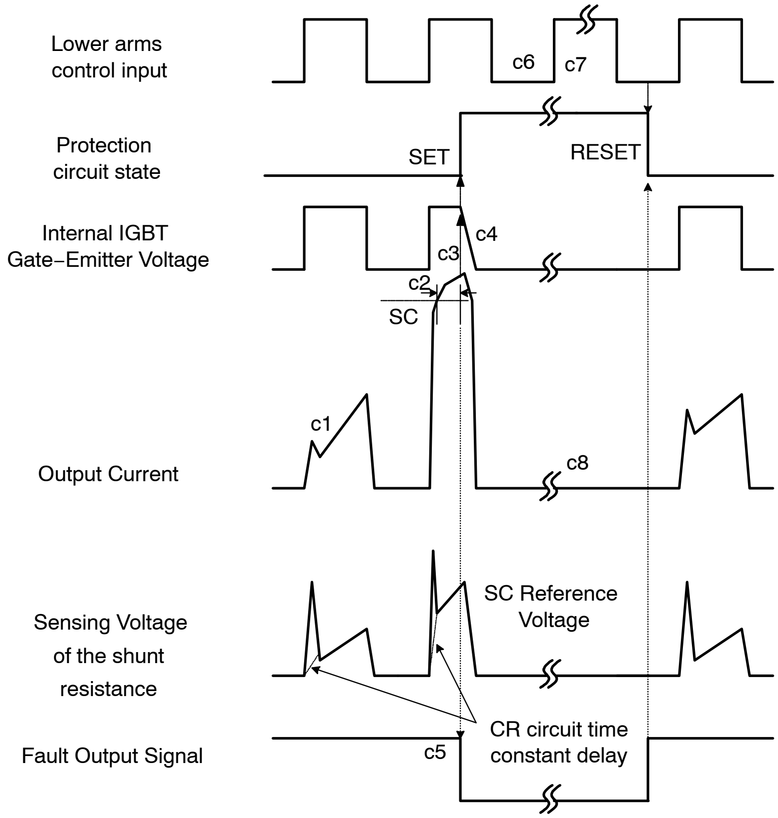
a1: Control supply voltage rises: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.
a2: Normal operation: IGBT ON and carrying current.
a3: Under voltage detection (UV_{CCD}).
a4: IGBT OFF in spite of control input condition.
a5: Fault output operation starts.
a6: Under voltage reset (UV_{CCR}).
a7: Normal operation: IGBT ON and carrying current.

Figure 7. Under−Voltage Protection (Low−Side)



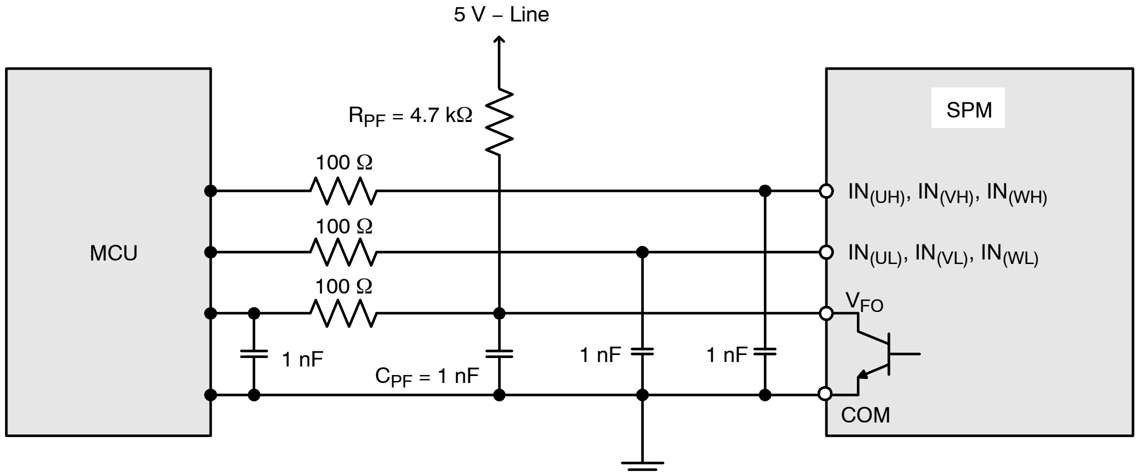
b1: Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.
b2: Normal operation: IGBT ON and carrying current.
b3: Under−voltage detection (UV_{BSD}).
b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
b5: Under−voltage reset (UV_{BSR}).
b6: Normal operation: IGBT ON and carrying current.

Figure 8. Under−Voltage Protection (High−Side)



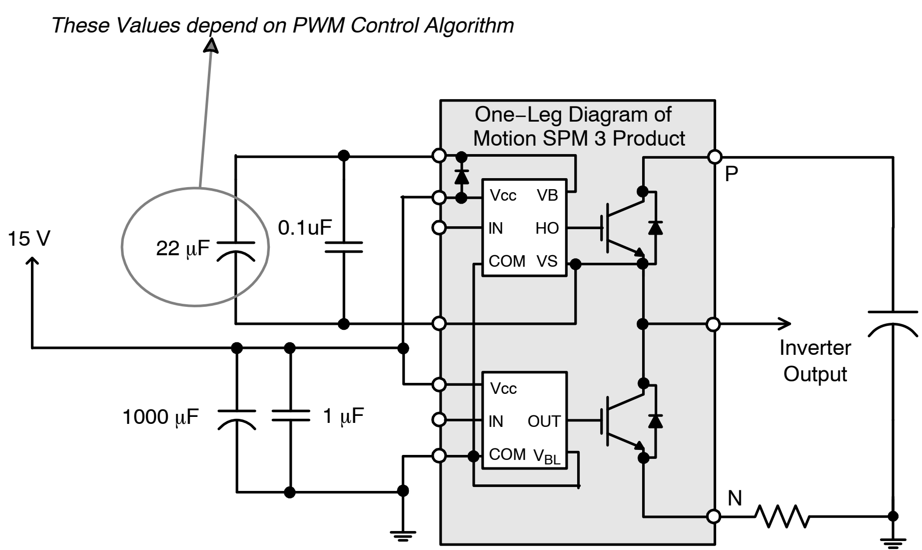
(with the external shunt resistance and CR connection)
c1: Normal operation: IGBT ON and carrying current.
c2: Short−circuit current detection (SC trigger).
c3: Hard IGBT gate interrupt.
c4: IGBT turns OFF.
c5: Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor C_{FO}.
c6: Input “LOW” : IGBT OFF state.
c7: Input “HIGH”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
c8: IGBT OFF state.

Figure 9. Short−Circuit Protection (Low−Side Operation only)



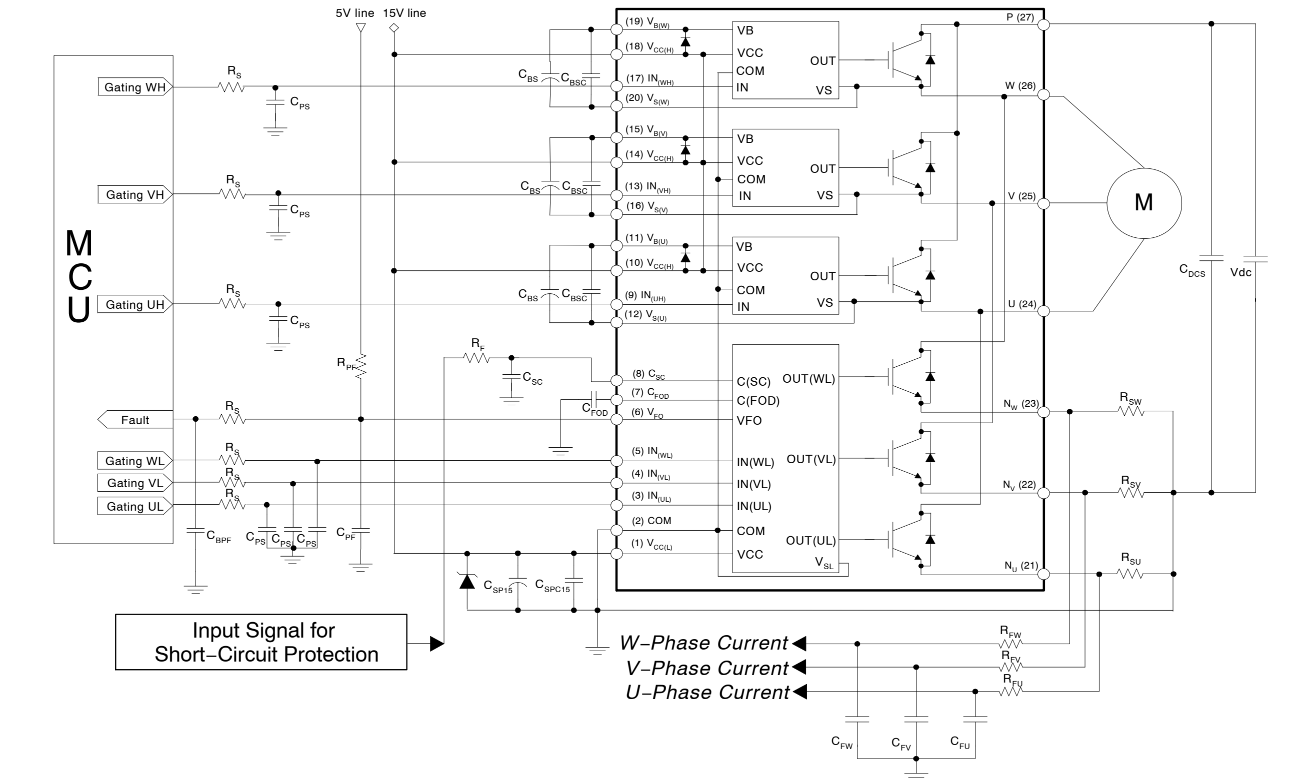
NOTES:
10. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 3 product integrates a 5 kΩ (typ.) pull−down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
11. The logic input works with standard CMOS or LSTTL outputs.

Figure 10. Recommended MCU I/O Interface Circuit



NOTE:
12. The ceramic capacitor placed between V_{CC} – COM should be over 1 μF and mounted as close to the pins of the Motion SPM 3 product as possible.

Figure 11. Recommended Bootstrap Operation Circuit and Parameters



NOTES:

13. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 − 3 cm).
14. By virtue of integrating an application−specific type of HVIC inside the Motion SPM 3 product, direct coupling to MCU terminals without any optocoupler or transformer isolation is possible.
15. V_{FO} output is open−collector type. This signal line should be pulled up to the positive side of the 5 V power supply with approximately 4.7 kΩ resistance. Please refer to Figure 10.
16. C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
17. V_{FO} output pulse width should be determined by connecting an external capacitor (C_{FOD}) between C_{FOD} (pin7) and COM (pin2). (Example: if C_{FOD} = 33 nF, then t_{FO} = 1.8 ms (typ.)) Please refer to the note 5 for calculation method.
18. Input signal is High−Active type. There is a 5 kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. $R_S C_{PS}$ time constant should be selected in the range 50 ~ 150 ns. C_{PS} should not be less than 1 nF.(Recommended R_S = 100 Ω, C_{PS} = 1 nF).
19. To prevent errors of the protection function, the wiring around R_F and C_{SC} should be as short as possible.
20. In the short−circuit protection circuit, please select the $R_F C_{SC}$ time constant in the range 1.5 ~ 2 μs.
21. Each capacitor should be mounted as close to the pins of the Motion SPM 3 product as possible.
22. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high frequency non−inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
23. Relays are used in almost every systems of electrical equipment of home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
24. C_{SPC15} should be over 1 μF and mounted as close to the pins of the Motion SPM 3 product as possible.

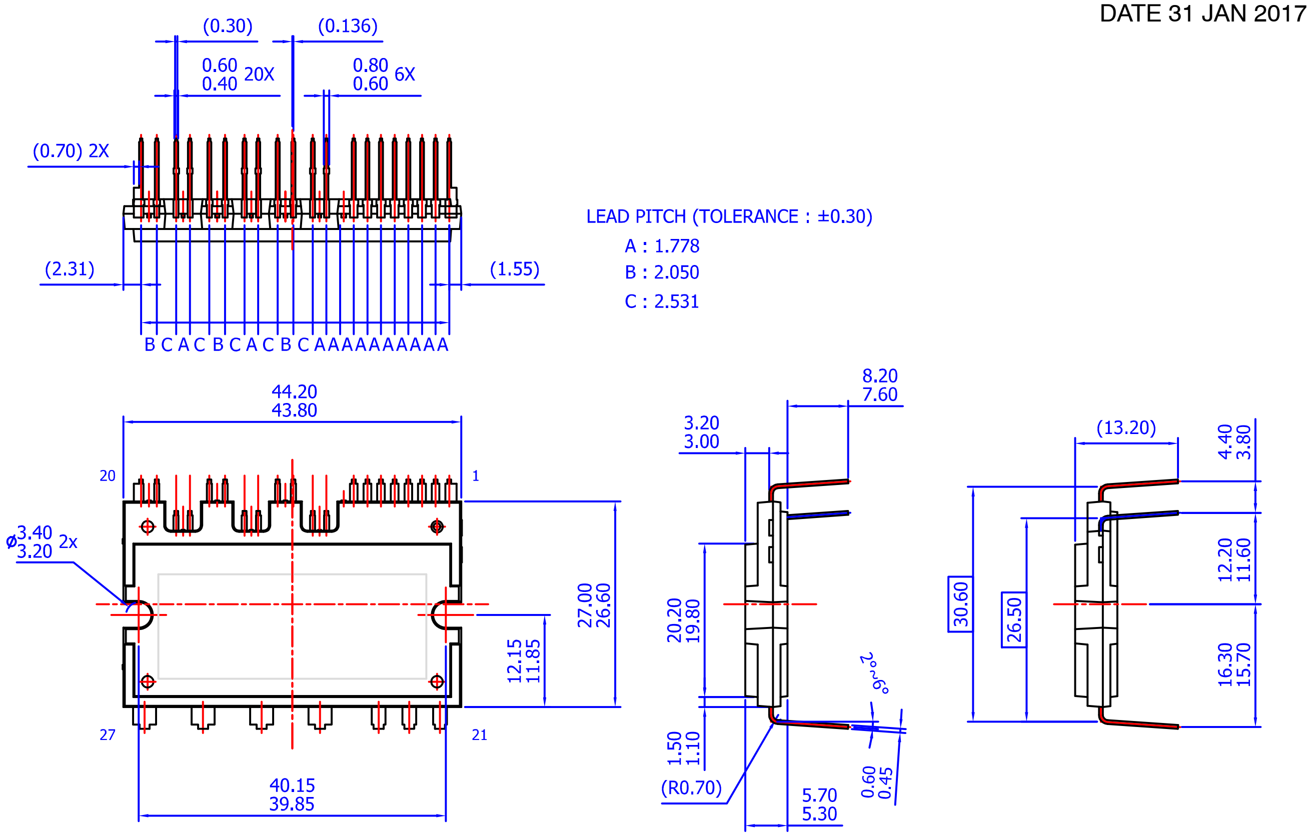
Figure 12. Typical Application Circuit

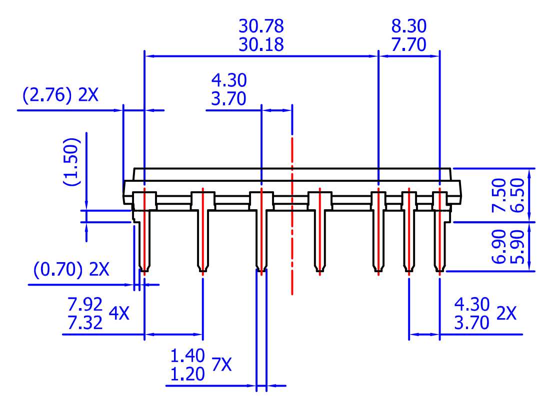
ORDERING INFORMATION

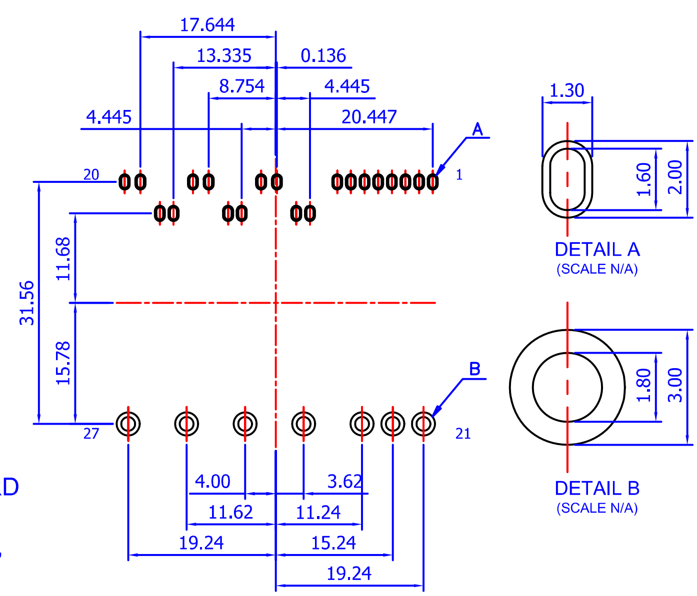
Device Order Number	Package Type	Shipping
FSBB30CH60C	SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE (Pb−Free)	60 Units / Tube

SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE
CASE MODFJ
ISSUE O

DATE 31 JAN 2017







NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

LAND PATTERN RECOMMENDATIONS

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