MAX1720x/MAX1721x Battery Pack Implementation Guide

UG6258; Rev 0; 2/16

Description

This guide provides the instructions for designing the PCB and programming the MAX17201/MAX17211/ MAX17205/MAX17215 for use in battery packs. Proper circuit board layout is critical for measurement accuracy and ESD ruggedness. This application note is a guide for achieving the highest performance possible given limited board size and component position flexibility. **Figure 1** shows a single-cell (MAX17201/MAX17211) and a multi-cell (MAX17205/MAX17215) circuit configuration. Note that other circuit configurations for this IC are possible, and should follow the same layout guidelines. This guide also includes a recommended board level production test procedure requiring minimum test time.

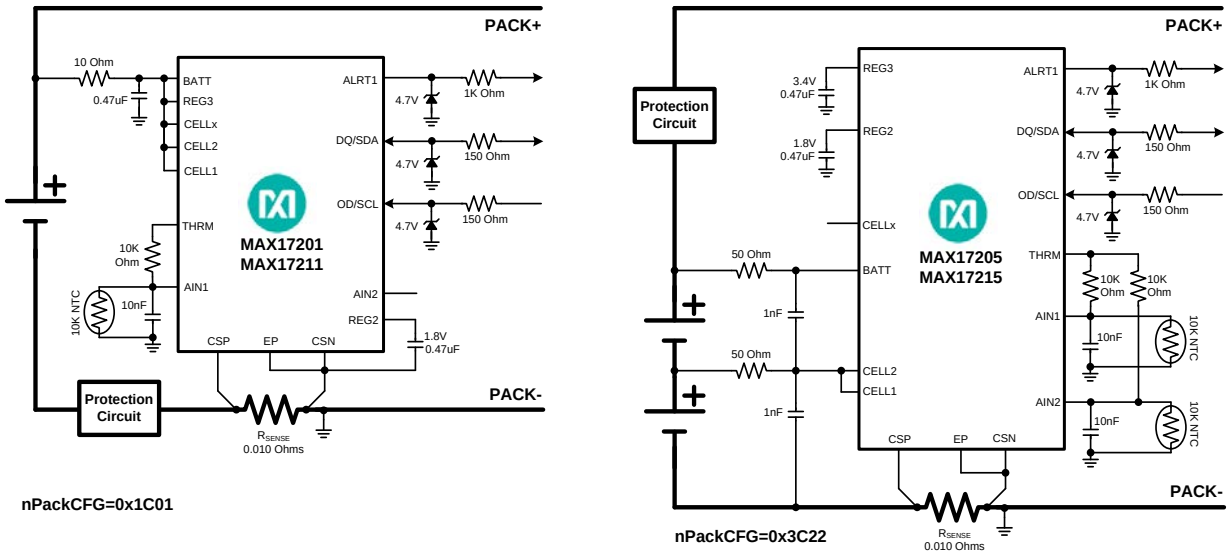

Figure 1. Single-cell and multi-cell circuit schematics.

Typical handheld applications limit board space to the dimensions of the accompanying cell. Components are normally limited to just one side of a 4-layer board with the external contacts located on the opposite side. The battery connection pads are normally on the ends while the external contact pads are normally grouped in the middle. **Figure 2** shows the physical board requirements for this example.

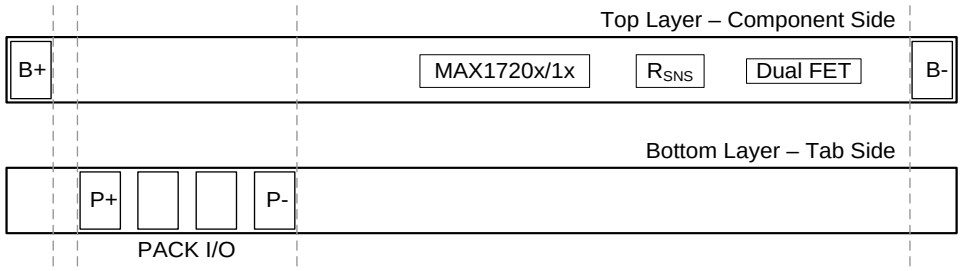

Figure 2. General board requirements.

Layout considerations for current measurement accuracy

To determine current flow through the pack, the MAX1720x/1x performs a differential voltage measurement across the external sense resistor through the CSP and CSN pins. The CSP pin is a high-impedance ADC input, but the CSN pin shares the ADC input with the power supply ground of the IC. Because there is current flow through the CSN pin, external resistance must be kept to a minimum. Any external resistance on CSN directly translates into negative offset error of the current measurement result.

Figure 3 shows the recommended board layout to achieve maximum current measurement accuracy. The circuit connections related to current measurement are shaded dark blue in the example.

1. Minimize CSN resistance

   The CSN trace should travel directly from the CSN pin to the battery side of the sense resistor. The trace length should be minimized, and should not travel through vias. Whenever possible maximize the trace width.

2. Minimize regulator bypass capacitor loop areas

   The REG2 and REG3 bypass capacitors should be mounted as close as possible to the IC with connections running directly to the CSN, REG2 and REG3 pins. Minimize any loop area between the capacitor and the IC. Note that the MAX17201/MAX17211 does not require a REG3 capacitor. The REG2 loop area must still be minimized.

3. Kelvin connection to sense resistor

   The CSN and CSP traces from the IC should run directly to the sense resistor pads. There should be no shared trace area with the high-current path of battery negative (B-) and pack negative (P-).

4. **Minimize CSN/CSP loop area**

   The CSP input is high impedance; therefore, the trace can have series resistance without affecting accuracy. Ideally, the CSP trace should run parallel to the CSN trace to minimize inductive loop area between the two.

5. **Exposed Pad connection**

   Connect the exposed pad directly to the CSN pin.

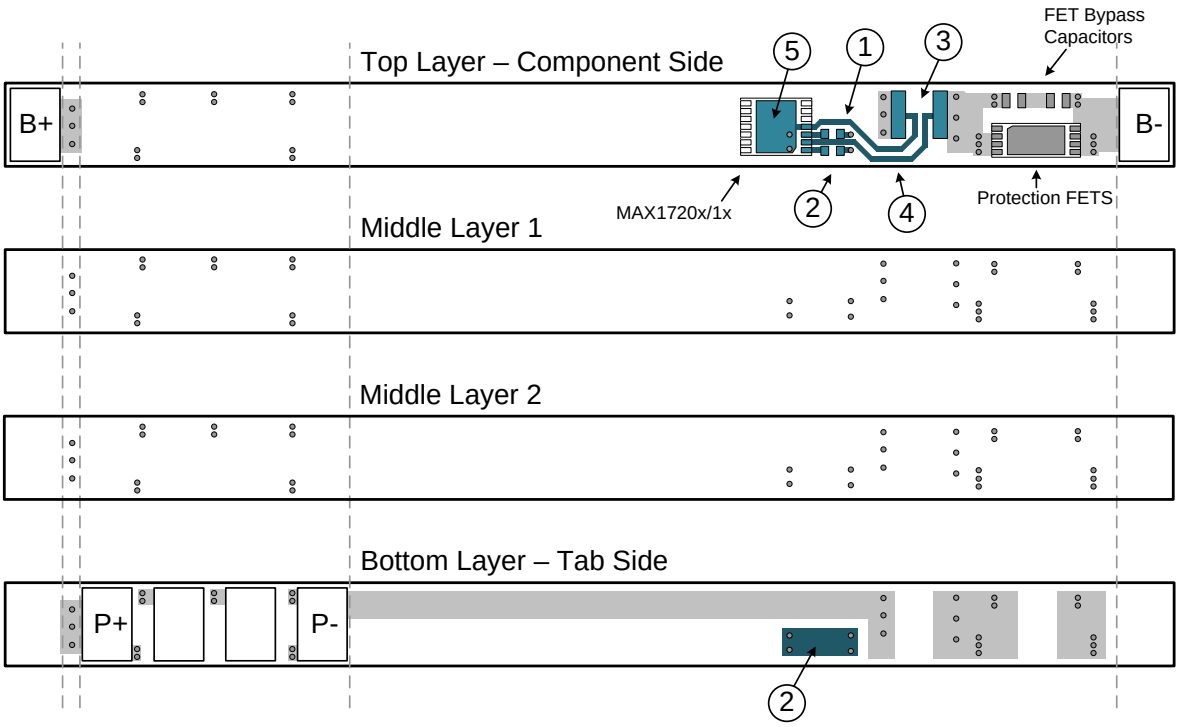

Figure 3. Recommended layout for current measurement accuracy.

Layout considerations for ESD Immunity

ESD energy can enter the cell pack through the exposed output pads. The energy follows the most direct path to the cell and leaves the cell pack through capacitive coupling to the environment. The goal of adding ESD protection to the MAX1720x/1x circuit board is to provide a channel for the ESD energy to leave the board safely and provide a buffer area around the MAX1720x/1x to isolate it.

External capacitors are added in series to provide a high energy path around the protection FETs and between the pack outputs. The Zener diodes on communication lines allow ESD energy to move to the negative pack terminal. The communication line resistors limit current through these diodes during an ESD event. **Figure 4** shows the desired high energy paths during ESD events.

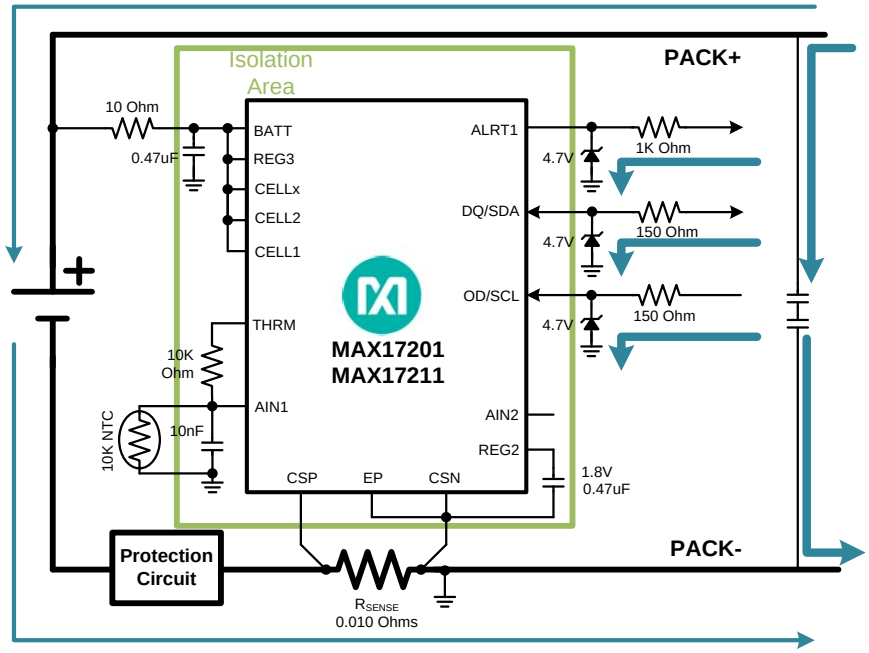

Figure 4. Circuit schematic showing ESD channeling paths.

For circuit layout, traces expected to carry ESD energy should have minimum inductance. They should be wide and short, and travel in the most direct manner possible from the input pads to the cell tabs. Ideally, the MAX1720x/1x should be completely removed from any area carrying high current; however, cell pack board limitations make this nearly impossible in most applications. At a minimum, the MAX1720x/1x should be isolated from these paths as much as possible by physical placement of the IC and by surrounding the IC with a ground plane. **Figure 5** shows the recommended board layout for optimum ESD performance. Only the components and traces associated with current measurement accuracy and ESD performance are shown.

1. Spark gaps

   Spark gaps provide a path for ESD energy to leave the board by a direct route instead of through critical components. The spark gaps in this example provide quick exit paths to the battery terminals from the input pads. The industry standard for a spark gap is 0.2mm spacing on an external board layer, exposed copper.

2. Passive component placement

   Depending on ESD strike location and polarity, ESD energy travels through the communication line series resistors and Zener diodes to PACK-. The ideal placement location for these components is directly behind the input pads using wide circuit traces. This helps direct the ESD energy through these components and away from the IC.

3. **FET bypass capacitors**

   FET bypass capacitors help provide an alternate path to channel ESD energy away from the protection FETs. As with the other passive components, trace widths should be kept short and wide.

4. **Ground plane**

   Not shown in **Figure 5**. Any unused board area on the component layer and middle layers should be connected to a ground plane that isolates the IC as much as possible from the ESD channeling traces. This ground plane should be connected to the battery negative as close as possible to the B- tab.

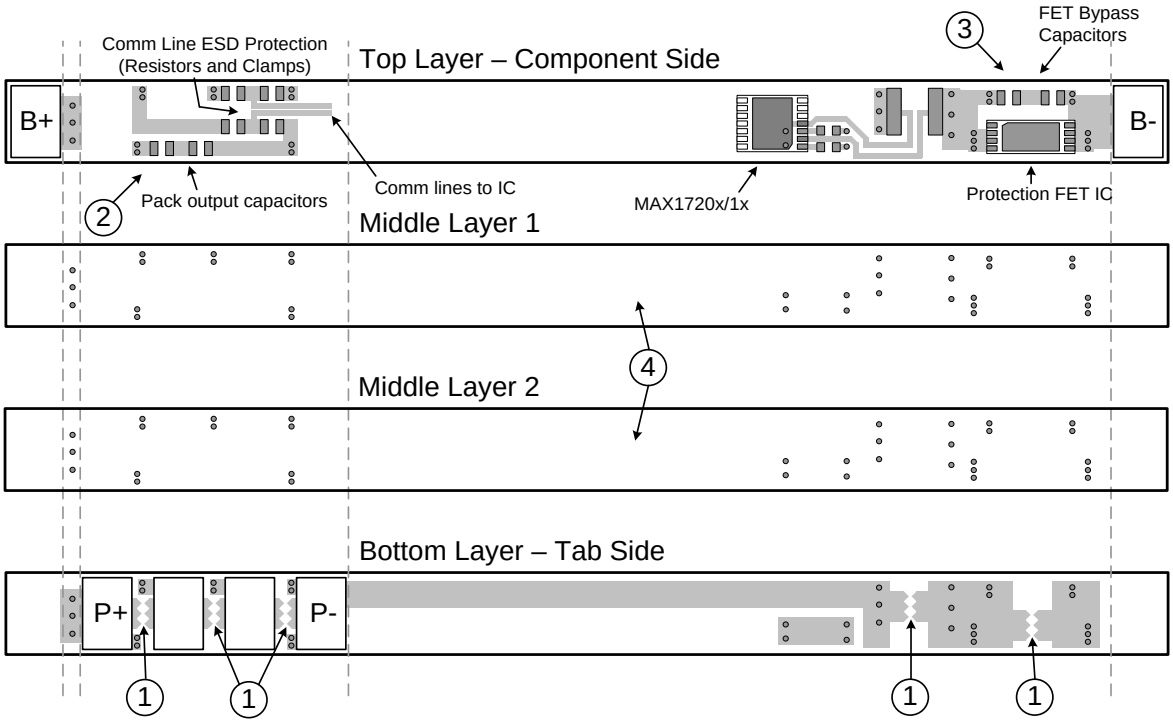

Figure 5. Recommended layout for ESD immunity.

Nonvolatile Memory Operations

The table below shows the nonvolatile memory of the MAX1720x/1x. The different highlighting separates the sections into what is provided by the battery characterization table, what is programmed by the factory, and the registers that are free or configurable to be free memory.

PAGE	18xh	19xh	1Axh	1Bxh	1Cxh	1Dxh
0h	nXTable0	nOCVTable0	nQRTable00	nConfig	nVAlrtTh	nUser1D0
1h	nXTable1	nOCVTable1	nQRTable10	nRippleCfg	nTAlrtTh	nUser1D1
2h	nXTable2	nOCVTable2	nQRTable20	nMiscCfg	nSAlrtTh	nAgeFcCfg
3h	nXTable3	nOCVTable3	nQRTable30	nDesignCap	nIAlrtTh	nDesignVoltage
4h	nXTable4	nOCVTable4	nCycles	nHibCfg	nUser1C4	nUser1D4
5h	nXTable5	nOCVTable5	nFullCapNom	nPackCfg	nUser1C5	nRFastVShdn
6h	nXTable6	nOCVTable6	nRComp0	nRelaxCfg	nFullSOCThr	nManfctrDate
7h	nXTable7	nOCVTable7	nTempCo	nConvgCfg	nTTFCfg	nFirstUsed
8h	nXTable8	nOCVTable8	nIAvgEmpty	nNVCfg0	nCGain	nSerialNumber0
9h	nXTable9	nOCVTable9	nFullCapRep	nNVCfg1	nTCurve	nSerialNumber1
Ah	nXTable10	nOCVTable10	nVoltTemp	nNVCfg2	nTGain	nSerialNumber2
Bh	nXTable11	nOCVTable11	nMaxMinCurr	nSBSCfg	nTOff	nDeviceName0
Ch	nUser18C	nIChgTerm	nMaxMinVolt	nROMID0	nManfctrName0	nDeviceName1
Dh	nUser18D	nFilterCfg	nMaxMinTemp	nROMID1	nManfctrName1	nDeviceName2
Eh	nODSCTh	nVEmpty	nSOC	nROMID2	nManfctrName2	nDeviceName3
Fh	nODSCCfg	nLearnCfg	nTimerH	nROMID3	nRSense	nDeviceName4

Legend:

Required for Custom Model	If a custom model is being used, these register needs to be programmed.
Required for 1-Wire® ID	These registers are used for the 1-Wire ROM ID and device serial number. They are not writable.
Optional Customer Registers	These registers don't have fuel gauge functions. The customer can use these for their suggested operation (such as FirstUsed, ManfctName), or in any other mode.
Free-able Memory	These registers contain algorithm/IC operation information, but the default values can be loaded from ROM, leaving these registers free for customer data.
Mandatory Configuration Registers	These registers must be configured for the IC to work correctly.

Figure 6. Nonvolatile memory operation descriptions.

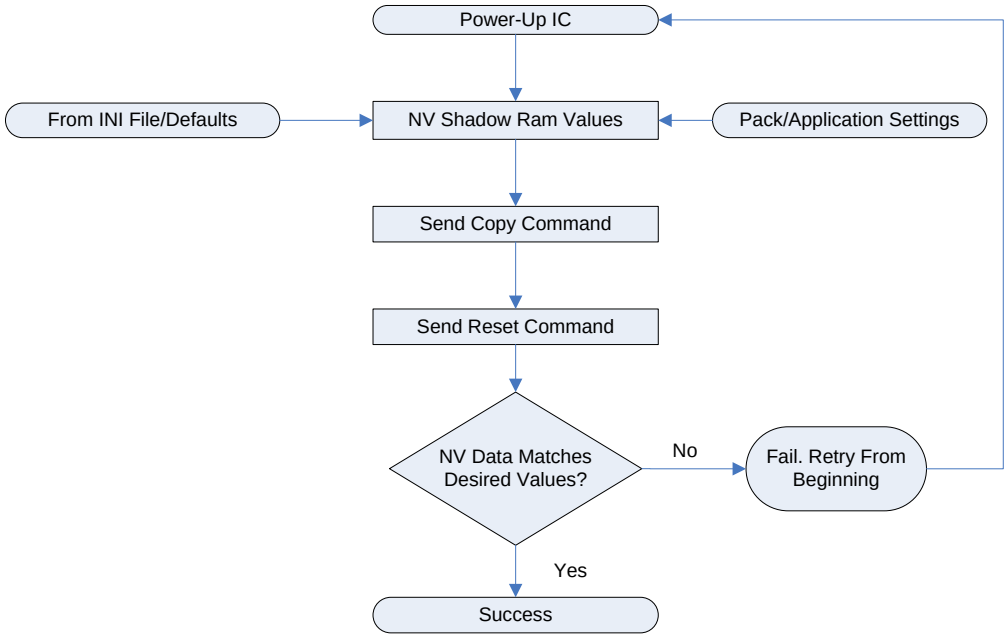

Figure 7. Nonvolatile memory loading process.

The starting values for the memory table should be obtained from the INI file (or default values if no custom model is available). The EV kit GUI configuration wizard can be used to configure all of the nonvolatile memory, or the values can be constructed by exploring each register in the data sheet. The Customer Memory can be written to any values desired by the pack maker or end customer.

Once the values are known, they should be written to the Shadow memory at the addresses listed in the above table. To copy the contents of Shadow Ram to nonvolatile memory, send command 0xE904 to register 0x060 to initiate a burn. Wait until CommStat.NVBusy is cleared to indicate the copy command is complete. This takes approximately 368 ms (t_{BLOCK}). Register 0x061 (CommStat) contains the NVBusy and NVError bits. NVError is set if an error occurred during the burn. NVBusy is clear when the burn operation is complete.

The IC should be reset to force the RAM to update to the desired configuration. To issue a full IC reset, the ESD detection mechanism has to be bypassed. This is accomplished by modifying the model table. The following sequence forces a complete IC reset. If the fuel gauge performance is evaluated shortly after the reset, the battery must be relaxed (no charge or load for 1 hour) before the reset command is sent.

1. Write register 0x062 = 0x0059
2. Write register 0x063 = 0x00C4
3. Write register 0x080 = 0x0000
4. Write register 0x060 = 0x000F
5. Wait 150ms (NV memory recall and RAM initialization)
6. Write register 0x0BA to clear bit 0x8000 (Disable hibernate mode. It should be re-enabled at the end of factory production.)

After the reset is complete, the contents of the nonvolatile memory should be verified against the desired write values. If everything matches, the process is complete. If there is any discrepancy, the number of write cycles should be examined to check if there is nonvolatile memory remaining. See the *Determining the Number of Remaining Updates* section of the data sheet for details.

Locking the Battery Model

MAX1720x/1x has a locking feature to permanently set the contents of the nonvolatile memory. The locks on the IC can be set for different portions of the memory in 5 different configuration sections. The process for setting the locks is:

1. Write register 0x061 = 0 to clear the Comstat.NVError bit
2. Write register 0x060 = 0x6Axx with xx representing the lock code. The lower 5 bits set Lock 5 to Lock 1 as described in the table below.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	1	0	X	X	X	LOCK5	LOCK4	LOCK3	LOCK2	LOCK1

3. Wait until NVBusy clears for the copy command to complete (t_{UPDATE} = 64 ms typical).
4. Read register 0x061 to see if the operation completed successfully.

Setting the SHA Secret for Authentication

The SHA secret in the IC cannot be directly read out or written. To initialize the SHA secret, the following sequence is needed.

1. Clear the NVError bit (Write register 0x060 = 0).
2. Validate the secret is all zeros by computing a response with all zeros.
3. If the secret is not all zeros, clear the SHA Secret to all zeros (Write register 0x060 = 0x5A00).
4. The secret clears to all zeros after the NVBusy flag clears (t_{UPDATE} = 64 ms typical).
5. Write a challenge to addresses 0x0C0 to 0x0C9.
6. Send either the Next Secret with ROM ID (write 0x060 = 0x3300) or without ROM ID (write 0x060=0x3000).
7. The New Secret is the last 160 bits of the response.
8. Validate that the internal secret is what is expected by writing a new challenge and validating the response.
9. Send the Lock Secret command (write 0x060 = 0x6000). **This lock is irreversible**. It permanently locks the SHA secret, and it is not changeable. If a multistep secret generation process is used, the lock should only be set at the final step.

Production Test

Hibernate mode should already be disabled in the nonvolatile memory initialization section. If it is not disabled, clear HibCfg.EnHib. Ensure that Status2.HibStat is clear before proceeding.

1. Check Communication
    - Validate that the IC is powered on by reading the DevName register (0x021). If the IC responds with the correct version number, the communication test is successful.
2. Check Voltage measurement
    - Read the VCell register (or Cell1, Cell2, Cell3 based on the pack configuration) and compare the measured voltage against the IC readings. If the error is less than 10mV, the voltage measurement check is successful.
3. Check no load current measurement
    - Check the current and AvgCurrent registers. The current should read in the range of +1mA to –1mA.
4. Set the load to the lesser of half the full scale measurement range ($25mV/R_{SENSE}$), or half of the cell C-Rate (C/2).
    - Apply the selected load current.
    - Read the Current register.
    - Wait until the Timer register changes (up to 702 ms).
    - The test is successful if the current reading is in an acceptable range of the set load current.

Calibration

This fuel gauge does not require any calibration. The voltage, current, and temperature accuracy are trimmed during the Maxim Integrated factory test program. The algorithm does not require any cycling for accurate state-of-charge reporting.

Conclusion

This application note describes the various steps for implementing MAX1720x/MAX17021x in a battery pack including how to lay out the circuit board to achieve the best possible current measurement accuracy and ESD immunity given the requirements of the circuit board. The memory programming instructions describe how to load the fuel gauge and authentication information and lock it to prevent tampering with the authentication or fuel gauge mechanisms.