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APPLICATION NOTE 6509

HOW TO TRANSMIT/RECEIVE SSMS IN THE DS26521 AND DS2155

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Abstract: This application note provides a step-by-step procedure to configure the DS26521 and DS2155 registers to handle SSMs in T1 and E1 modes.

Introduction

Apart from BITS elements like in the DS26504, DS26503, etc., normal SCTs like the DS26521 and DS2155 can also be used to transmit/receive SSMs. SSMs (synchronization status messages) defined in ANSI (T1.105) and ITU-T (G.703) recommendations identify the quality level of the incoming clock. In T1 mode, these messages are transmitted as bit-oriented codes in the datalink bits; in E1 mode, these are transmitted using one of the five Sa bits. The HDLC controllers present in the device can also be used to transmit or receive an SSM. In addition to the DS2155 and DS26521, this application note can be used to configure SSMs in the DS26514, DS26518, and DS26522 by mapping the registers.

In T1 mode, an SSM is transmitted and received in the DS26521 and DS2155 using two methods:

- BOC generator on the transmit side and a BOC detector on the receive side
- HDLC controllers

Even though HDLC controllers could be used for this purpose, using the BOC engine is recommended.

In E1 mode, an SSM is transmitted and received using the five Sa bits. An SSM is valid only when seven out of 10 messages are alike.

Acronyn	Description
BOC	Bit Oriented Code
CRC	Cyclic Redundancy Check
FDL	Facilities Data Link
HDLC	High-Level Data Link Control
SSM	Synchronization Status Message

Procedure for Configuring the DS2155 to Transmit/Receive SSM in T1 Mode

Steps to Transmit a BOC Message

1. Bits 0 to 5 of the TFDL register must be loaded with messages to be transmitted. The message is transmitted as 0xxxxxx0 11111111, where x's represent an actual SSM. The transmit BOC controller automatically handles the 0s and ignores FFh. The respective FDL code from **Table 1** should be loaded to the TFDL register from bit 0 to bit 5.

Table 1. SSM Codes for T1 Operation

Quality Level	Description	FDL Code Word (DS1 ESF)
1	Stratum 1 traceable	0 **000010**0 11111111
2	Synchronized traceability unknown	0 **000010**0 11111111
3	Stratum 2 traceable	0 **000110** 0 11111111
4	Stratum 3 traceable	0 **000010**0 11111111
5	SONET minimum clock traceable	0 **010001**0 11111111
6	Stratum 4 traceable	0 **010100** 0 11111111
7	Do not use for synchronization	0 **011000** 0 11111111
User Assignable	Reserved for network synchronization use	0 **100000** 0 11111111

2. Set bit 0 of the BOCC register to 1 to start transmitting the SSM.

Register Description **BOC Control Register**
Register Address **37h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RBOCE	RBR	RBF1	RBF0	SBOC
Default	0	0	0	0	0	0	0	0

Bit 0/Send BOC (SBOC). Set = 1 to transmit BOC Code placed in bits 0 to 5 of the TFDL register.

Figure 1. BOCC control register description.

Steps to Receive a BOC Message

1. Set bit 0 of the receive BOCC register to 1.
2. Enable the receive BOC change of state interrupt by bit 0 of the IMR8 register to 1.

3. Bit 0 of the SR8 register indicates if any change of state interrupt has occurred.
4. The lower 6 bits of the RFDL register contain the received BOC messages.

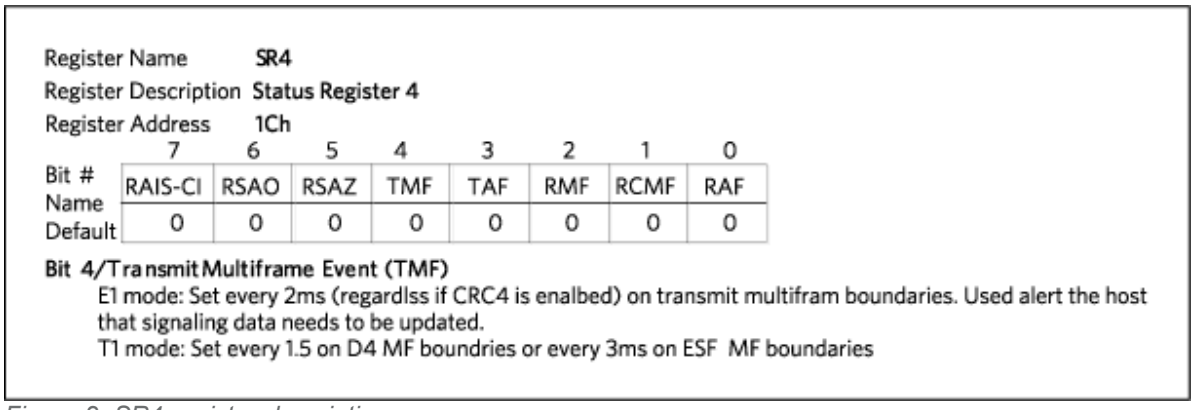
The host can then read the RFDL register for the received BOC message. Bit 7 of the SR2 register is set if the received BOC message is valid.

Procedure for Configuring DS2155 to Transmit/Receive SSM in E1 Mode

Steps to Transmit SSM

On the transmit side, Sa bits can be inserted into the Sa bit control registers (TSACR).

1. Load any register among TSa4 to TSa8 with the SSM code to be transmitted.
2. Set bit 4 of SR4 register to start transmitting the SSM.



Register Name SR4
Register Description Status Register 4
Register Address 1Ch

Bit #	7	6	5	4	3	2	1	0
Name	RAIS-CI	RSAO	RSAZ	TMF	TAF	RMF	RCMF	RAF
Default	0	0	0	0	0	0	0	0

Bit 4/Transmit Multiframe Event (TMF)
E1 mode: Set every 2ms (regardlss if CRC4 is enalbed) on transmit multifram boundaries. Used alert the host that signaling data needs to be updated.
T1 mode: Set every 1.5 on D4 MF boundries or every 3ms on ESF MF boundaries

Figure 2. SR4 register description.

3. TASCR, which is the transmit Sa-bit control register, should be configured to insert data from the TSa4:TSa8 register into the transmit data stream.

Steps to Receive SSM

1. Set bit 1 of SR4 register. This enables CRC4 multiframe boundaries.
2. The received Sa bits are stored in RSa4 to RSa8. Any of these registers can be selected to receive the incoming Sa bits.

Procedure for Configuring DS26521 to Transmit/Receive SSM in T1 Mode

Steps to Transmit SSM

1. Write 6-bit SSM code into T1TBOC register.
2. Set bit 6 (SBOC) of THC2 register to enable SSM transmission.

Register Name THC2
Register Description Transmit HDLC Control Register 2
Register Address 113h

Bit #	7	6	5	4	3	2	1	0
Name	TABT	SBOC	THCEN	THCS4	THCS3	THCS2	THCS1	THCS0
Default	0	0	0	0	0	0	0	0

Bit 6/Send BOC (SBOC) (T1 mode only). Set =1 to transmit the BOC code placed in bits 0 to 5 of the T1TBOC register

Figure 3. THC2 register description.

Steps to Receive SSM

1. Bit 0 of the RLS7 register is set when a valid BOC message is received.
2. T1RBOC register contains the received BOC message.

Procedure for Configuring DS26521 to Transmit/Receive SSM in E1 Mode

Steps to Transmit SSM

1. E1TSa4:E1TSa8 registers can be used to send SSM.

Register Name E1TSa4
Register Description Transmit Sa4 Bits Register
Register Address 169h

Bit #	7	6	5	4	3	2	1	0
Name	TSa4F15	TSa4F13	TSa4F11	TSa4F9	TSa4F7	TSa4F5	TSa4F3	TSa4F1
Default	0	0	0	0	0	0	0	0

Bit 7/Sa 4 bit of Frame 15 (TSa415).
Bit 6/Sa 4 bit of Frame 13 (TSa413).
Bit 5/Sa 4 bit of Frame 11 (TSa411).
Bit 4/Sa 4 bit of Frame 9 (TSa49).
Bit 3/Sa 4 bit of Frame 7 (TSa47).
Bit 2/Sa 4 bit of Frame 5 (TSa45).
Bit 1/Sa 4 bit of Frame 3 (TSa43).
Bit 0/Sa 4 bit of Frame 1 (TSa41).

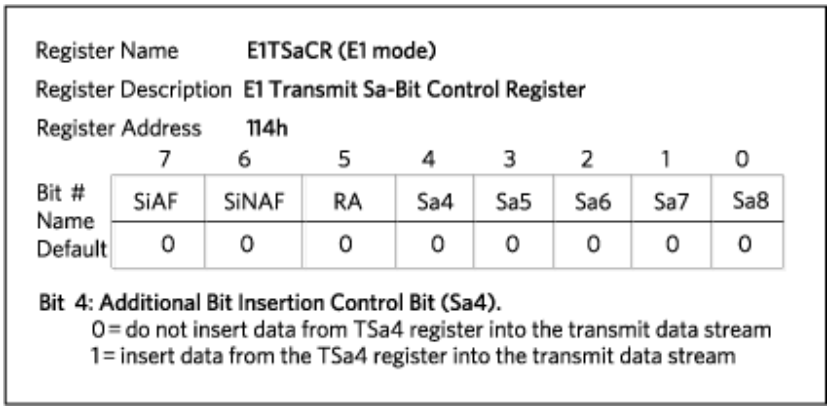
Figure 4. E1TSa4 register description.

Note: The lower nibble and higher nibble of this register should be loaded with the same SSM code.

Table 2. SSM Codes for E1 Operation

Quality Level	Description	San1, San2, San3, San4 (where n = bit number 4, 5, 6, 7, or 8)
0		0000
1		0001
2		0010
3		0011
4		0100
5		0101
6		0110
7		0111
8		1000
9		1001
10		1010
11		1011
12		1100
13		1101
14		1110
15		1111

2. E1TASCR, which is the transmit Sa-bit control register, should be configured to insert data from the TSa4:TSa8 register into the transmit data stream.



Register Name E1TSaCR (E1 mode)
Register Description E1 Transmit Sa-Bit Control Register
Register Address 114h

Bit #	7	6	5	4	3	2	1	0
Name	SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

Bit 4: Additional Bit Insertion Control Bit (Sa4).
0 = do not insert data from TSa4 register into the transmit data stream
1 = insert data from the TSa4 register into the transmit data stream

Figure 5. E1TSa4 register description.

3. CRC-4 multiframe mode should be enabled in the E1TCR1 register.

Register Name TCR1 (E1 mode)

Register Description Transmit Control Resister 1

Register Address 181h

Bit #	7	6	5	4	3	2	1	0
Name	TTPT	T16S	TG802	TSiS	TSA1	THDB3	TAIS	TCRC4
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit CRC4 Enable (TCRC4)
0= CRC4 disabled
1= CRC4 enabled

Figure 6. TCR1register description.

Steps to Receive SSM

1. Wait for Bit 1 of RLS2 register to set.
2. The received SSM code is in any of the RSa4:RSa8 registers.

Related Parts		
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS26514	4-Port T1/E1/J1 Transceiver	Free Samples
DS26518	8-Port T1/E1/J1 Transceiver	Free Samples
DS26521	Single T1/E1/J1 Transceiver	Free Samples
DS26522	Dual T1/E1/J1 Transceiver	Free Samples

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