DLP3000 DLP® 0.3 WVGA Series 220 DMD

1 Features

- 0.3-Inch (7.62 mm) Diagonal Micromirror Array
  - 608 × 684 Array of Aluminum, Micrometer-Sized Mirrors Offering up to WVGA Resolution (854 × 480) Wide Aspect Ratio Display
  - 7.6-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Side Illumination for Optimized Efficiency
  - 5-µs Micromirror Crossover Time
- Highly Efficient in Visible Light (420 to 700 nm):
  - Window Transmission 97%
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
  - Polarization Independent
- Package Footprint of 16.6-mm × 7-mm × 4.6-mm
- Low Power Consumption at 200 mW (Typical)
- Dedicated DLPC300 Controller for Reliable Operation
- Supports High-Speed Pattern Rates of 4000 Hz (Binary) and 120 Hz (8-Bit)
- 15-Bit, Double Data Rate (DDR) Input Data Bus
- 60- to 80-MHz Input Data Clock Rate
- Integrated Micromirror Driver Circuitry
- Supports 0°C to 70°C
- Package Mates to PANASONIC AXT550224 Socket

2 Applications

- Machine Vision
- Industrial Inspection
- 3D Scanning Such as Dental Scanners
- 3D Optical Metrology
- Automated Fingerprint Identification
- Face Recognition
- Augmented Reality
- Embedded Display
- Interactive Display
- Information Overlay
- Spectroscopy
- Chemical Analyzers
- Medical Instruments
- Photo-Stimulation
- Virtual Gauges

3 Description

The DLP3000 digital micromirror device (DMD) is a digitally-controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM) optimized for small form-factor applications. When coupled to an appropriate optical system, the DLP3000 can be used to modulate the amplitude and direction of incoming light. The DLP3000 creates highly flexible light patterns with speed, precision, and efficiency.

Architecturally, the DLP3000 is a latchable, electrical-in/optical-out semiconductor device. This architecture makes the DLP3000 well-suited for use in applications such as 3D scanning or metrology with structured light, augmented reality, microscopy, medical instruments, and spectroscopy. The compact physical size of the DLP3000 is well-suited for portable equipment where small form factor and lower cost are important. The compact package complements the small size of LEDs to enable highly-efficient, robust light engines.

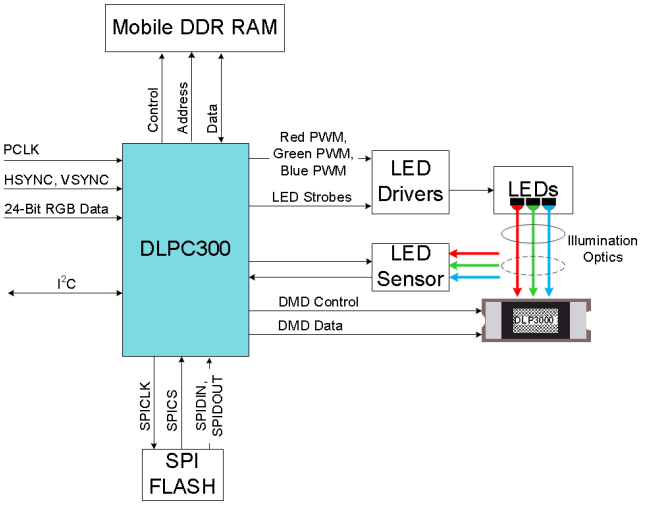
The DLP3000 is one of two devices in the DLP® 0.3 WVGA chipset. Proper function and reliable operation of the DLP3000 requires that it be used in conjunction with the DLPC300 controller. See the DLP 0.3 WVGA chipset data sheet (DLPZ005) for further details.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP3000	LCCC (50)	16.6 mm × 7.0 mm × 4.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2012) to Revision B **Page**

- Added *ESD Ratings* table, *Storage Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed package thickness from 5.0mm to 4.6mm ... 1
- Changed minimum temperature from -10°C to 0°C to match long term operational temperature range ... 1
- Added package body size dimensions to Device Information table ... 1
- Changed DMD picture to simplified application block diagram ... 1
- Changed image to a cleaner source file ... 4
- Changed *Absolute Maximum Ratings* table to include operational temperatures and dew points ... 7
- Changed the *Recommended Operating Conditions* table to include operating and non-operating temperature ranges, dew points, and the illumination power density ... 8
- Added *Max Recommended Array Temperature - Derating Curve* ... 9
- Added note to *Thermal Information* table ... 9
- Added *Bit Depth versus Pattern Rate* table ... 12
- Moved the Mechanical section from the *Recommended Operating Conditions* table to the *System Mounting Interface Loads section* ... 13
- Added *Window Characteristics* section ... 17
- Added *Chipset Component Usage Specification* ... 17
- Added *Overview* in *Detailed Description* section ... 18
- Added description of *Functional Block Diagram* interfaces ... 18
- Changed formating of Thermal Characteristics, Package Thermal Resistance, Case Temperature, and Micromirror Array Temperature Calculation sections ... 22

Revision History (continued)

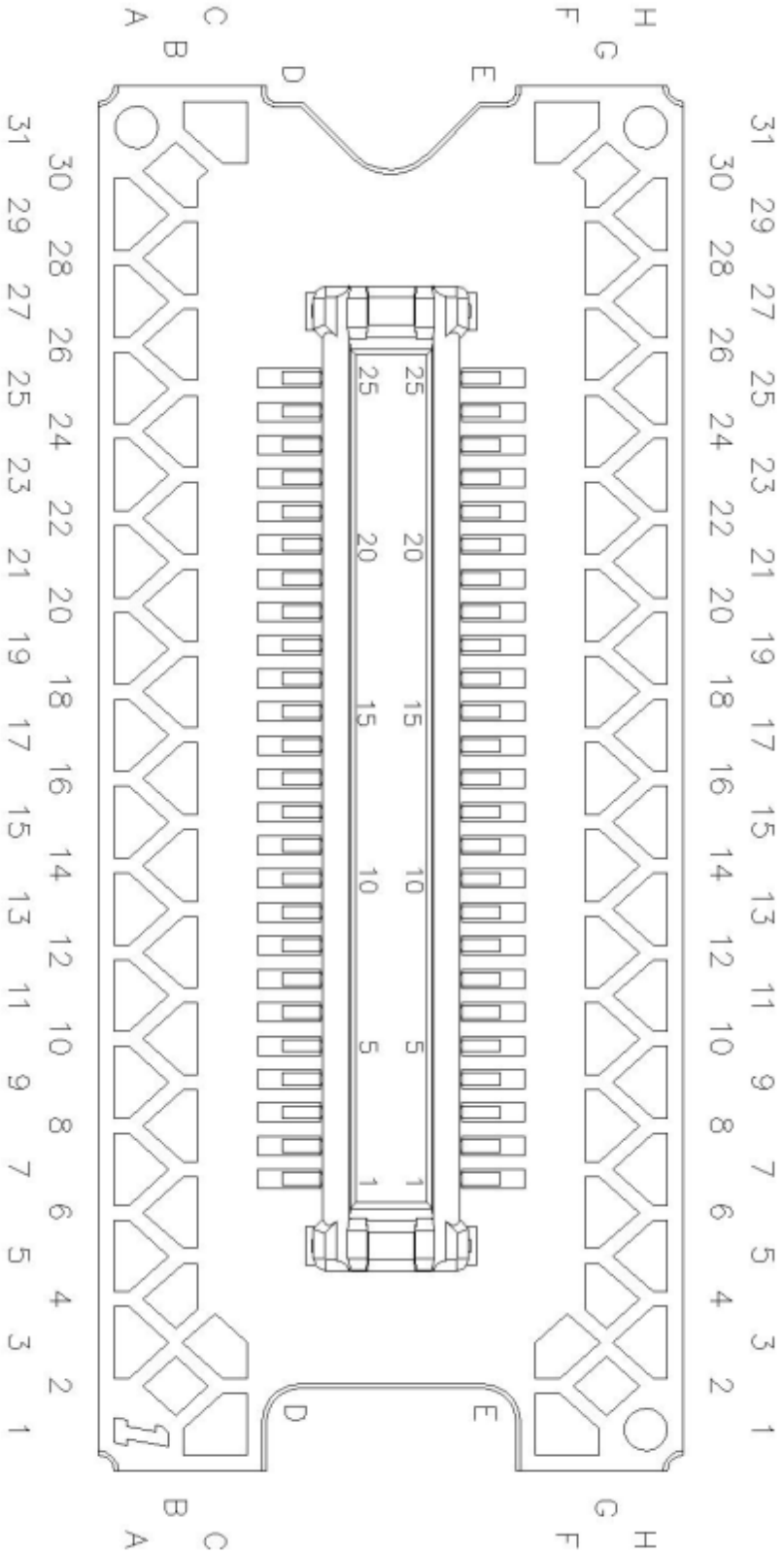
- Added *Landed Duty Cycle and Operational DMD Temperature* section 24

Changes from Original (January 2012) to Revision A **Page**

- Corrected the C_{L2W} constant value from: 0.00274 to 0.00293 W/lm 23

5 Pin Configuration And Functions

Package Connector Signal Names (Device Bottom View)



Pin Functions – Connector

PIN		I/O/P	SIGNAL	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
NAME	NO.						
DATA INPUTS							
DATA(0)	D2	Input	LVCMOS	None	DCLK	DDR	Input data bus
DATA(1)	D4	Input	LVCMOS	None	DCLK	DDR	
DATA(2)	D5	Input	LVCMOS	None	DCLK	DDR	
DATA(3)	D6	Input	LVCMOS	None	DCLK	DDR	
DATA(4)	D8	Input	LVCMOS	None	DCLK	DDR	
DATA(5)	D10	Input	LVCMOS	None	DCLK	DDR	
DATA(6)	D12	Input	LVCMOS	None	DCLK	DDR	
DATA(7)	D14	Input	LVCMOS	None	DCLK	DDR	
DATA(8)	E16	Input	LVCMOS	None	DCLK	DDR	
DATA(9)	E14	Input	LVCMOS	None	DCLK	DDR	
DATA(10)	E12	Input	LVCMOS	None	DCLK	DDR	
DATA(11)	E10	Input	LVCMOS	None	DCLK	DDR	
DATA(12)	E5	Input	LVCMOS	None	DCLK	DDR	
DATA(13)	E6	Input	LVCMOS	None	DCLK	DDR	
DATA(14)	E8	Input	LVCMOS	None	DCLK	DDR	
DCLK	E18	Input	LVCMOS	None	—	—	Input data bus clock
DATA CONTROL INPUTS							
$\overline{\text{LOADB}}$	E20	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	E4	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	E2	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SAC_BUS	E24	Input	LVCMOS	None	SAC_CLK	—	Stepped address control serial bus data
SAC_CLK	D24	Input	LVCMOS	None	—	—	Stepped address control serial bus clock
MIRROR RESET CONTROL INPUTS							
DRC_BUS	D22	Input	LVCMOS	None	SAC_CLK		DMD reset-control serial bus
$\overline{\text{DRC\_OE}}$	D20	Input	LVCMOS	None	—	—	Active-low output enable signal for internal DMD reset driver circuitry
DRC_STROBE	E22	Input	LVCMOS	None	SAC_CLK		Strobe signal for DMD reset control inputs
POWER							
VBIAS	D16	Power	Analog	None	—	—	Mirror reset bias voltage
VOFFSET	D21	Power	Analog	None	—	—	Mirror reset offset voltage
VRESET	D18	Power	Analog	None	—	—	Mirror reset voltage
VREF	E21	Power	Analog	None	—	—	Power supply for DDR low-voltage CMOS logic pins
VCC	D1, D13, D25, E1, E13, E25	Power	Analog	None	—	—	Power supply for single-data-rate LVCMOS logic pins
VSS	D3, D7, D9, D11, D15, D17, D19, D23, E3, E7, E9, E11, E15, E17, E19, E23	Power	Analog	None	—	—	Common return for all power inputs

Pin Functions – Connector (continued)

PIN		I/O/P	SIGNAL	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
NAME	NO.						
No connect	A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29 A31, B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B24, B26, B28, B30, C1, C3, C31, F1, F3, F31, G2, G4, G6, G8, G10, G12, G14, G16, G18, G20, G22, G24, G26, G28, G30, H1, H3, H5, H7, H9, H11, H13, H15, H17, H19, H21, H23, H25, H27, H29, H31	—	—	—	—	—	No connection (any connection to these pins may result in undesirable effects)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Voltage applied to V_{CC} (2)	–0.5	4	V
V_{REF}	Voltage applied to V_{REF} (2)	–0.5	4	V
V_{OFFSET}	Voltage applied to V_{OFFSET} (2)(3)(4)	–0.5	8.75	V
V_{BIAS}	Voltage applied to V_{BIAS} (2)(4)	–0.5	17	V
V_{RESET}	Voltage applied to V_{RESET} (2)	–11	0.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value) (4)		8.75	V
INPUT VOLTAGES				
	Voltage applied to all other input pins (2)	–0.5	V_{REF} + 0.3	V
I_{OH}	Current required from a high-level output, V_{OH} = 2.4 V		–20	mA
I_{OL}	Current required from a low-level output, V_{OL} = 0.4 V		15	mA
ENVIRONMENTAL				
T_{CASE}	Case temperature - operational (5) (6)	–20	90	ºC
	Case temperature - non–operational (6)	–40	90	ºC
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window, ceramic, or array - operational (7) (8)		15	°C
T_{DP}	Dew Point (operational and non-operational)		81	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminals V_{SS} (ground). The following power supplies are all required to operate the DMD: Voltages V_{SS}, V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than specified limit.
(5) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density will reduce the device lifetime.
(6) DMD Temperature is the worst-case of any test point shown in Figure 11, or the active array as calculated by the *Micromirror Array Temperature Calculation*.
(7) Ceramic package temperature as measured at test point 3 (TP 3) in Figure 11.
(8) As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. Refer to the *Micromirror Array Temperature Calculation* for information related to calculating the micromirror array temperature.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{stg}	DMD Storage Temperature	–40	85	°C
T_{DP}	Storage Dew Point - long-term (1)		24	°C
	Storage Dew Point - short-term (2)		28	°C

(1) Long-term is defined as the usable life of the device.
(2) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
ELECTRICAL					
V_{REF}	LVCMOS interface supply voltage(1)	1.65	1.8	1.95	V
V_{CC}	LVCMOS logic supply voltage(1)	2.375	2.5	2.625	V
V_{OFFSET}	Mirror electrode and HVCMOS supply voltage (1)(2)	8.25	8.5	8.75	V
V_{BIAS}	Mirror electrode voltage(1)(2)	15.5	16	16.5	V
V_{RESET}	Mirror electrode voltage(1)	–9.5	–10	–10.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(2)			8.75	V
V_{T+}	Positive-going threshold voltage	$0.4 \times V_{REF}$		$0.7 \times V_{REF}$	V
V_{T-}	Negative-going threshold voltage	$0.3 \times V_{REF}$		$0.6 \times V_{REF}$	V
V_{HYS}	Hysteresis voltage ($V_{T+} - V_{T-}$)	$0.1 \times V_{REF}$		$0.4 \times V_{REF}$	V
f_{DCLK}	DCLK clock frequency	60		80	MHz
ENVIRONMENTAL (3)					
T_{ARRAY}	Array Temperature – operational, long-term (4) (5) (6)	0		40 to 70(5)	°C
	Array Temperature – operational, short-term(4)(7)	–20		75	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window, ceramic, or array - operational(8) (9)			10	°C
ILL_{UV}	Illumination, wavelength < 420 nm			0.68	mW/cm^2
ILL_{VIS}	Illumination, wavelengths between 420 and 700 nm			Thermally Limited(10)	mW/cm^2
ILL_{IR}	Illumination, wavelength > 700 nm			10	mW/cm^2

(1) All voltage values are with respect to the ground terminals V_{SS} (ground). The following power supplies are all required to operate the DMD: Voltages V_{SS}, V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}.
(2) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than specified limit. See the *Absolute Maximum Ratings* for further details.
(3) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(4) Array Temperature is the worst-case of any test point shown in Figure 11, or the active array as calculated by the *Micromirror Array Temperature Calculation*.
(5) Per Figure 1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(6) Long-term is defined as the usable life of the device.
(7) Short-term is defined as less than 500 hours over the usable life of the device.
(8) Ceramic package temperature as measured at test point 3 (TP 3) in Figure 11.
(9) As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. Refer to the *Micromirror Array Temperature Calculation* for information related to calculating the micromirror array temperature.
(10) Refer to *Thermal Information* and *Micromirror Array Temperature Calculation*.

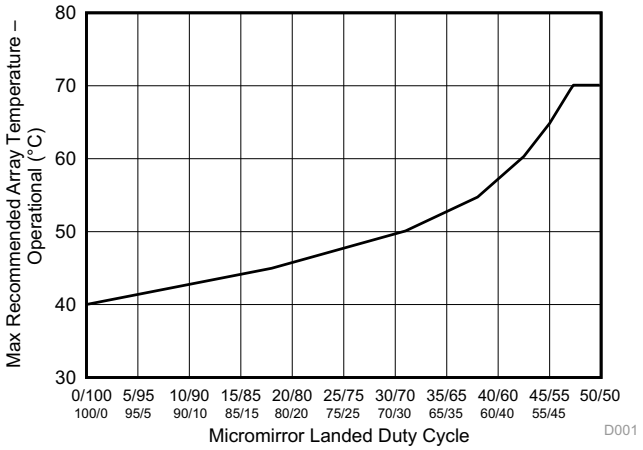


Figure 1. Max Recommended Array Temperature – Derating Curve

6.5 Thermal Information

THERMAL METRIC(1)	MIN	NOM	MAX	UNIT
Thermal resistance from active micromirror array to TC3			5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage(1)	V_{CC} = 2.375 V,	I_{OH} = –20 mA	1.7			V
V_{OL}	Low-level output voltage(1)	V_{CC} = 2.625 V,	I_{OL} = 15 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 1.7 V				–15	mA
I_{OL}	Low-level output current	V_{OL} = 0.4 V				14	mA
I_{IL}	Low-level input current	V_{REF} = 1.95 V,	V_I = 0 V	–1.6			nA
I_{IH}	High-level input current	V_{REF} = 1.95 V,	V_I = V_{REF}			1.9	nA
I_{REF}	Current into V_{REF} pin	V_{REF} = 1.95 V,	f_{DCLK} = 77 MHz			0.7	mA
I_{CC}	Current into V_{CC} pin	V_{CC} = 2.625 V,	f_{DCLK} = 77 MHz			55	mA
I_{OFFSET}	Current into V_{OFFSET} pin(2)	V_{OFFSET} = 8.75 V				1	mA
I_{BIAS}	Current into V_{BIAS} pin (2)	V_{BIAS} = 17 V				1.6	mA
I_{RESET}	Current into V_{RESET} pin (2)	V_{RESET} = –11 V				1.5	mA
P_{REF}	Power into V_{REF} pin(3)	V_{REF} = 1.95 V,	f_{DCLK} = 77 MHz			1.5	mW
P_{CC}	Power into V_{CC} pin (3)	V_{CC} = 2.625 V,	f_{DCLK} = 77 MHz			144	mW
P_{OFFSET}	Power into V_{OFFSET} pin(3)	V_{OFFSET} = 8.75 V				9	mW
P_{BIAS}	Power into V_{BIAS} pin(3)	V_{BIAS} = 17 V				27.2	mW
P_{RESET}	Power into V_{RESET} pin (3)	V_{RESET} = –11 V				18	mW
C_I	Input capacitance	f = 1 MHz				10	pF
C_O	Output capacitance	f = 1 MHz				10	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw. See the *Micromirror Array Temperature Calculation* for further details.
(3) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See the *Micromirror Array Temperature Calculation* for further details.

6.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
t_{s1}	Setup time: DATA before rising or falling edge of DCLK	1			ns
	Setup time: TRC before rising or falling edge of DCLK	1			
	Setup time: SCTRL before rising or falling edge of DCLK	1			
t_{s2}	Setup time: $\overline{\text{LOADB}}$ low before rising edge of DCLK	1			ns
t_{s3}	Setup time: SAC_BUS low before rising edge of SAC_CLK	1			ns
t_{s4}	Setup time: DRC_BUS high before rising edge of SAC_CLK	1			ns
t_{s5}	Setup time: DRC_STROBE high before rising edge of SAC_CLK	1			ns
t_{h1}	Hold time: DATA after rising or falling edge of DCLK	1			ns
	Hold time: TRC after rising or falling edge of DCLK	1			
	Hold time: SCTRL after rising or falling edge of DCLK	1			
t_{h2}	Hold time: $\overline{\text{LOADB}}$ low after falling edge of DCLK	1			ns
t_{h3}	Hold time: SAC_BUS low after rising edge of SAC_CLK	1			ns
t_{h4}	Hold time: DRC_BUS after rising edge of SAC_CLK	1			ns
t_{h5}	Hold time: DRC_STROBE after rising edge of SAC_CLK	1			ns
t_{c1}	Clock cycle: DCLK	12.5		16.67	ns
t_{c3}	Clock cycle: SAC_CLK	12.5		16.67	ns
t_{w1}	Pulse duration high or low: DCLK	5			ns
t_{w2}	Pulse duration low: $\overline{\text{LOADB}}$	7			ns
t_{w3}	Pulse duration high or low: SAC_CLK	5			ns
t_{w5}	Pulse duration high: DRC_STROBE	7			ns
t_r	Rise time: DCLK / SAC_CLK			2.5	ns
	Rise time: DATA / TRC / SCTRL / $\overline{\text{LOADB}}$			2.5	
t_f	Fall time: DCLK / SAC_CLK			2.5	ns
	Fall time: DATA / TRC / SCTRL / $\overline{\text{LOADB}}$			2.5	

6.8 Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, consider the tester pin electronics and its transmission line effects. Figure 2 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

All rise and fall transition timing parameters are referenced to V_{IL} max and V_{IH} min for input clocks and V_{OL} max and V_{OH} min for output clocks.

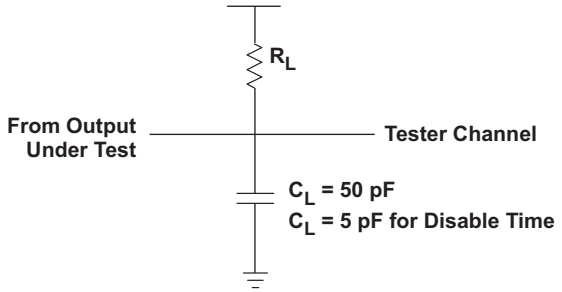


Figure 2. Test Load Circuit for AC Timing Measurements

Measurement Conditions (continued)

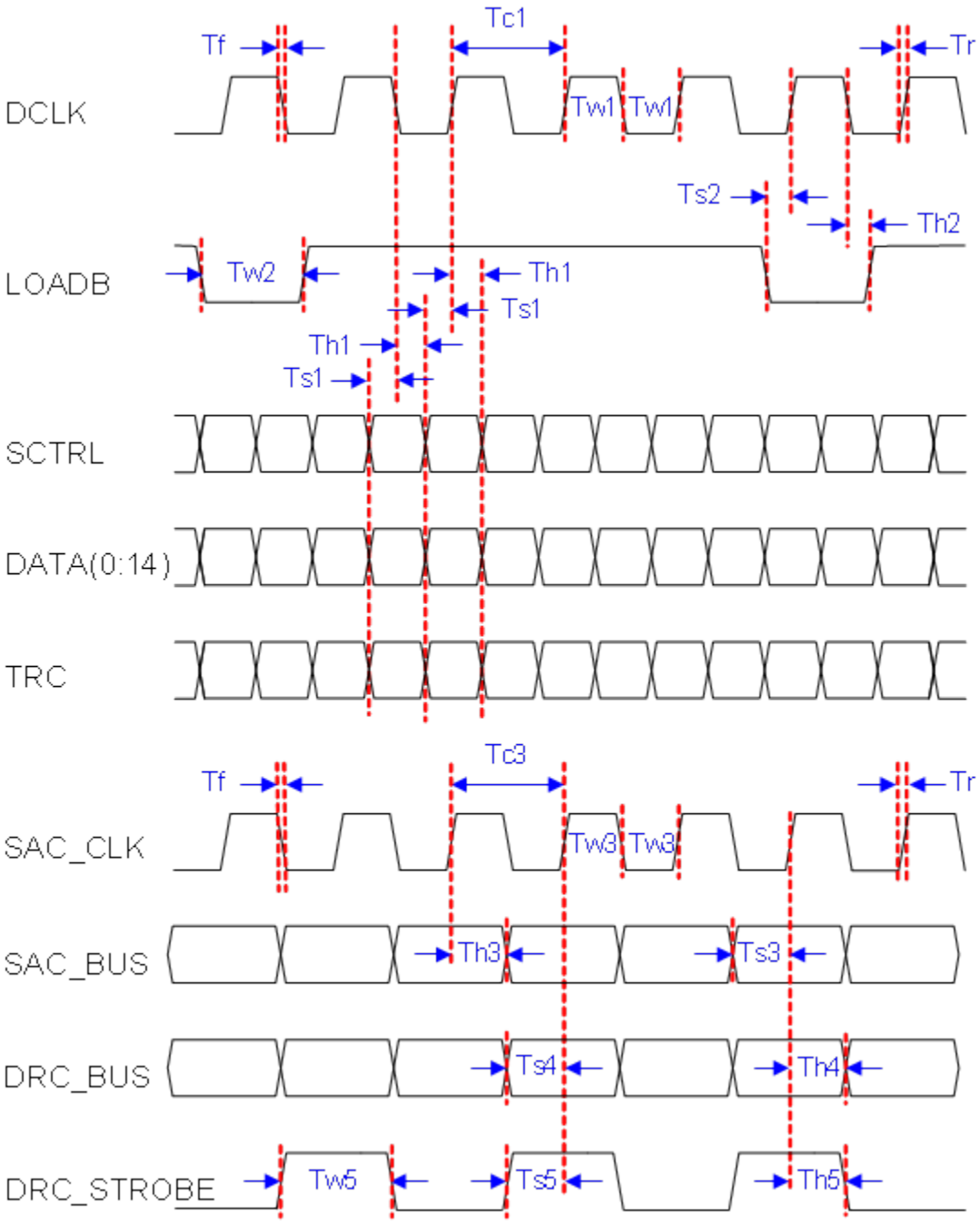


Figure 3. Switching Characteristics Diagram

6.9 Typical Characteristics

The DLP3000 DMD is controlled by the DLPC300 controller. The controller has two modes of operation. The first is Video mode where the video source is displayed on the DMD. The second is Pattern mode, where the patterns are pre-stored in flash memory and then streamed to the DMD. The allowed DMD pattern rate depends on which mode and bit-depth is selected.

Table 1. Bit Depth Versus Pattern Rate

COLOR MODE	BIT DEPTH	VIDEO MODE RATE (Hz)(1)	PATTERN MODE RATE (Hz)
Monochrome	1	1440	4000
	2	720	1600
	3	480	480
	4	360	360
	5	240	240
	6	240	240
	7	180	180
	8	120	120

(1) Video Mode pattern rate is based on a frame rate of 60 Hz.

6.10 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be	Package electrical connector area(1) (See Figure 4)			45	N
	DMD mounting area(2)			100	N

(1) Load should be uniformly distributed across the entire connector area.
(2) Load should be uniformly distributed across the three datum-A surfaces.

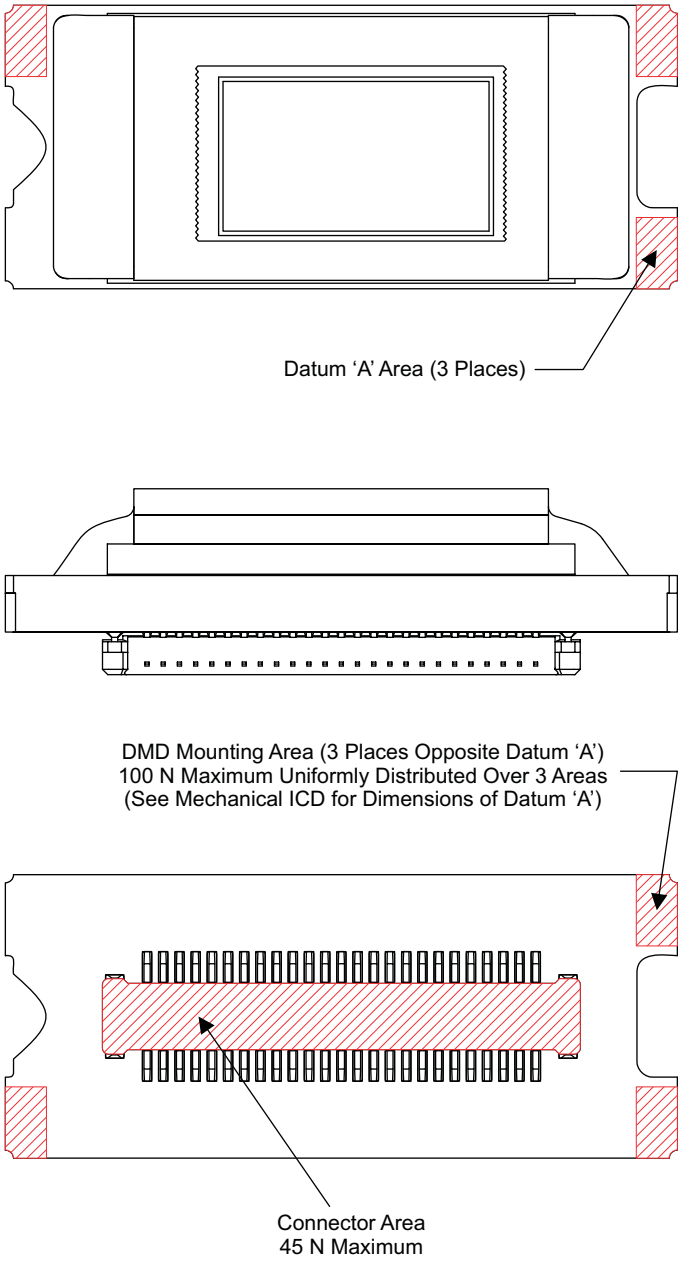


Figure 4. System Interface Loads

6.11 Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNIT
Number of active micromirror rows (1)	684	micromirrors
Number of active micromirror columns (1)	608	micromirrors
Micromirror pitch, diagonal (2)	7.637	µm
Micromirror pitch, vertical and horizontal (2)	10.8	µm
Micromirror active array height (3)	684	micromirrors
	3.699	mm
Micromirror active array width (3)	604	micromirrors
	6.5718	mm
Micromirror array border (4)	10	mirrors/side

(1) See Figure 7.
(2) See Figure 5.
(3) See Figure 6.
(4) The mirrors that form the array border are hard-wired to tilt in the –12° (off) direction once power is applied to the DMD (see Figure 9 and Figure 10).

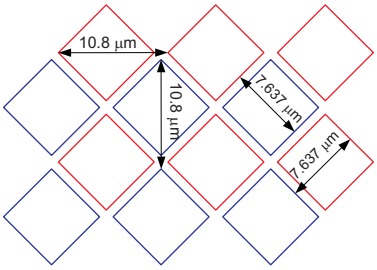


Figure 5. DLP3000 Pixel Pitch Dimensions

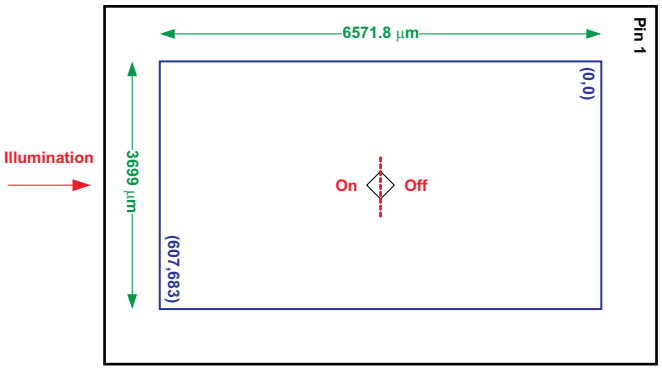


Figure 6. DLP3000 Micromirror Active Area

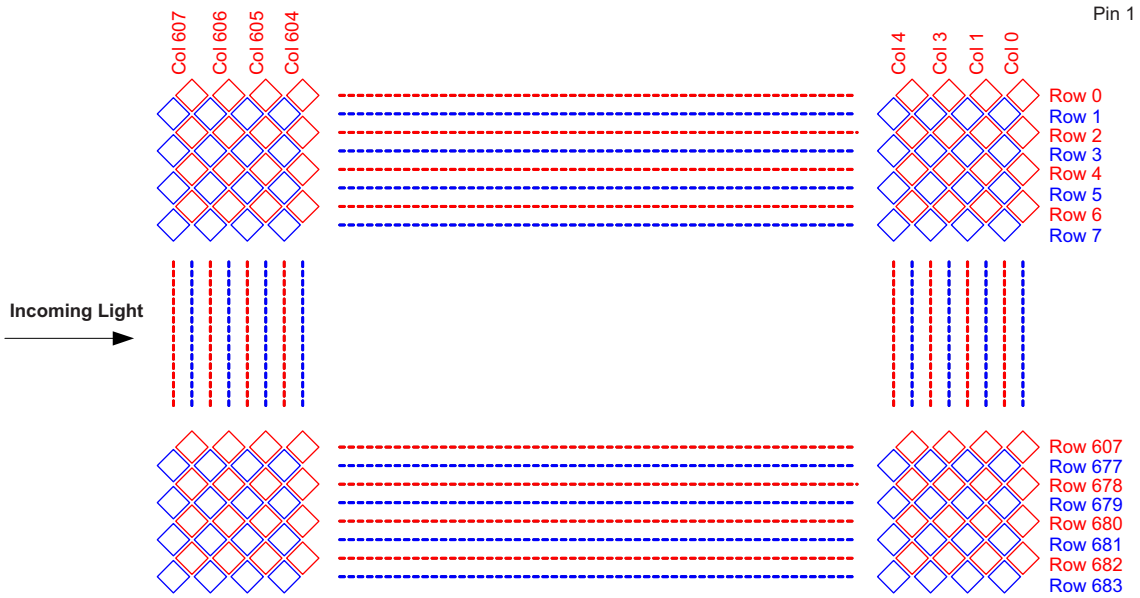


Figure 7. DLP3000 Pixel Arrangement

6.12 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD *parked* state(1)(2)(3), see Figure 10		0		°
		DMD *landed* state(1)(4)(5), see Figure 10		12		
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 10	–1		1	°
	Micromirror crossover time(9)			5		µs
	Micromirror switching time(9)			16		µs
	Non-operating micromirrors(10)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation(11)		89	90	91	°
	Micromirror array optical efficiency(12)(13)	420 to 700 nm, with all micromirrors in the ON state		68%		
	Mirror metal specular reflectivity (420 to 700 nm)			89.4%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Parking the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is *parked*, the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums.
(5) When the micromirror array is *landed*, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in an nominal angular position of +12°. A binary value of 0 results in a micromirror landing in an nominal angular position of –12°.
(6) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable nonuniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.
(9) Performance as measured at the start of life.
(10) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12° position to +12° or vice versa.
(11) Measured relative to the package datums B and C, shown in the Mechanical, Packaging, and Orderable Information.
(12) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
  (a) Illumination wavelength, bandwidth/line-width, degree of coherence
  (b) Illumination angle, plus angle tolerance
  (c) Illumination and projection aperture size, and location in the system optical path
  (d) Illumination overfill of the DMD micromirror array
  (e) Aberrations present in the illumination source and/or path
  (f) Aberrations present in the projection path

  The specified nominal DMD optical efficiency is based on the following use conditions:
  (a) Visible illumination (420 to 700 nm)
  (b) Input illumination optical axis oriented at 24° relative to the window normal
  (c) Projection optical axis oriented at 0° relative to the window normal
  (d) ƒ / 3 illumination aperture
  (e) ƒ / 2.4 projection aperture

  Based on these use conditions, the nominal DMD optical efficiency results from the following four components:
  (a) Micromirror array fill factor: nominally 92.5%
  (b) Micromirror array diffraction efficiency: nominally 86%
  (c) Micromirror surface reflectivity: nominally 88%
  (d) Window transmission: nominally 97% (single pass, through two surface transitions)
(13) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, projection aperture size, and micromirror array update rate.

NOTE

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the related application reports (listed in Related Documentation) for guidelines.

6.13 Window Characteristics

PARAMETER(1)	CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning Eagle XG				
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(2)	See(2)				
Illumination overfill(3)	See(3)				
Window transmittance, single–pass through both surfaces and glass (4)	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in section Mechanical, Packaging, and Orderable Information.
(3) Refer to *Illumination Overfill*.
(4) See the TI application report , *Wavelength Transmittance Considerations for DLP DMD Window* DLPA031.

6.14 Chipset Component Usage Specification

The DLP3000 is a component of one or more of DLP® chipsets. Reliable function and operation of the DLP3000 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

7 Detailed Description

7.1 Overview

The DLP3000 is a 0.3 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and diamond grid pixel arrangement are shown in Figure 9. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Double Data Rate (DDR) input data bus.

The DLP3000 is part of the DLP 0.3 WVGA chipset comprising of the DLP3000 DMD and the DLPC300 controller (reference Figure 8). To ensure reliable operation of the DLP3000 requires that it be used in conjunction with the DLPC300 controller.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

7.2 Functional Block Diagram

Figure 8 illustrates the connectivity between the individual components in the chipset, which include the following internal chipset interfaces:

- DLPC300 to DLP3000 data and control interface (DMD pattern data)
- DLPC300 to DLP3000 micromirror array reset control interface
- DLPC300 to mobile DDR SDRAM
- DLPC300 to SPI serial flash

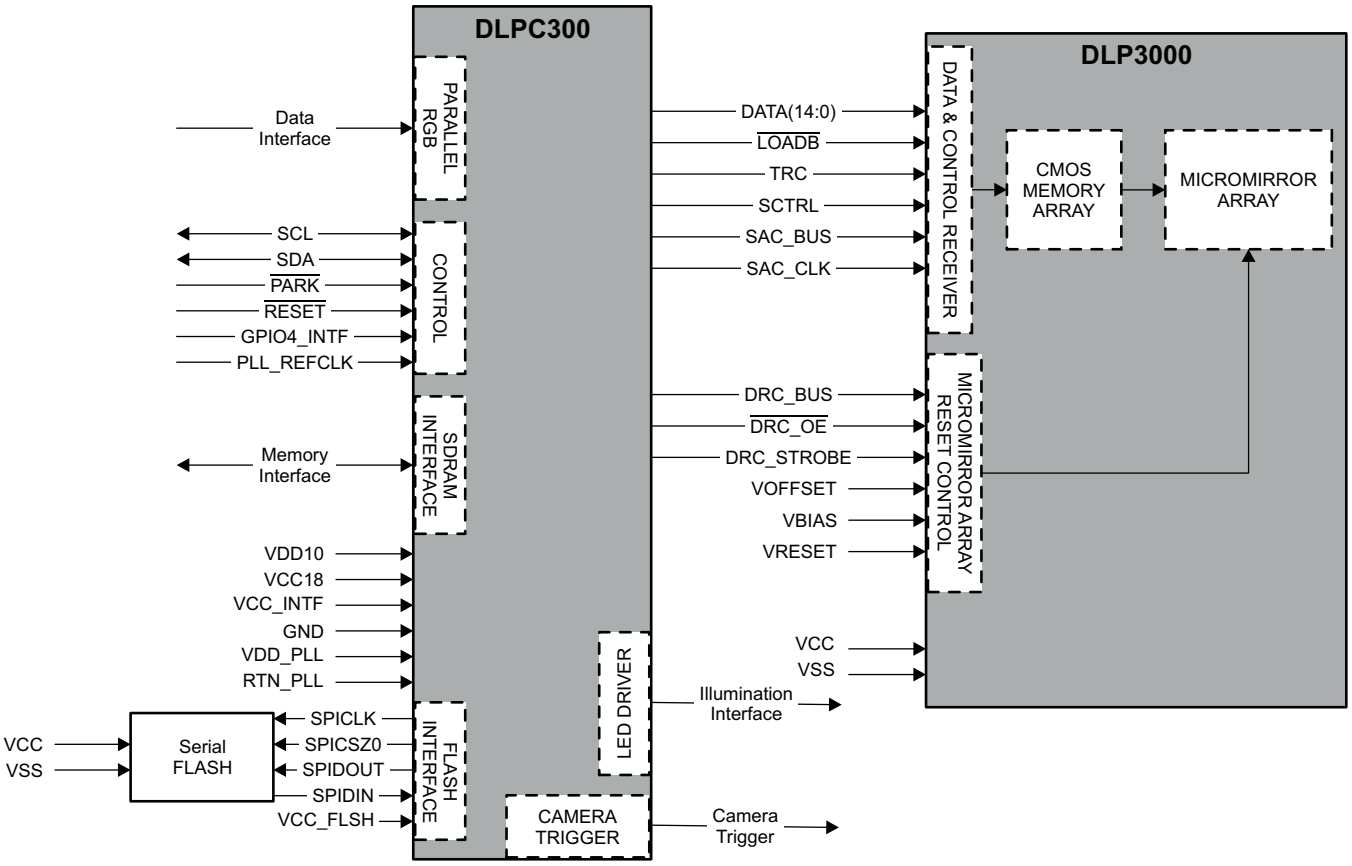


Figure 8. DLP 0.3 WVGA Chipset

7.3 Feature Description

Electrically, the DLP3000 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 608 memory cell columns by 684 memory cell rows. The CMOS memory array is addressed on a column-by-column basis, over a 15-bit DDR bus. Addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC300 digital controller.

Optically, the DLP3000 consists of 415872 highly-reflective, digitally-switchable, micrometer-sized mirrors (micromirrors) organized in a 2-D array. The micromirror array consists of 608 micromirror columns by 684 micromirror rows in diamond pixel configuration (Figure 9). Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row.

Each aluminum micromirror is approximately 7.6 microns in size (see *Micromirror Pitch* in Figure 9) and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° flat reference when the mirrors are parked in their inactive state, parallel to the array plane (see Figure 10). The tilt direction is perpendicular to the hinge-axis. The on-state landed position is directed toward the left side of the package (see *DLP3000 Active Mirror Array*, *Micromirror Pitch*, and *Micromirror Hinge-Axis Orientation* in Figure 9).

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps.

1. Update the contents of the CMOS memory.
2. Apply a mirror reset to all of the micromirror array. Mirror reset pulses are generated internally by the DLP3000 DMD, with application of the pulses being coordinated by the DLPC300 controller. See *Timing Requirements* timing specifications.

Around the perimeter of the 608 × 684 array of micromirrors is a uniform band of border micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position after power is applied to the device. There are 10 border micromirrors on each side of the 608 × 684 active array.

Feature Description (continued)

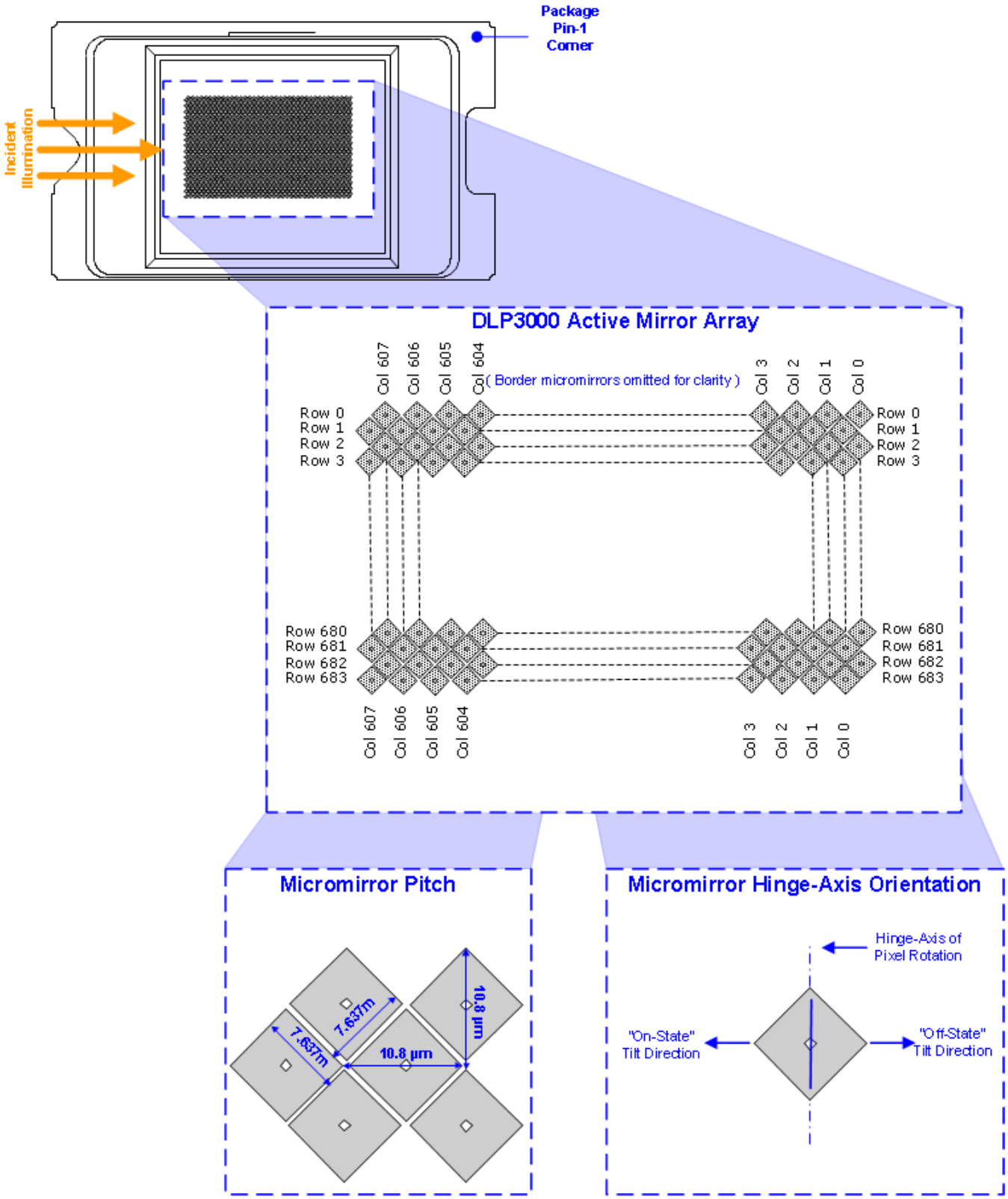


Figure 9. Micromirror Array, Pitch, and Hinge-Axis Orientation

Feature Description (continued)

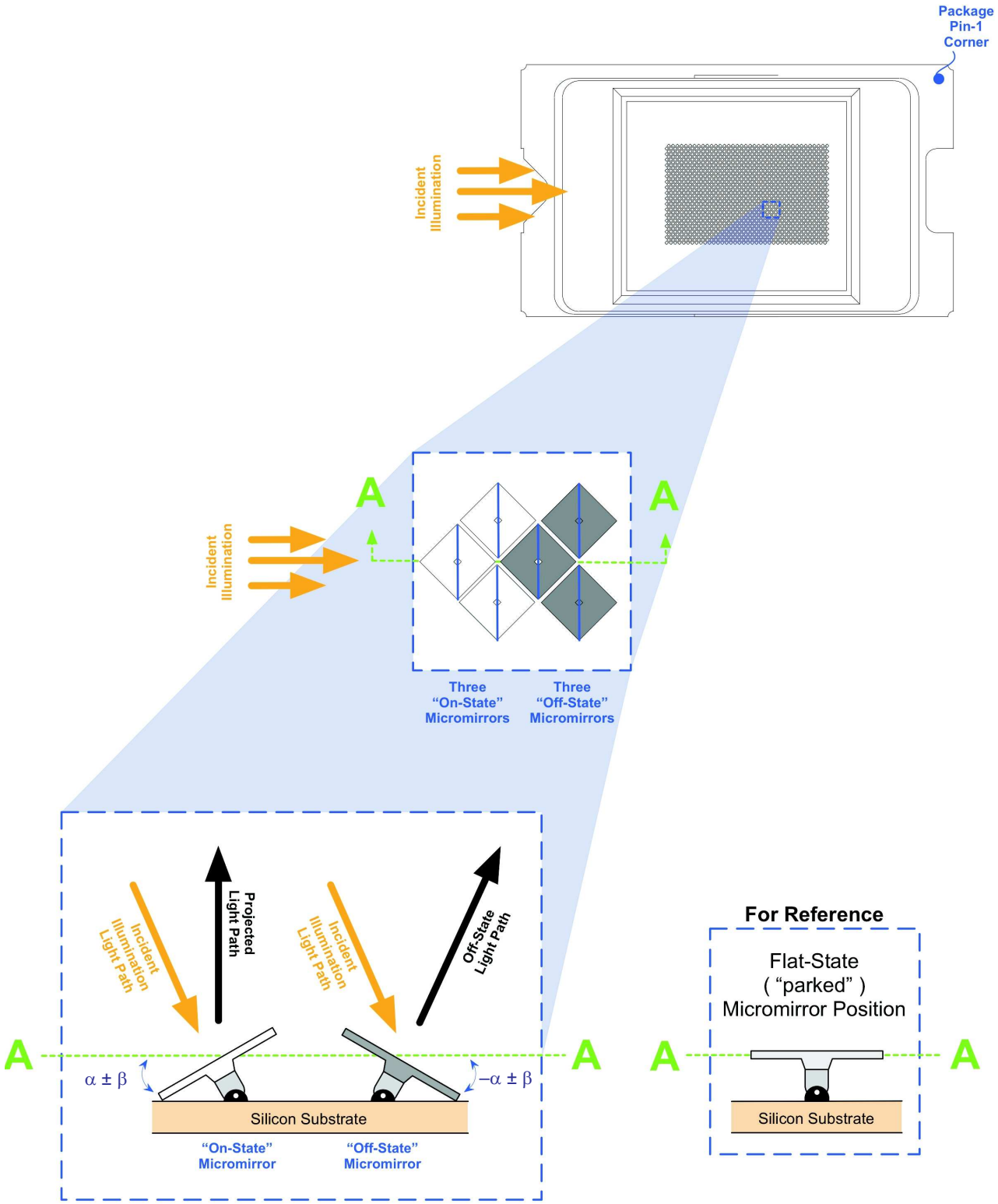


Figure 10. Micromirror Landed Positions and Light Paths

7.4 Device Functional Modes

DLP3000 is part of the chipset comprising of the DLP3000 DMD and DLPC300 display controller. To ensure reliable operation, DLP3000 DMD must always be used with a DLPC300 display controller.

DMD functional modes are controlled by the DLPC300 digital display controller. See the DLPC300 data sheet listed in *Related Documentation*.

7.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

See the *Absolute Maximum Ratings* and *Recommended Operating Conditions* for applicable temperature limits.

Micromirror Array Temperature Calculation (continued)

The DMD is designed to conduct the absorbed and dissipated heat back to the series 220 package where it can be removed by an appropriate system thermal management. The system thermal management must be capable of maintaining the package within the specified operational temperatures at the Thermal test point location, see Figure 11. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and/or parasitic heating.

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location is defined, as shown in Figure 11.

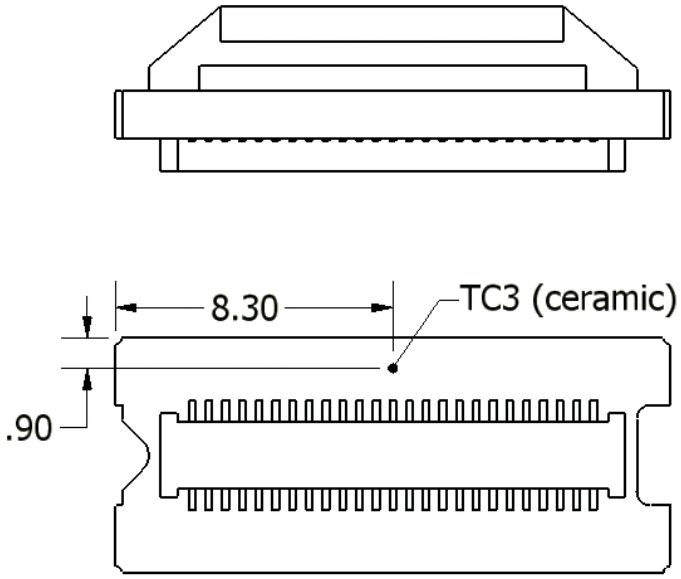


Figure 11. Thermal Test Point Location

Micromirror array temperature cannot be measured directly. Therefore, it must be computed analytically from:

- Thermal test point location (see Figure 11)
- Package thermal resistance
- Electrical power dissipation
- Illumination heat load

The relationship between the micromirror array and the case temperature is provided by the following equations:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) \quad (1)$$

$$Q_{Array} = Q_{Elec} + Q_{Illum} \quad (2)$$

$$Q_{Illum} = C_{L2W} \times SL \quad (3)$$

where

- T_{Array} = Computed micromirror array temperature (°C)
- $T_{Ceramic}$ = Ceramic case temperature (°C) (TC3 location)
- Q_{Array} = Total DMD array power (electrical + absorbed) (W)
- $R_{Array\text{-}to\text{-}Ceramic}$ = Thermal resistance of DMD package from array to TC3 (°C/W)
- Q_{Elec} = Nominal electrical power (W)
- Q_{Illum} = Absorbed illumination heat (W)
- C_{L2W} = Lumens-to-watts constant, estimated at 0.00293 W/lm, based on array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light, illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.
- SL = Screen lumens

Micromirror Array Temperature Calculation (continued)

These equations are based on traditional 1-chip DLP system with a total projection efficiency from the DMD to the screen of 87%. An example calculation is provided in Equation 4 and Equation 5. DMD electrical power dissipation varies and depends on the voltage, data rates, and operating frequencies. The nominal electrical power dissipation used in this calculation is 0.15 W. Screen lumens is nominally 20 lm. The ceramic case temperature at TC3 is 55°C. Using these values in the previous equations, the following values are computed:

$$Q_{Array} = Q_{Elec} + C_{L2W} \times SL = 0.144\ W + (0.00293\ W/Lumen \times 20\ Lumen) = 0.2026\ W \quad (4)$$

$$T_{Array} = T_{Ceramic} + (Q_{Array} * R_{Array\text{-}To\text{-}Ceramic}) = 55°C + (0.2026\ W \times 5\ °C/W) = 56.01°C \quad (5)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On–state 100% of the time (and in the Off–state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off–state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational Array Temperature

Operational Array Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating Array Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 2.

Table 2. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value) (6)

Where:

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 3.

Table 3. Example Landed Duty Cycle for Full-Color

Red Cycle Percentage 50%	Green Cycle Percentage 20%	Blue Cycle Percentage 30%	Landed Duty Cycle
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP3000 along with the DLPC300 controller provides a solution for many applications including structured light and video projection. The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC300. Applications of interest include 3D machine vision, 3D printing, and spectroscopy.

8.2 Typical Application

A typical embedded system application using the DLPC300 controller and a DLP3000 is shown in Figure 12. In this configuration, the DLPC300 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system configuration supports still and motion video sources plus sequential pattern mode. Refer to Related Documents for the DLPC300 digital controller data sheet.

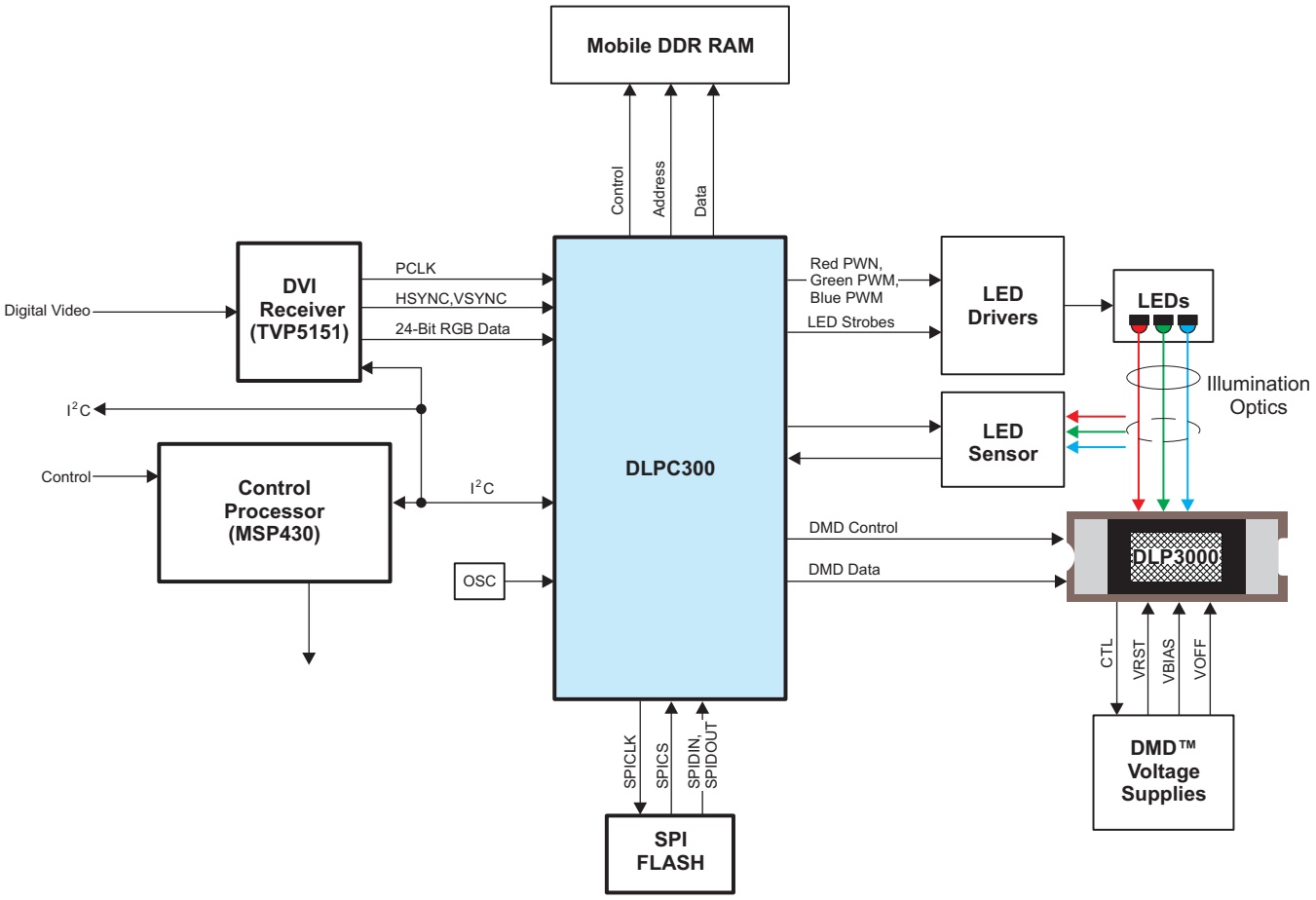


Figure 12. Typical System Block Diagram

Typical Application (continued)

8.2.1 Design Requirements

Detailed design requirements are located in the DLPC300 digital controller data sheet. Refer to *Related Documentation*.

8.2.2 Detailed Design Procedure

See the reference design schematic for connecting together the DLPC300 display controller and the DLP3000 DMD. An example board layout is included in the DLP 0.3 WVGA Chipset Reference Design. *Layout Guidelines* should be followed for reliability.

8.2.3 Application Curve

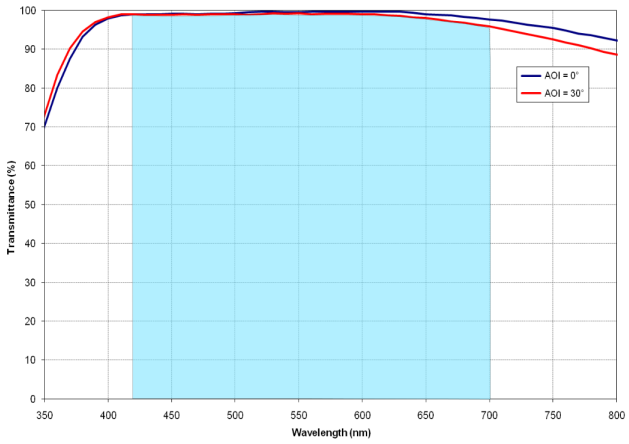


Figure 13. Corning Eagle XG Visible AR Coating Transmittance

9 Power Supply Recommendations

9.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: six voltage-level supplies (V_{SS},V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}). For reliable operation of DLP3000, the following power-supply sequencing requirements must be followed.

CAUTION

Reliable performance of the DMD requires that the following conditions be met:

- The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supply inputs all be present during operation.
- The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies be sequenced on and off in the manner prescribed.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

9.2 DMD Power Supply Power-Up Procedure

Follow these steps to power-up the DMD power supply.

1. Power up V_{CC} and V_{REF} in any order.
2. Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.
3. Power up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).

NOTE

During the power-up procedure, the DMD LVCMOS inputs should not be driven high until after step 2 is completed. Power supply slew rates during power up are unrestricted, provided that all other conditions are met.

9.3 DMD Power Supply Power-Down Procedure

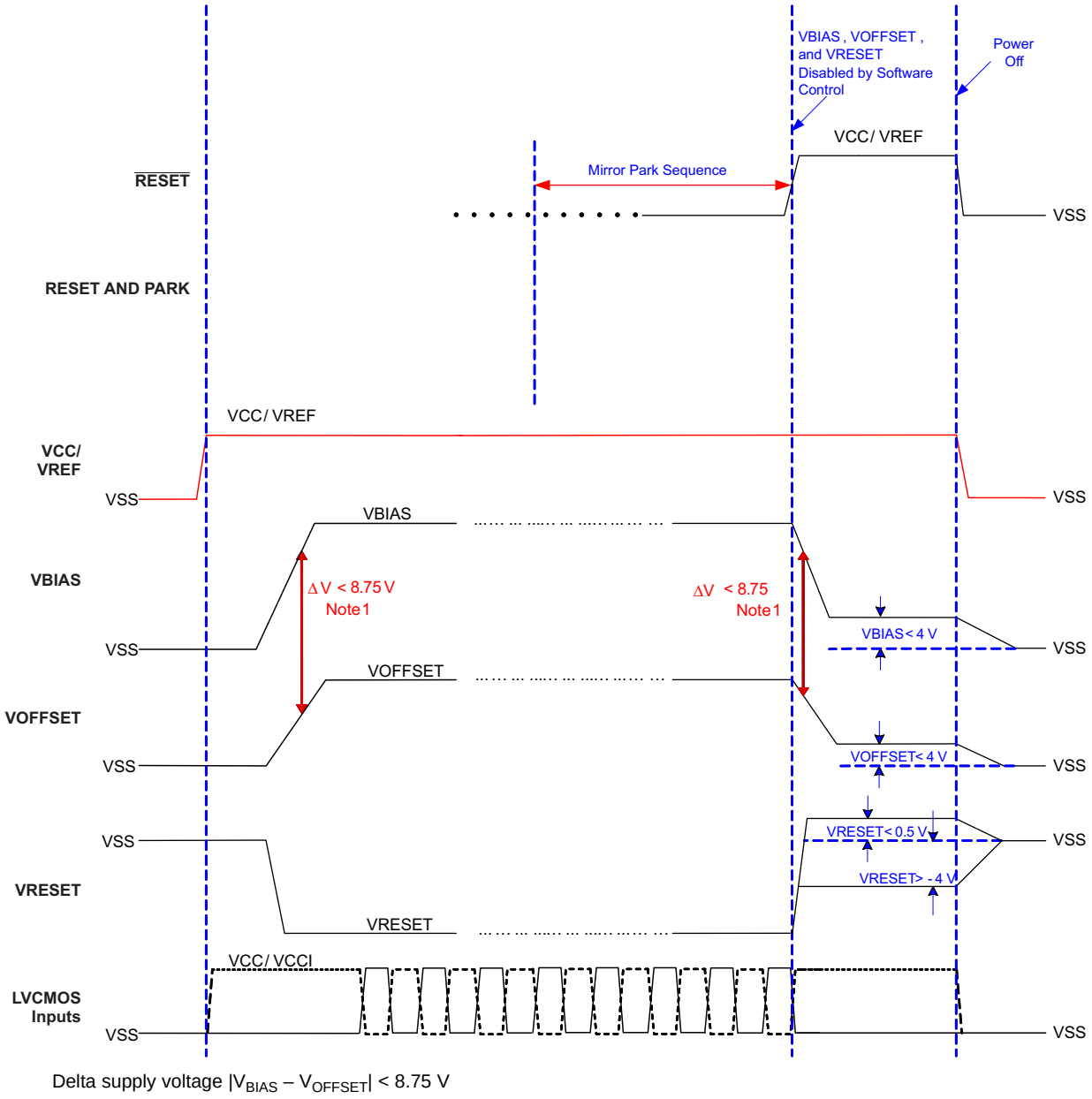
Follow these steps to power-down the DMD power supply.

1. Command the chipset controller to execute a mirror-parking sequence. See the controller data sheet (listed in Related Documentation) for details.
2. Power down V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).
3. Wait for V_{BIAS}, V_{OFFSET}, and V_{RESET} to each discharge to a stable level within 4 V of the reference ground.
4. Power down V_{CC} and V_{REF} in any order.

NOTE

During the power-down procedure, the DMD LVCMOS inputs should be held at a level less than V_{REF} + 0.3 V. Power-supply slew rates during power down are unrestricted, provided that all other conditions are met.

DMD Power Supply Power-Down Procedure (continued)



Delta supply voltage $|V_{BIAS} - V_{OFFSET}| < 8.75$ V

Figure 14. Power-Up and Power-Down Timing

10 Layout

10.1 Layout Guidelines

The 0.3 WVGA chipset is a high-performance (high-frequency and high-bandwidth) set of components. This section provides PCB guidelines to ensure proper operation of the 0.3 WVGA chipset with respect to the mobile DDR memory and the DMD interface.

10.1.1 Printed Circuit Board Design Guidelines

The PCB design may vary depending on system design. Table 4 provides general recommendations on the PCB design.

Table 4. PCB General Recommendations for MDDR and DMD Interfaces

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	0.5-oz. (0.18-mm thick) copper
Single-ended signal impedance	50 Ω (± 10%)
Differential signal impedance	100 Ω differential (± 10%)

10.1.2 Printed Circuit Board Layer Stackup Geometry

The PCB layer stack may vary depending on system design. However, careful attention is required in order to meet design considerations listed in the following sections. Table 5 provides general guidelines for the mDDR and DMD interface stackup geometry.

Table 5. PCB Layer Stackup Geometry for MDDR and DMD Interfaces

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Er	Dielectirc FR4	4.2 (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	34.2 mil (0.869 mm)
Reference plane 2	I/O power plane or ground	

10.1.3 Signal Layers

The PCB signal layers should follow these recommendations:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.

10.1.4 DMD Interfaces

10.1.4.1 DLPC300-to-DLP3000 Digital Data

The DLPC300 provides the DMD pattern data to the DMD over a double data rate (DDR) interface. Table 6 describes the signals used for this interface.

Table 6. Active Signals – DLPC300-to-DLP3000 Digital Data Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME
DMD_D(14:0)	DATA(14:0)
DMD_DCLK	DCLK

10.1.4.2 DLPC300-to-DLP3000 Control Interface

The DLPC300 provides the control data to the DMD over a serial bus. Table 7 describes the signals used for this interface.

Table 7. Active Signals – DLPC300 to DLP3000 Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD\_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

10.1.4.3 DLPC300-to-DLP3000 Micromirror Reset Control Interface

The DLPC300 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD. Table 8 describes the signals used for this interface.

Table 8. Active Signals – DLPC300-to-DLP3000 Micromirror Reset Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD\_DRC\_OE}}$	$\overline{\text{DRC\_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

10.1.5 Routing Constraints

In order to meet the specifications listed in Table 9 and Table 10, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long traces all around the PCB.

Table 9. Signal Length Routing Constraints for MDDR and DMD Interfaces

SIGNALS	MAX SIGNAL SINGLE-BOARD ROUTING LENGTH	MAX SIGNAL MULTI-BOARD ROUTING LENGTH
DMD_D(14:0), $\overline{\text{DMD\_CLK}}$, DMD_TRC, DMD_SCTRL, $\overline{\text{DMD\_LOADB}}$, $\overline{\text{DMD\_OE}}$, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	4 in (10.15 cm)	3.5 in (8.8891 cm)
MEM_CLK_P, MEM_CLK_N, MEM_A(12:0), MEM_BA(1:0), MEM_CKE, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_RAS}}$, $\overline{\text{MEM\_CAS}}$, and $\overline{\text{MEM\_WE}}$	2.5 in (6.35 cm)	Not recommended
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	1.5 in (3.81 cm)	Not recommended

Each high-speed, single-ended signal must be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping lengths to a minimum. The following signals should follow these signal matching requirements.

Table 10. High-Speed Signal Matching Requirements for MDDR and DMD Interfaces

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OE,	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS	DMD_DCLK	±750 (19.05)	mil (mm)
DMD_SAC_CLK	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_SAC_BUS	DMD_SAC_CLK	±750 (19.05)	mil (mm)
MEM_CLK_P	MEM_CLK_N	±150 (3.81)	mil (mm)
MEM_DQ(7:0), MEM_LDM	MEM_LDQS	±300 (7.62)	mil (mm)
MEM_DQ(15:8), MEM_UDM	MEM_UDQS	±300 (7.62)	mil (mm)
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, MEM_WE	MEM_CLK_P, MEM_CLK_N	±1000 (25.4)	mil (mm)
MEM_LDQS, MEM_UDQS	MEM_CLK_P, MEM_CLK_N	±300 (7.62)	mil (mm)

10.1.6 Termination Requirements

Table 11 lists the termination requirements for the DMD and mDDR interfaces.

For applications where the routed distance of the mDDR or DMD signal can be kept less than 0.75 inches, then this signal is short enough not to be considered a transmission line and should not need a series terminating resistor.

Table 11. Termination Requirements for MDDR and DMD Interfaces

SIGNALS	SYSTEM TERMINATION
DMD_D(14:0), DMD_CLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	Terminated at source with 10-Ω to 30-Ω series resistor. 30 Ω is recommended for most applications as this minimizes over/under-shoot and reduces EMI.
MEM_CLK_P and MEM_CLK_N	Terminated at source with 30-Ω series resistor. The pair should also be terminated with an external 100-Ω differential termination across the two signals as close to the mDDR as possible.
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	Terminated with 30-Ω series resistor located midway between the two devices
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, and MEM_WE	Terminated at the source with a 30-Ω series resistor

10.2 Layout Example

The interface between the DLP3000 and DLPC300 is typically connected through a board to board interface using a flex cable. The signal length and matching constraints listed in Table 9 and Table 10 should be considered in the board layout and flex cable design. Figure 15 shows a flex cable example from the LightCrafter Evaluation Module. The length of the cable is 2.362 in (60 mm).

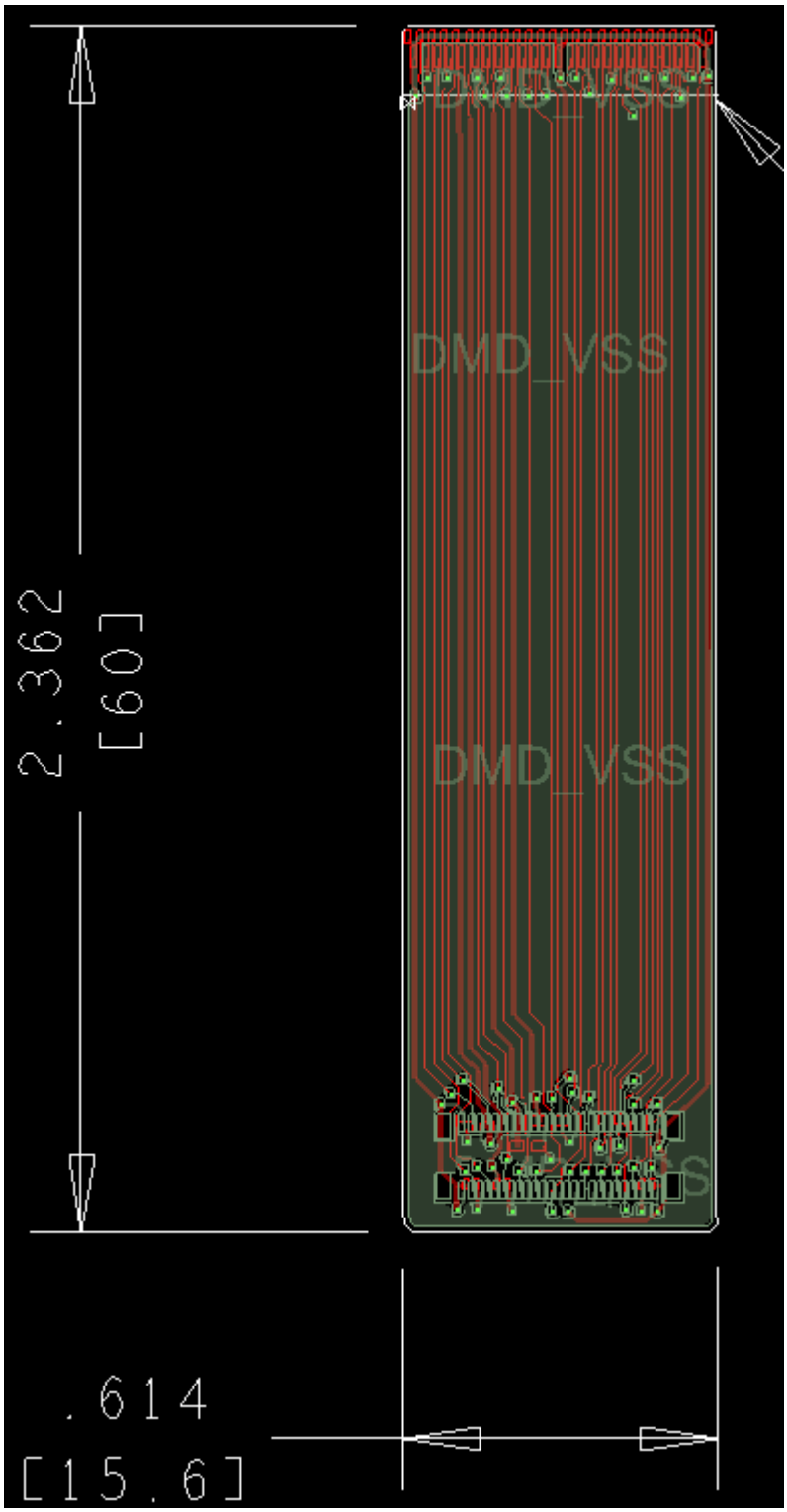


Figure 15. Flex Cable Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 16 provides a legend for reading the device name for any DLP device.

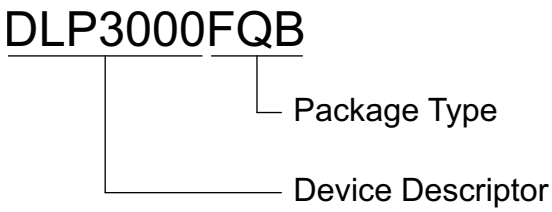


Figure 16. Device Nomenclature

11.1.1.1 Device Marking

The device marking consists of the fields shown in Figure 17.

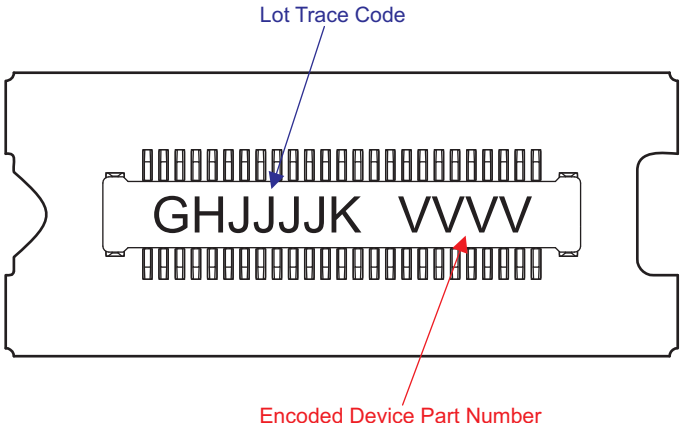


Figure 17. Device Marking

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP3000 device:

- *DLP 0.3 WVGA chipset data sheet,* DLPZ005
- *DLPC300 digital controller data sheet,* DLPS023
- *DLPC300 Software Programmer's Guide,* DLPU004

11.3 Trademarks

DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3000FQB	ACTIVE	LCCC	FQB	50	10	RoHS & Green	Call TI	Level-1-NC-NC			Samples
DLP3000FQBDH	ACTIVE	LCCC	FQB	50	10	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

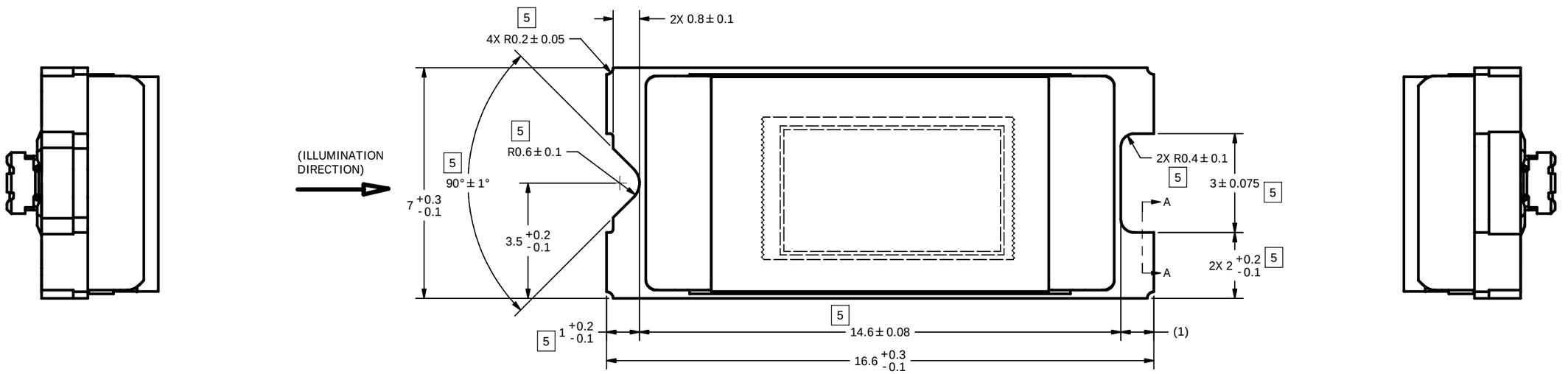
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

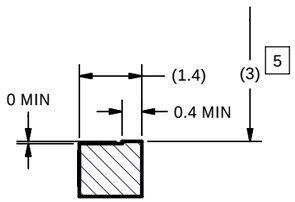
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2097098 INITIAL RELEASE	03/02/09	J. HOLM
B	ECO 2098984 TIGHTEN DIE ROTATION, NOTE 2; ADD 'DD1' SUFFIX TO CONNECTOR PART#; CHG DWG TO INVENTOR	08/27/09	BMH

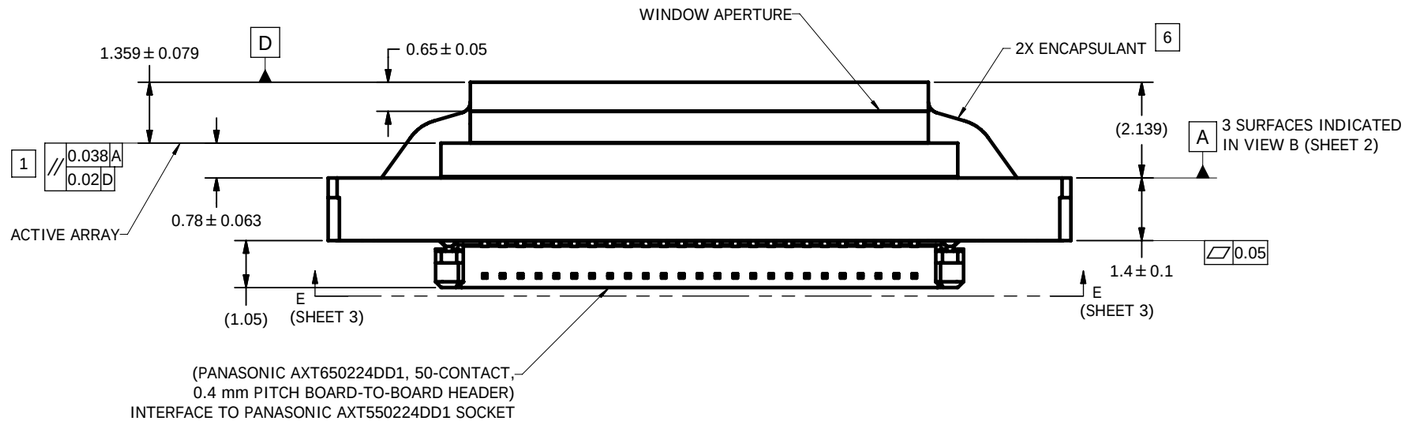
NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR ON BOTTOM OF CONNECTOR.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND G (SHEET 2).





SECTION A-A
NOTCH OFFSETS



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NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1'
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	2/25/2009
ENGINEER	B. HASKETT	2/25/2009
QA/CE	P. KONRAD	3/9/2009
CM		
	J. GRIMMETT	3/9/2009
APPROVED		

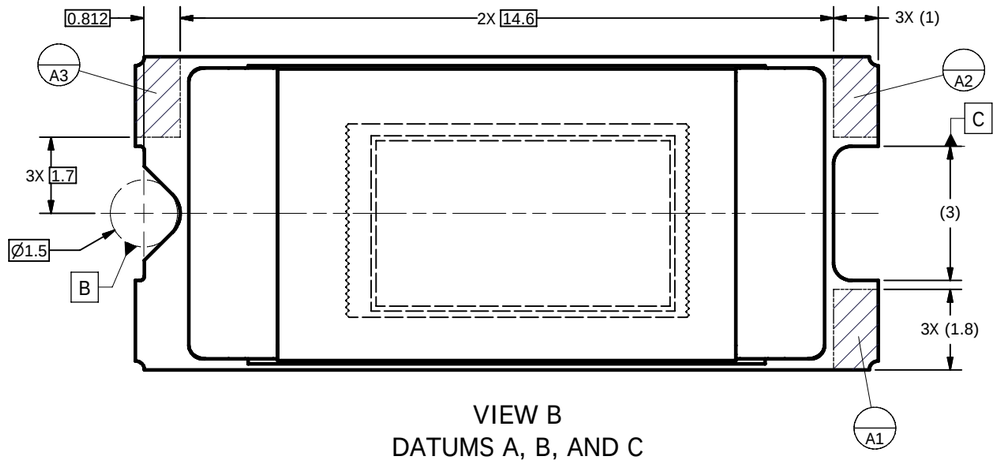
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.3 WVGA DDR SERIES 220
0.4 mm PITCH CONNECTOR

SIZE		DWG NO	REV
D		2510388	B

SCALE 15:1 SHEET 1 OF 3

INV11-2006a



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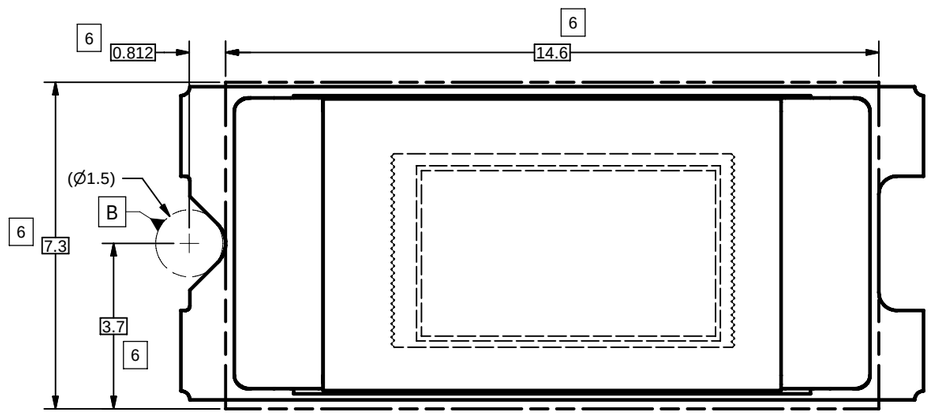

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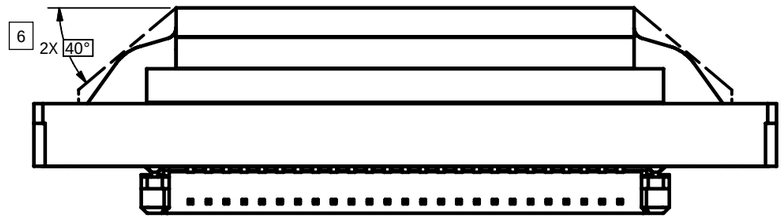

VIEW G
ENCAPSULANT HEIGHT LIMITS

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 2 OF 3	

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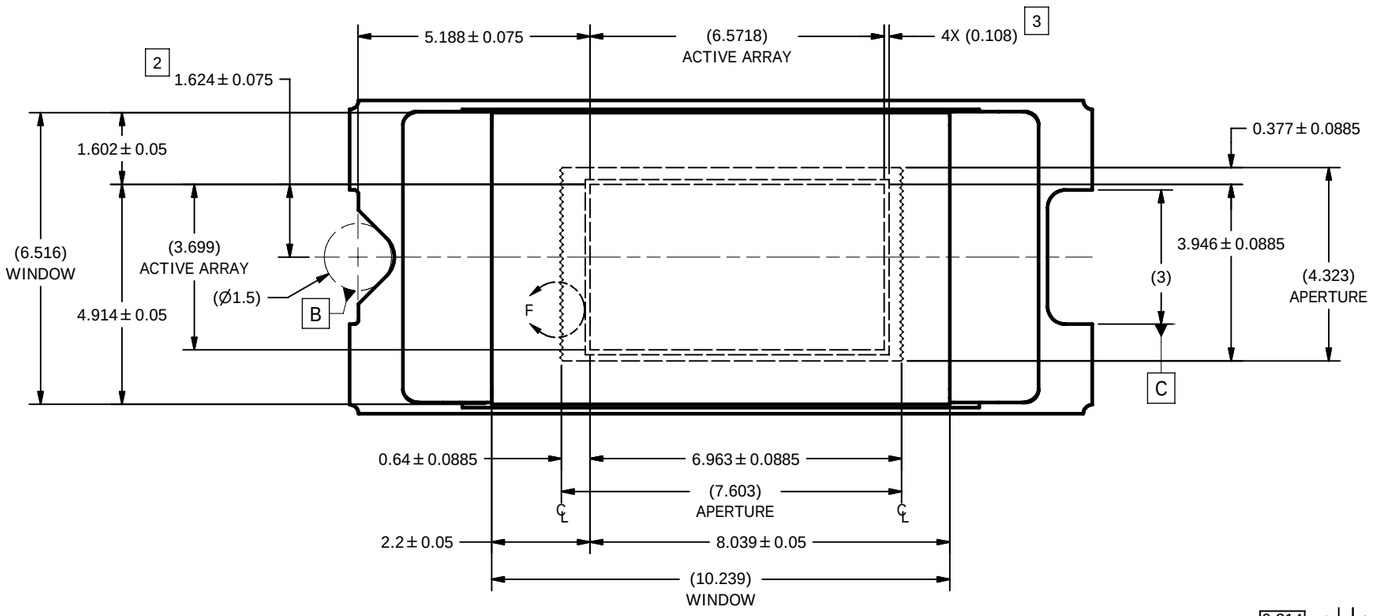

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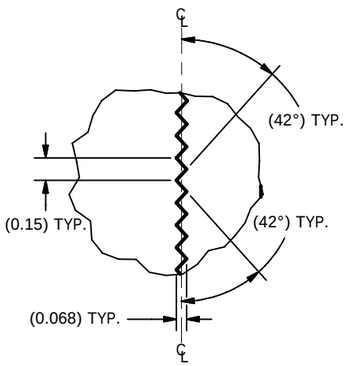
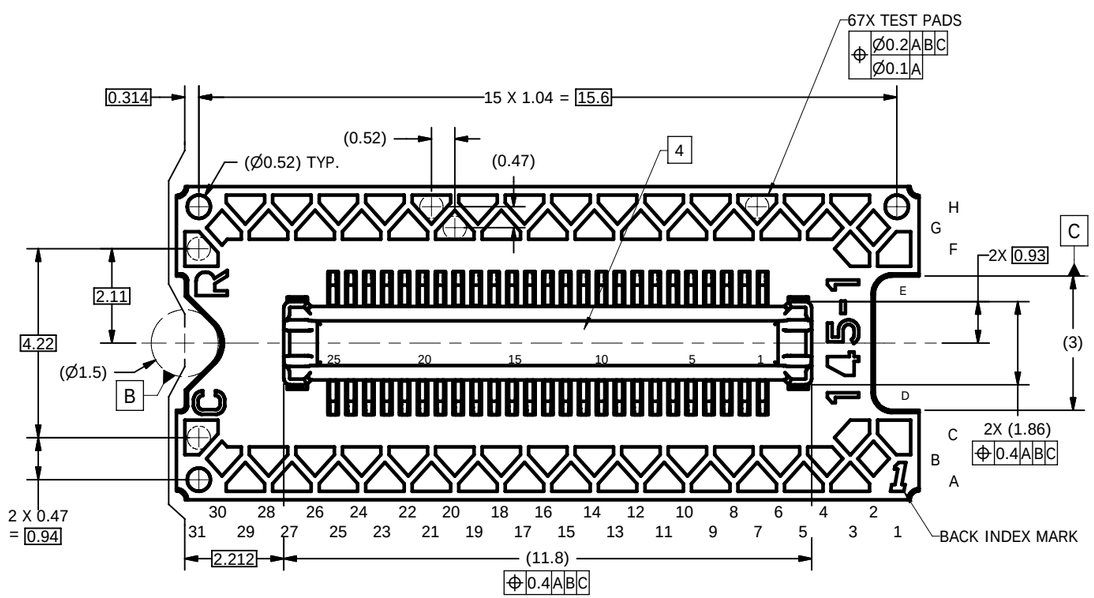


DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 3 OF 3	

INV11-2006a

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DLP3000FQB	LIFEBUY	CLGA	FQB	50		RoHS & non-Green					

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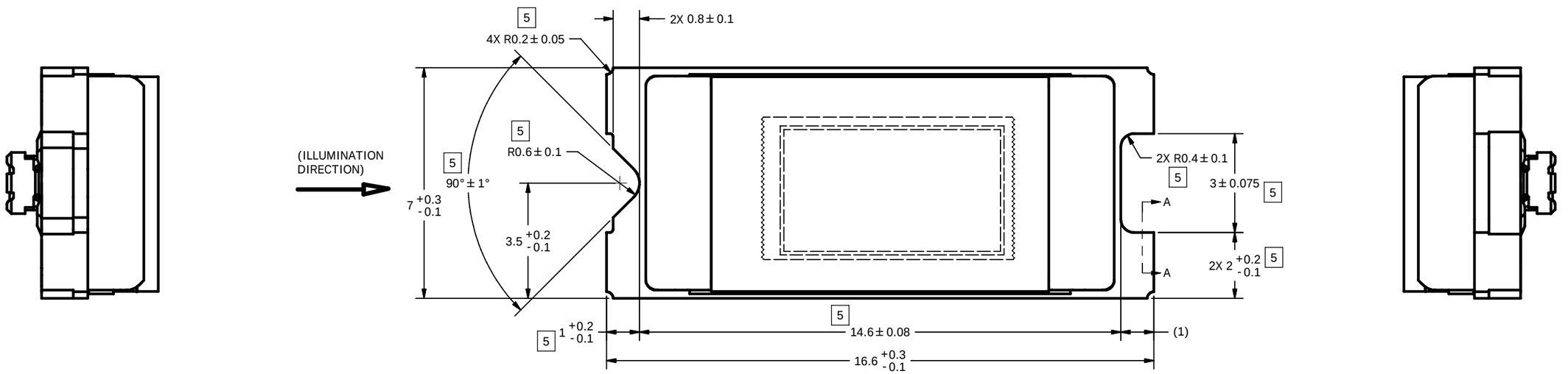
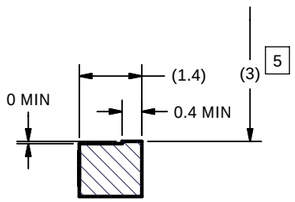
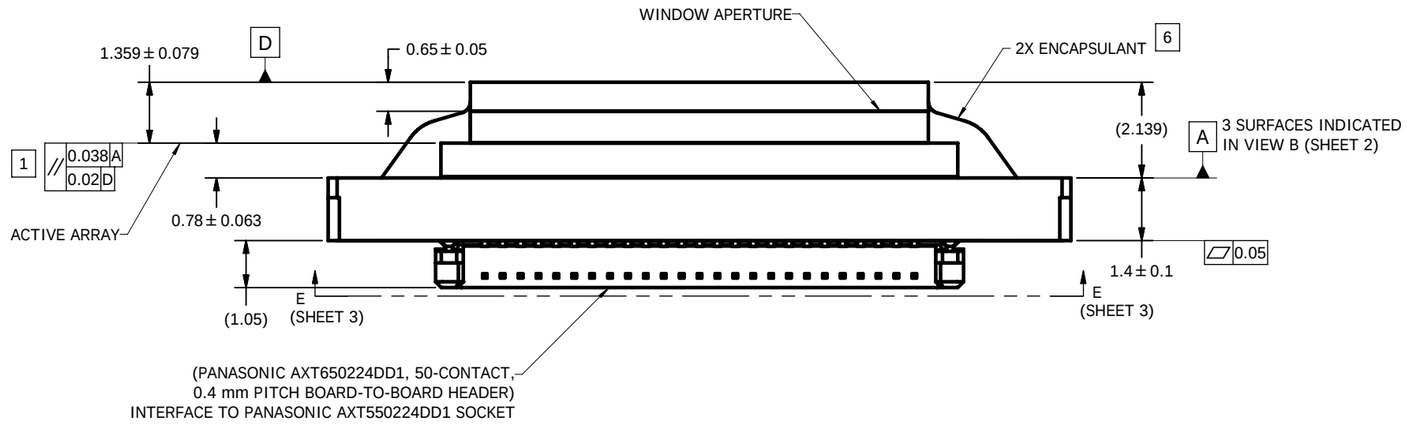




SECTION A-A
NOTCH OFFSETS



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NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

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SCALE 15:1 SHEET 1 OF 3

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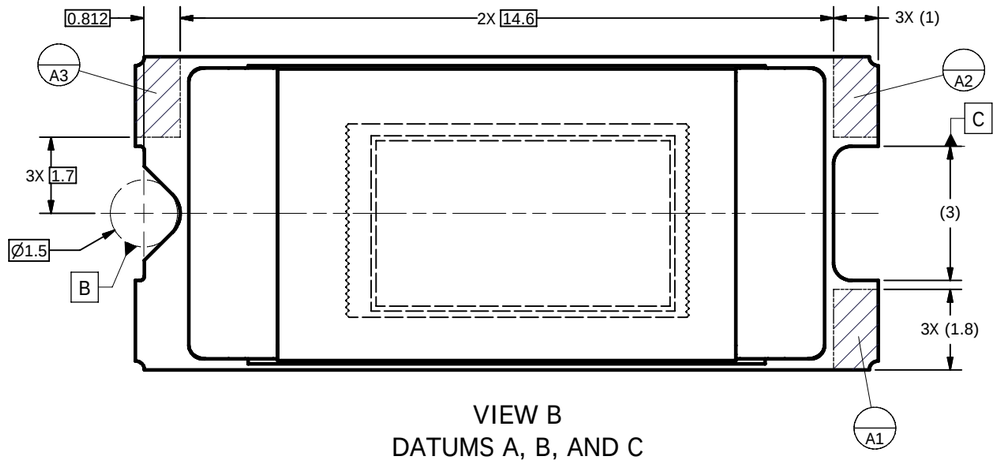
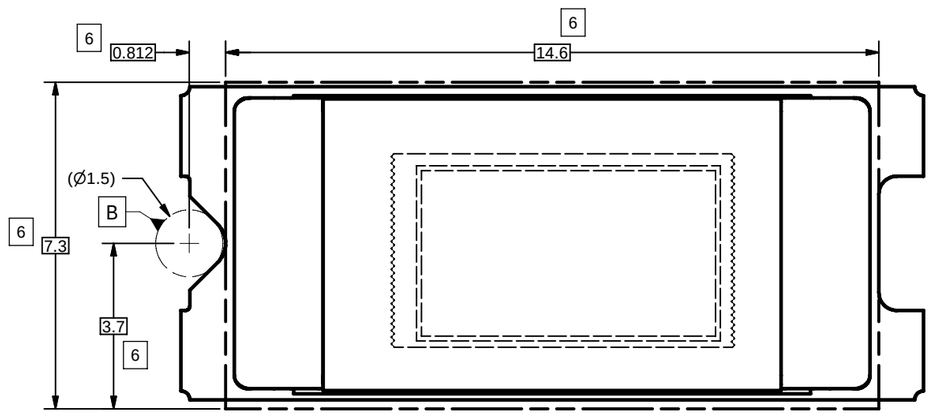
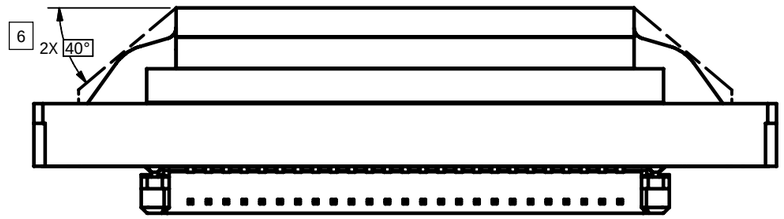


VIEW B
DATUMS A, B, AND C
(FROM SHEET 1)



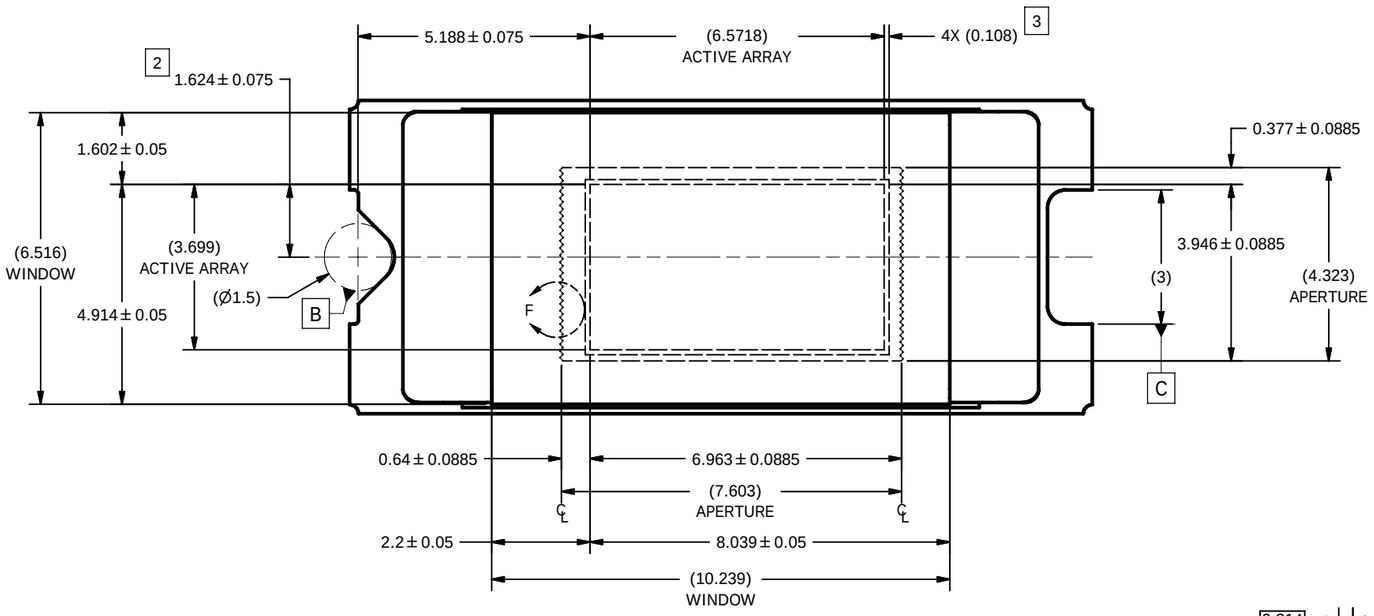
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



VIEW G
ENCAPSULANT HEIGHT LIMITS

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 2 OF 3	

INV11-2006a



VIEW D
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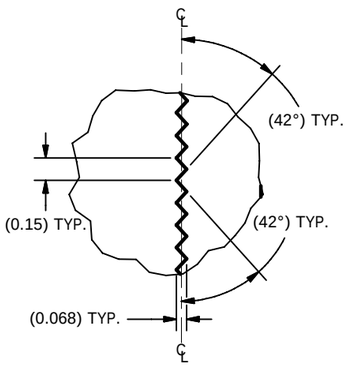
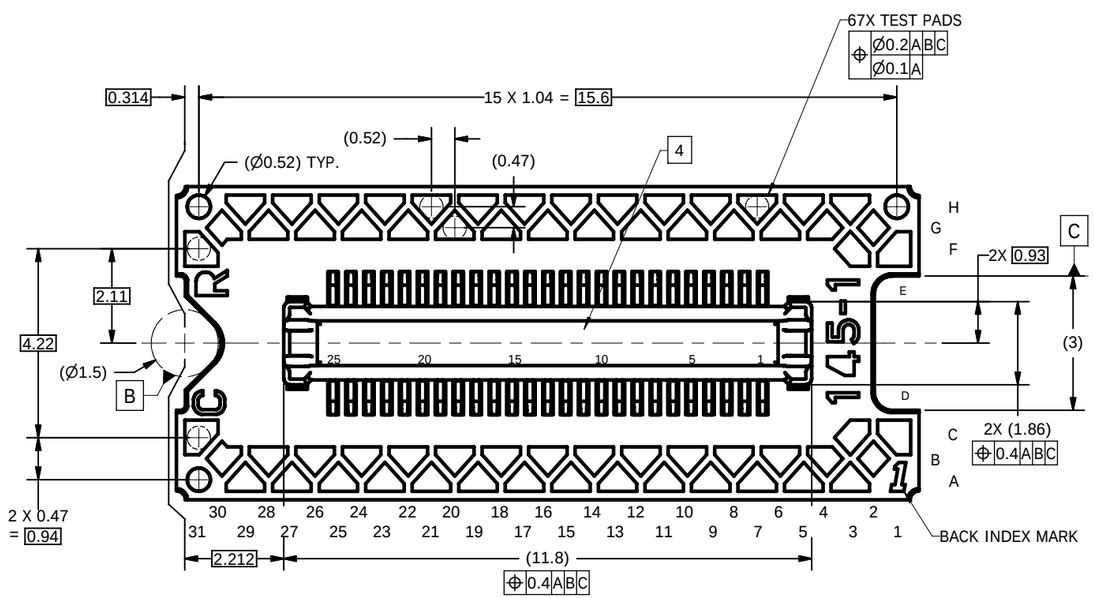
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 3 OF 3	

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